National Semiconductor

August 1989

MM54HC4051/MM74HC4051 8-Channel Analog Multiplexer MM54HC4052/MM74HC4052 Dual 4-Channel Analog Multiplexer MM54HC4053/MM74HC4053 Triple 2-Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low ''on'' resistance and low ''off'' leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when $V_{CC} = 5V$ and an analog input range of ±5V when $V_{EE} = 5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is ''on'', and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is ''on'', connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

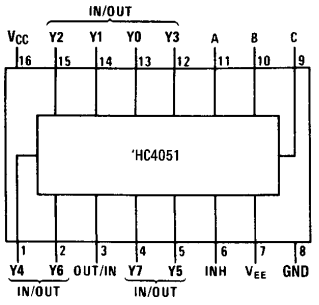
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be ''on''.

Features

- Wide analog input voltage range: ±6V
- Low ''on'' resistance: 50 typ. ($V_{CC}-V_{EE} = 4.5V$)
  30 typ. ($V_{CC}-V_{EE} = 9V$)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

Connection Diagrams

Dual-In-Line Packages



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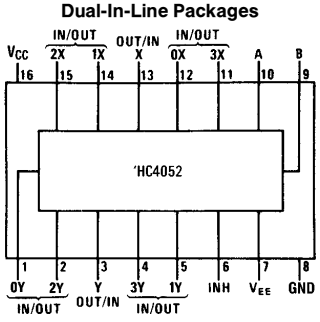
Top View



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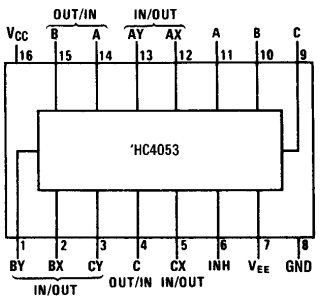
Top View



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Top View

Order Number MM54HC4051, MM74HC4051, MM54HC4052, MM74HC4052, MM54HC4053 or MM74HC4053

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
Switch I/O Voltage (V_{IO})	V_{EE} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V	1000		ns
V_{CC} = 4.5V	500		ns
V_{CC} = 6.0V	400		ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
						Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0V		1.5	1.5	1.5	V
					4.5V		3.15	3.15	3.15	V
					6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**				2.0V		0.5	0.5	0.5	V
					4.5V		1.35	1.35	1.35	V
					6.0V		1.8	1.8	1.8	V
R_{ON}	Maximum "ON" Resistance (Note 5)		V_{INH} = V_{IL}, I_S = 2.0 mA	GND	4.5V	40	160	200	240	Ω
			V_{IS} = V_{CC} to V_{EE}	−4.5V	4.5V	30	120	150	170	Ω
			(Figure 1)	−6.0V	6.0V	20	100	125	140	Ω
			V_{INH} = V_{IL}, I_S = 2.0 mA	GND	2.0V	100	230	280	320	Ω
			V_{IS} = V_{CC} or V_{EE}	GND	4.5V	40	110	140	170	Ω
			(Figure 1)	−4.5V	4.5V	20	90	120	140	Ω
				−6.0V	6.0V	15	80	100	115	Ω
R_{ON}	Maximum "ON"Resistance Matching		V_{CTL} = V_{IL}	GND	4.5V	10	20	25	25	Ω
			V_{IS} = V_{CC} to GND	−4.5V	4.5V	5	10	15	15	Ω
				−6.0V	6.0V	5	10	12	15	Ω
I_{IN}	Maximum Control Input Current		V_{IN} = V_{CC} or GND				±0.1	±1.0	±1.0	μA
			V_{CC} = 2−6V							
I_{CC}	Maximum Quiescent Supply Current		V_{IN} = V_{CC} or GND	GND	6.0V		8	80	160	μA
			I_{OUT} = 0 μA	−6.0V	6.0V		16	160	320	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current (Switch Input)		V_{OS} = V_{CC} or V_{EE}	GND	6.0V		±60	±600	±600	nA
			V_{IS} = V_{EE} or V_{CC}	−6.0V	6.0V		±100	±1000	±1000	nA
			V_{INH} = V_{IH} *(Figure 2)*							
I_{IZ}	Maximum Switch "ON" Leakage Current	HC4051	V_{IS} = V_{CC} to V_{EE}	GND	6.0V		±0.2	±2.0	±2.0	μA
			V_{INH} = V_{IL}	−6.0V	6.0V		±0.4	±4.0	±4.0	μA
			(Figure 3)							
		HC4052	V_{IS} = V_{CC} to V_{EE}	GND	6.0V		±0.1	±1.0	±1.0	μA
			V_{INH} = V_{IL}	−6.0V	6.0V		±0.2	±2.0	±2.0	μA
			(Figure 3)							
		HC4053	V_{IS} = V_{CC} to V_{EE}	GND	6.0V		±0.1	±1.0	±1.0	μA
			V_{INH} = V_{IL}	−6.0V	6.0V		±0.1	±1.0	±1.0	μA
			(Figure 3)							

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits			
I_{IZ}	Maximum Switch "OFF" Leakage Current (Common Pin)	HC4051	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V		±0.2 ±0.4	±2.0 ±4.0	±2.0 ±4.0	μA μA
		HC4052	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V		±0.1 ±0.2	±1.0 ±2.0	±1.0 ±2.0	μA μA
		HC4053	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V		±0.1 ±0.1	±1.0 ±1.0	±1.0 ±1.0	μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages ($V_{CC}-V_{EE}$) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

Note 6: Adjust 0 dB for f = 1 kHz (Null R1/R_{ON} Attenuation).

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 2.0V-6.0V$, $V_{EE} = 0V-6V$, $C_L = 50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions		V_{EE}	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out			GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	25 5 4 3	60 12 8 7	75 15 12 11	90 18 14 13	ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L = 1$ kΩ		GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	92 16 15	355 69 46 41	435 87 58 51	515 103 69 62	ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay			GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	65 28 18 16	290 58 37 32	365 73 46 41	435 87 56 48	ns ns ns ns
f_{MAX}	Minimum Switch Frequency Response 20 log (V_I/V_O) = 3 dB			GND −4.5V	4.5V 4.5V	30 35				MHz MHz
	Control to Switch Feedthrough Noise	$R_L = 600\Omega$, f = 1 MHz, $C_L = 50$ pF	V_{IS} = 4 V_{PP} V_{IS} = 8 V_{PP}	0V −4.5V	4.5V 4.5V	1080 250				mV mV
	Crosstalk between any Two Switches	$R_L = 600\Omega$, f = 1 MHz	V_{IS} = 4 V_{PP} V_{IS} = 8 V_{PP}	0V −4.5V	4.5 4.5V	−52 −50				dB dB
	Switch OFF Signal Feedthrough Isolation	$R_L = 600\Omega$, f = 1 MHz, $V_{CTL} = V_{IL}$	V_{IS} = 4 V_{PP} V_{IS} = 8 V_{PP}	0V −4.5V	4.5V 4.5V	−42 −44				dB dB
THD	Sinewave Harmonic Distortion	$R_L = 10$ kΩ, $C_L = 50$ pF, f = 1 kHz	V_{IS} = 4 V_{PP} V_{IS} = 8 V_{PP}	0V −4.5V	4.5V 4.5V	0.013 0.008				% %

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input 4051 Common 4052 Common 4053 Common			15 90 45 30				pF
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms

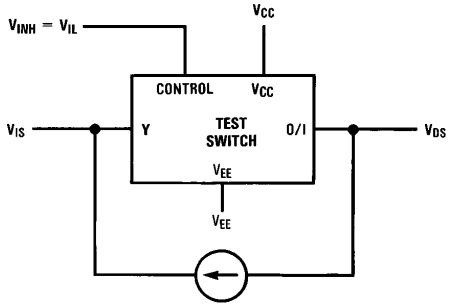

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FIGURE 1. "ON" Resistance

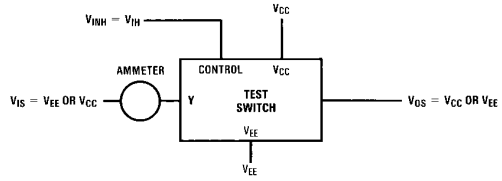

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FIGURE 2. "OFF" Channel Leakage Current

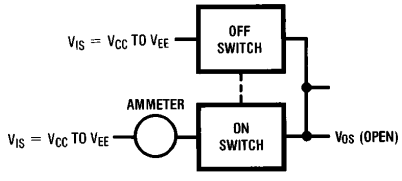

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FIGURE 3. "ON" Channel Leakage Current

AC Test Circuits and Switching Time Waveforms (Continued)

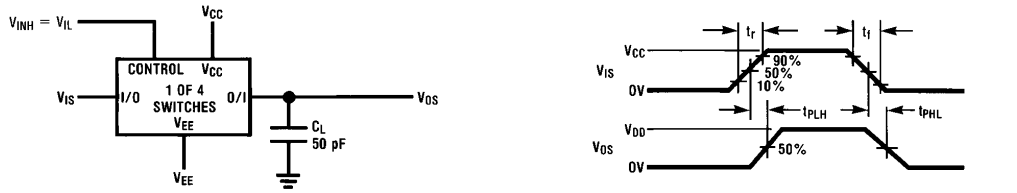

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FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

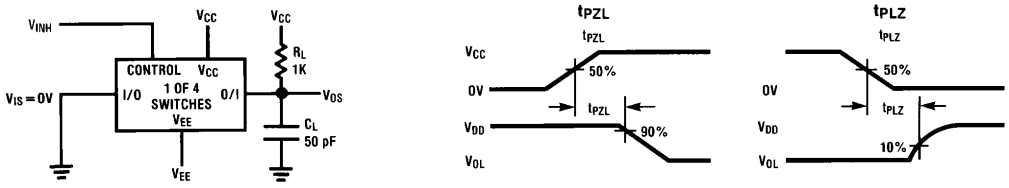

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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

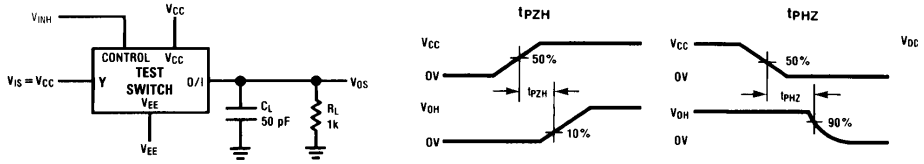

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FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay TIme Control to Signal Output

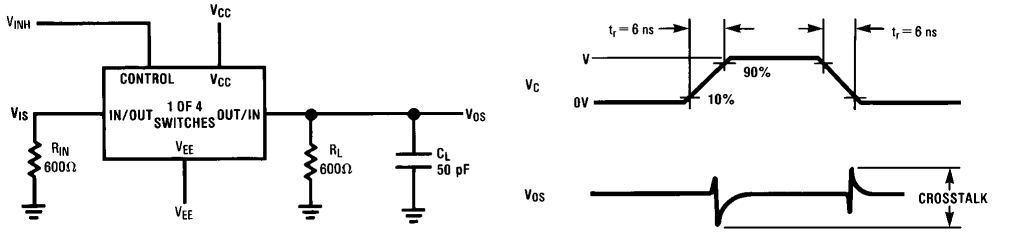

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FIGURE 7. Crosstalk: Control Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

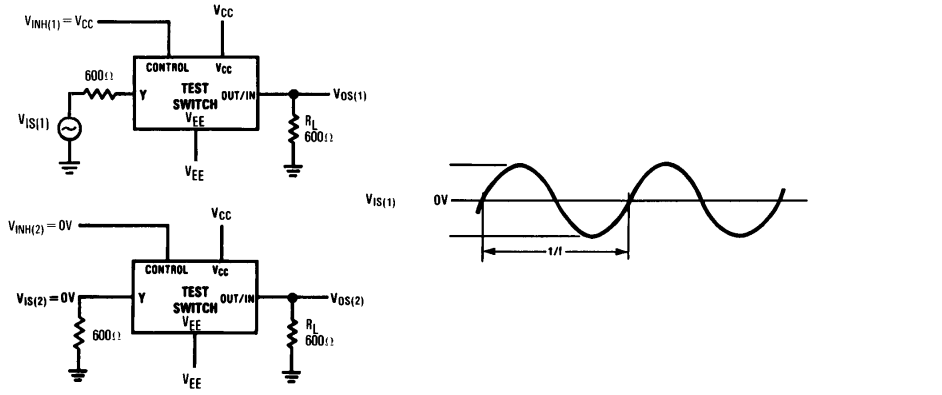

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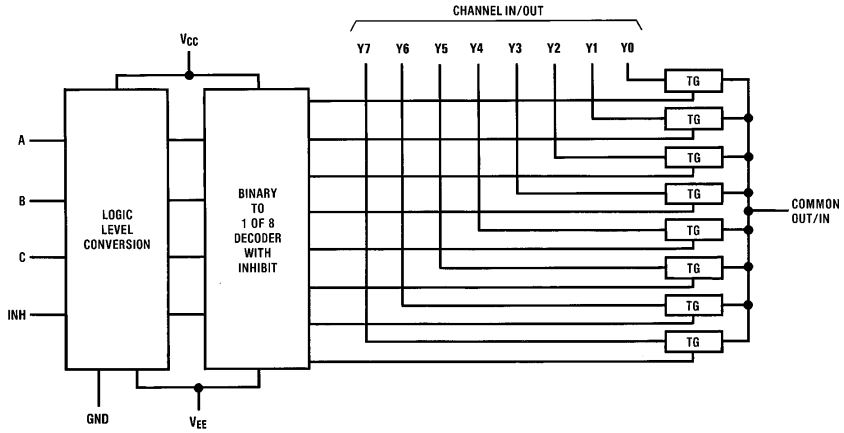
FIGURE 8. Crosstalk Between Any Two Switches

Logic Diagrams

MM54HC4051/MM74HC4051



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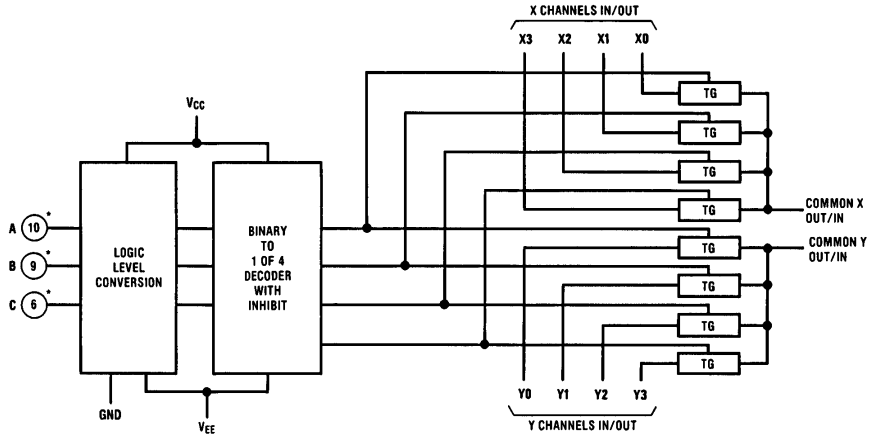
MM54HC4052/MM74HC4052



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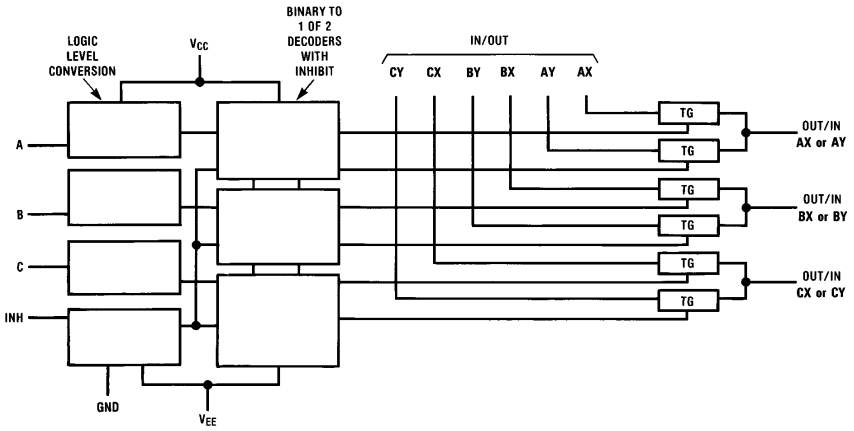
Logic Diagrams (Continued)

MM54HC4053/MM74HC4053



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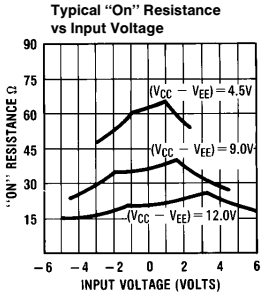
Typical Performance Characteristics



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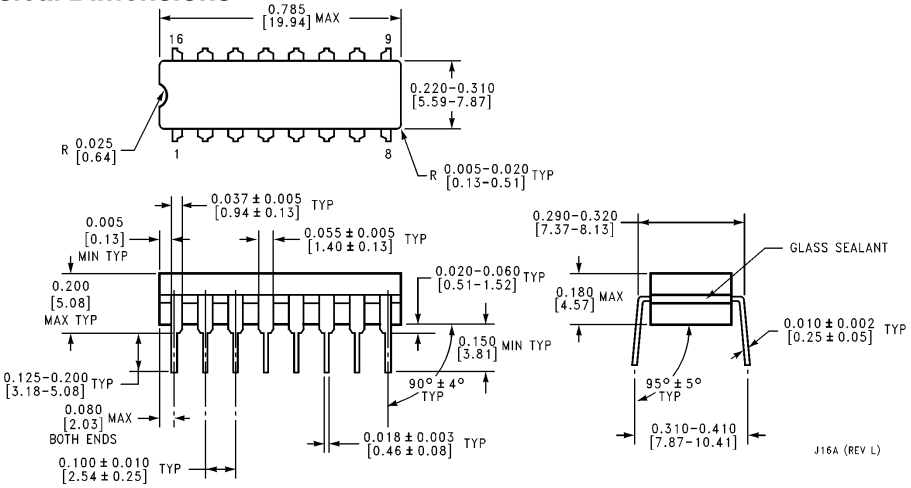
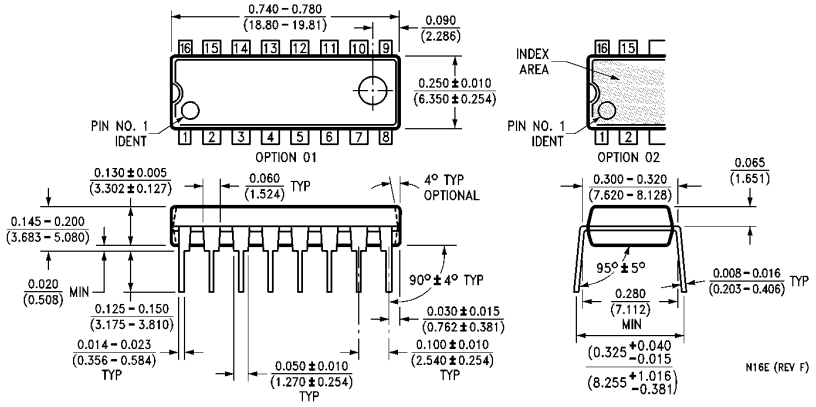
Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch pins, the voltage drop across the switch must not exceed 1.2V (calculated from the ON resistance).

Physical Dimensions



Order Number MM54HC4051J, MM54HC4052J, MM54HC4053J, MM74HC4051J, MM74HC4052J, or MM74HC4053J
NS Package J16A



Order Number MM74HC4051N, MM74HC4052N, or MM74HC4053N
NS Package N16E

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