

## **N76E003 BSP Guide**

Directory Introduction for Nuvoton 8051 Family

### **Directory Information**

Please extract the “N76E003\_BSP\_Keil\_C51\_V1.0.2.zip” file firstly, and confirm the following folder all contain.

This BSP folder contents:

<b>Document</b>	Driver reference manual and reversion history.
<b>Common</b>	The common usual subroutine include Timer delay and basic UART baud rate setting
<b>Include</b>	All include header file and define
<b>Sample_Code</b>	Driver sample code.
<b>Startup</b>	Startup file for N76E003

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## 1 .\Document\

Nuvoton\_N76E003\_BSP\_Revision\_History.pdf

This document shows the revision history of N76E003 BSP.

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## 2 \Common

<b>Common.c</b>	UART0 Baud rate setting base on Time 1 or Timer 3, UART1 baud rate setting base on Timer 3
<b>Delay.c</b>	Timer0_Delay100us, Timer0_Delay1ms, Timer1_Delay10ms, Timer2_Delay500us, Timer3_Delay100ms setting

### 3 \Include

<b>Common.h</b>	Header file to extern function for Common.c
<b>Delay.h</b>	Header file of extern function for Delay.c
<b>Function_Define.h</b>	Function setting include GPIO initial, External pin interrupt trig mode, Timer value common value define, Timer 2 capture enable, PWM initial, ADC initial
<b>N76E003.h</b>	N76E003 SFR define header file
<b>SFR_Macro.h</b>	Extend N76E003 define for no-bit-addressable SFR with bit enable or disable function.

## 4 \Sample\_Code

<b>ADC_Bandgap</b>	ADC band-gap input demo code
<b>ADC_Bandgap_VDD</b>	ADC converts demo code with band-gap value to calculate the VDD value. Add 5 times average value test and add delay 20ms in each sampling.
<b>ADC_IO_Trig</b>	ADC trig start polling or interrupt by special I/O
<b>ADC_Optimizing_16x</b>	ADC convert 16 times average value to get an optimized value of the ADC convert result
<b>ADC_PWM_Trig</b>	ADC trig start by PWM cycle finish
<b>ADC_Simple</b>	ADC trig start polling or interrupt by SFR start bit
<b>Clock_Out</b>	N76E003 HIRC clock out setting
<b>Fsys_Select</b>	System clock select demo
<b>GPIO</b>	All GPIO quasi / push pull/ input only/ open drain four status initial setting and toggle out
<b>I2C_EEPROM</b>	I <sup>2</sup> C module connect with external EEPROM read writer demo
<b>I2C_Master-Slave</b>	Two piece of N76E003 I <sup>2</sup> C module connect, the master and slave demo code
<b>IAP_AP-program-AP_Dataflash</b>	IAP run in APROM to program APROM demo code, It's also used as program data flash area.
<b>IAP_Dataflash_EEPROM</b>	Customer use this macro, each time call this subroutine, can use Data flash as EEPROM mode, the process include read old data / erase / modify new code/ write in.
<b>IAP_LD-Program-AP</b>	IAP run in LDROM to program APROM. This function is use in ISP function.
<b>IAP_ModifyHIRC</b>	The function to modify HIRC value to 16.6MHz for UART baud rate over 38400 application system.
<b>IAP_program_Config</b>	Use code IAP function to modify CONFIG area.
<b>IAP_Read_Bandgap</b>	Use IAP command to read actually band-gap value for each

	N76E003.
<b>IAP_Read_UID</b>	Use IAP command to read the UID of each N76E003.
<b>IAP_Read_UCID</b>	Use IAP command to read the UCID of each N76E003.
<b>Pin_Interrupt</b>	Each GPIO of N76E003 can use as external interrupt pin. Trig IC wakeup from idle / power down mode.
<b>PWM_DeadTime</b>	PWM output with dead time insert initial setting
<b>PWM_INT</b>	PWM output with interrupt subroutine
<b>PWM_Simple</b>	Simple PWM output setting initial
<b>SPI_Flash</b>	Read / writer W25Q16 sample code.
<b>SPI_Master-Slave</b>	SPI connect with two N76E003, Include master and slave sample code, use interrupt and polling.
<b>Timer01_mode_0</b>	Timer 0 and Timer 1 mode 0 demo code
<b>Timer01_mode_1</b>	Timer 0 and Timer 1 mode 1 demo code
<b>Timer01_mode_2</b>	Timer 0 and Timer 1 mode 2 demo code
<b>Timer01_mode_3</b>	Timer 0 and Timer 1 mode 3 demo code
<b>Timer2_AutoReload_Capture</b>	Timer 2 capture with compare function demo code
<b>Timer2_AutoReload_Delay</b>	Timer 2 auto reload mode for delay function demo code
<b>Timer3</b>	Timer 3 delay counter demo code
<b>UART0</b>	UART0 demo code
<b>UART0_mode_3</b>	UART0 mode 3 with TB8/RB8 function
<b>UART1</b>	UART1 demo code
<b>WakeupTimer_INT</b>	Wakeup timer with interrupt subroutine demo code
<b>Watchdog_INT</b>	Watch dog without reset, only interrupt function initial
<b>Watchdog_Reset</b>	Watch dog reset MCU function setting initial
<b>xRAM_768B</b>	XRAM 768 bit test, assembler and c code compiler in one

project demo

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## 5 REVISION HISTORY

Date	Revision	Description
2016.12.28	1.00	Initially issued.
2017.2.1	1.01	<ol style="list-style-type: none"> <li>1. Add HIRC modify</li> <li>2. Add SPI master / slave control demo code include interrupt and polling</li> </ol>
2017.6.20	1.02	<ol style="list-style-type: none"> <li>1. Add POR disable instruction in startup.a51</li> <li>2. Add ADC read band-gap and calculate VDD value demo</li> <li>3. Add ADC 16 times optimize demo</li> <li>4. Add read UCID sample code</li> </ol>
2017.9.26	1.03	<ol style="list-style-type: none"> <li>1. Modify ADC read band-gap and calculate VDD value demo</li> </ol>

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