ARM Cortex®-M0

32-BIT MICROCONTROLLER

NM18101 Series Product Brief

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1 GENERAL DESCRIPTION

The NM1810 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and monolithic half-bridge gate driver for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The MCU of NM18101 series can run up to 48 MHz and offers 29.5K-bytes embedded program flash, size configurable Data Flash (shared with program flash), 2K-byte flash for the ISP, 1.5K-byte SPROM for security, and 4K-byte SRAM. Plentiful system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM18101 series in order to reduce component count, board space and system cost. These useful functions make the NM18101 series powerful for a wide range of motor driver applications.

The power supply input of NM18101 is up to 30V. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component.

Additionally, the NM18101 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Operation Supply Voltage VIN Range from 4.5 to 30V
  - Gate Driver (half-bridge gate drive)
  - Programmable enable/disable gate driver by MCU I/O of PC.4
  - 3 low-side and 3 high-side gate drivers
  - More than 0.6A gate driving capability
  - UVLO(Under voltage lockout=4.1V) function to disable PWM output (PWM output low)
  - Embedded 2 Internal 5V voltage regulators with 35mA driving capability for MCU and Gate driver.
  - Matched propagation delay of around 500ns for both PWM complementary channels
  - PWM output delay matching < 50 ns
  - Max V_{GS} of Power MOS is up to 10V
  - Thermal shutdown circuitry to limit the junction temperature at 160 ℃
- MCU Core
  - ARM® Cortex™-M0 core running up to 48 MHz
  - One 24-bit system tick timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Memory
  - 29.5KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2KB Flash memory for loader (LDROM)
  - Three 0.5KB Flash memory for security protection (SPROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)

- 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up

- I/O Port
  - Up to 14 general-purpose I/O (GPIO) pins and 1 input only pin
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - GPIO built-in Pull-up/Pull-low resistor for selection
  - The input only pin with high voltage capability upto VIN voltage
- Timer
  - Provides two Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides four operation modes: One-shot, Periodic, Toggle and Continuous
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
- Continuous Capture
  - Timer0, Timer1 and Systick support Continuous Capture function which can continuously capture 4 edges on one signal
- Enhanced Input Capture
  - One 24-bit input capture up-counter with multi-capture triggered sources.
  - Capture surce:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - Outputs of ACMP0 and ACMP1
    - ADC compare result
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- PWM

- Support a built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
- Supports group/synchronous/independent/ complementary modes
- Supports One-shot PWM function
- Supports Edge-aligned and Center-aligned PWM type
- Support Asymmetric mode
- Programmable dead-zone insertion between complementary channels
- Each output has independent polarity setting control
- Supports hardware fault brake and software brake protections
- Supports rising, falling, central, period, and fault break interrupts
- Supports duty/period trigger ADC conversion
- Auto phase change triggered by timer comparing matching event
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function
- Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - Supports to configure as UART, SPI, I²C, or LIN individually
  - Supports programmable baud-rate generator
- 12-bit ADC (Analog-to-Digital Converter)
  - 1us conversion time at minimum
  - Supports 2 sample/hold
  - Up to 8-ch single-end input from I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Support temperature sensor for measurement chip temperature
  - Support Simultaneous and Sequential function to continuous conversion 4 channels maximum.
- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13.

- Unity gain frequency up to 8MHz

- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: Digital IO: EFT > ± 3.5KV, ESD HBM pass 4KV; Power IO: ESD 2KV
- Packages:
  - Green package (RoHS)
  - 33-pin, QFN, 5mm x 5mm

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NM18100 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48 MHz*	BOD	PWM	Analog Comp.	PGA	ADC (12-Bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI											
							UART*	I^2C	SPI									
NM18101ZCAE	29.5	4	2	√	14	3	2	2	1/1	1	1	6	2	1	8x 12bit	1	√	QFN 33

Table 3.1-1 NM18100 Base Series Selection Guide

3.2 Pin Configuration

3.2.1 NM18101ZCAE Series QFN 33-Pin Diagram

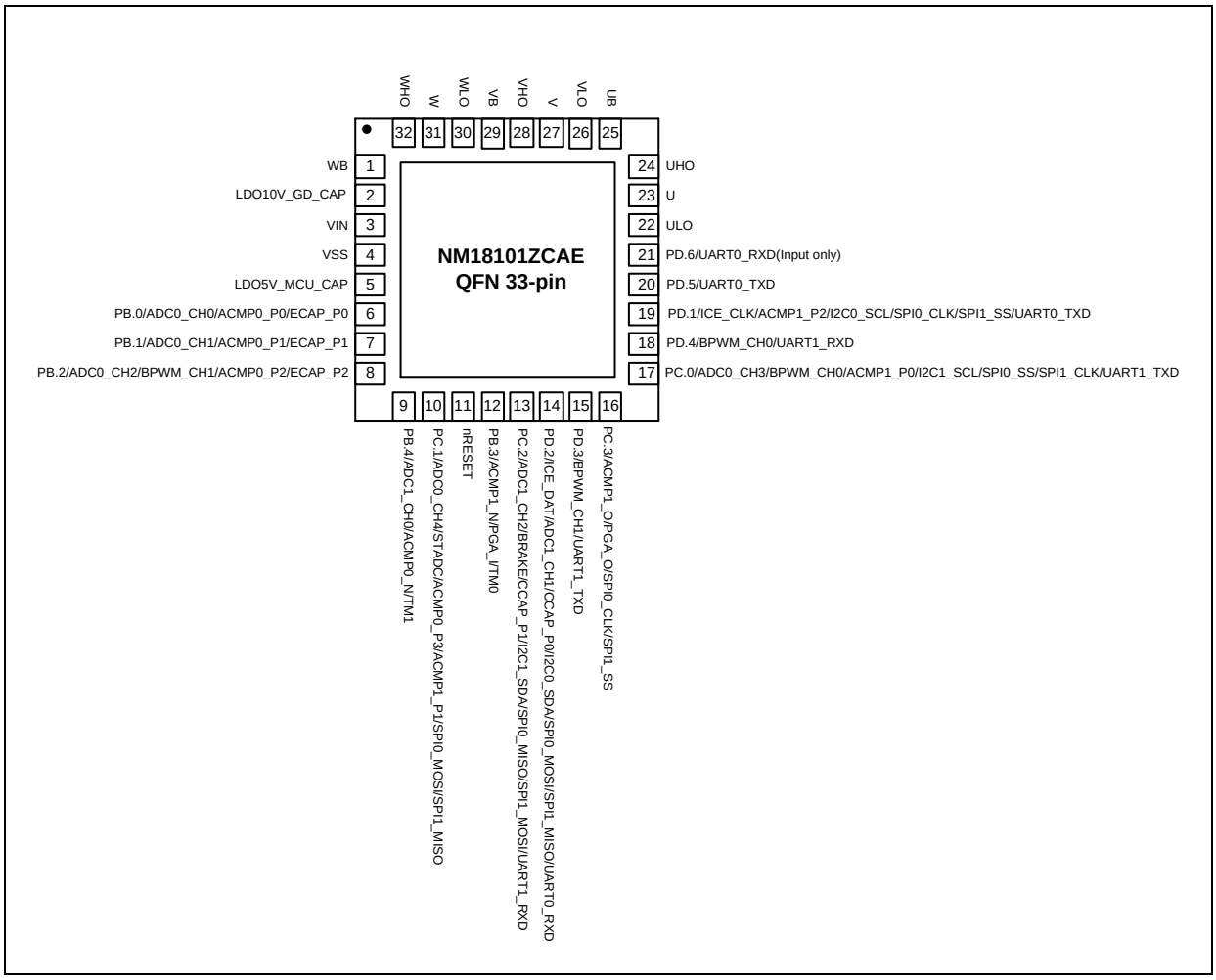


Figure 3.2-1 NM18101ZCAE QFN 33-pin Diagram

3.3 Pin Description

3.3.1 NM18101ZCAE Series QFN 33-Pin Description

Pin Number QFN 5x5 32-pin	Pin Name	Pin Type	Description
1	WB	HP	W-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and W.
2	LDO10V_GD_CAP	P	10V LDO OUT for gate driver. Recommend connect an at least 4.7uF capacitor to GND.
3	VIN	HP	Power supply for internal control circuit. Recommend connect a capacitor to GND to stable the input power.
4	VSS	P	Ground pin for digital circuit
5	LDO5V_MCU_CAP	P	5V LDO OUT for MCU. Recommend connect a 1uF capacitor to GND.
6	PB.0	I/O	General purpose digital I/O pin.
	ADC0_CH0	A	ADC0 analog input channel 0.
	ACMP0_P0	A	Comparator0 positive input pin.
	ECAP_P0	I	Input capture channel 0
7	PB.1	I/O	General purpose digital I/O pin.
	ADC0_CH1	A	ADC0 analog input channel 1.
	ACMP0_P1	A	Comparator0 positive input pin.
	ECAP_P1	I	Input capture channel 1
8	PB.2	I/O	General purpose digital I/O pin.
	ADC0_CH2	A	ADC0 analog input channel 2.
	BPWM_CH1	O	Basic PWM channel 1 output
	ACMP0_P2	A	Comparator0 positive input pin.
	ECAP_P2	I	Input capture channel 2
9	PB.4	I/O	General purpose digital I/O pin.
	ADC1_CH0	A	ADC1 analog input channel 0.
	ACMP0_N	A	Comparator0 negative input pin.
	TM1	I	Timer1 event counter input / toggle output
10	PC.1	I/O	General purpose digital I/O pin.
	ADC0_CH4	A	ADC0 analog input channel 4.
	STADC	I	External ADC trigger input pin.

	ACMP0_P3	**A**	Comparator0 positive input pin.
	ACMP1_P1	**A**	Comparator1 positive input pin.
	SPI0_MOSI	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	**I/O**	SPI1 MISO (Master In, Slave Out) pin.
11	**nRESET**	**I**	External reset pin, internal pull-high.
12	**PB.3**	**I/O**	General purpose digital I/O pin.
	ACMP1_N	**A**	Comparator1 negative input pin.
	PGA_I	**A**	PGA analog input pin.
	TM0	**I**	Timer0 event counter input / toggle output
13	**PC.2**	**I/O**	General purpose digital I/O pin.
	ADC1_CH2	**A**	ADC1 channel2 analog input.
	BRAKE	**I**	Brake input pin of EPWM.
	CCAP_P1	**I**	Timer Continuous Capture input pin
	I2C1_SDA	**I/O**	I2C1 data input/output pin.
	SPI0_MISO	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	**I/O**	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	**I**	Data receiver input pin for UART1.
14	**PD.2**	**I/O**	General purpose digital I/O pin.
	ICE_DAT	**I/O**	Serial wired debugger data pin
	ADC1_CH1	**A**	ADC1 analog input channel 1.
	CCAP_P0	**I**	Continuous Capture Input
	I2C0_SDA	**I/O**	I2C0 data pin.
	SPI0_MOSI	**I/O**	SPI0 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	**I/O**	SPI1 MISO (Master In, Slave Out) pin
	UART0_RXD	**I**	UART0 data receiver input pin.
15	**PD.3**	**I/O**	General purpose digital I/O pin.
	BPWM_CH1	**I/O**	PWM channel1 output/capture input.
	UART1_TXD	**O**	Data transmitter output pin for UART1.
16	**PC.3**	**I/O**	General purpose digital I/O pin.
	ACMP1_O	**O**	Analog comparator1 output
	PGA_O	**A**	PGA output pin

	SPI0_CLK	**I/O**	SPI0 clock pin.
	SPI1_SS	**I/O**	SPI1 Slave Select
17	**PC.0**	**I/O**	General purpose digital I/O pin.
	ADC0_CH3	**A**	ADC0 analog input channel 3.
	BPWM_CH0	**O**	Basic PWM channel 0 output
	ACMP1_P0	**A**	Comparator1 positive input pin.
	I2C1_SCL	**I/O**	I2C1 clock pin.
	SPI0_SS	**I**	SPI0 slave selection pin.
	SPI1_CLK	**I/O**	SPI1 clock pin.
	UART1_TXD	**O**	UART1 data transmitter output pin.
18	**PD.4**	**I/O**	General purpose digital I/O pin.
	BPWM_CH0	**I/O**	PWM chanel0 output/capture input.
	UART1_RXD	**I**	Data receiver input pin for UART1
19	**PD.1**	**I/O**	General purpose digital I/O pin.
	ICE_CLK	**I**	Serial wired debugger clock pin
	ACMP1_P2	**A**	Analog comparator1 positive input pin
	I2C0_SCL	**I/O**	I2C0 clock pin
	SPI0_CLK	**I/O**	SPI0 serial clock pin
	SPI1_SS	**I/O**	SPI1 slave select pin
	UART0_TXD	**O**	Data transmitter output pin for UART0
20	**PD.5**	**I/O**	General purpose digital I/O pin.
	UART0_TXD	**O**	Data transmitter output pin for UART0
21	**PD.6**	**I**	General purpose digital input pin[3]
	UART0_RXD	**I**	Data receiver input pin for UART0
22	**ULO**	**HO**	Output for U-phase low-side MOSFET. Connect to U-phase low-side MOSFET gate.
23	**U**	**HI**	U-Phase input. It should be connected to U-phase high-side MOSFET source and low-side FET drain.
24	**UHO**	**HO**	Output for U-phase high-side MOSFET. Connect to U-phase high-side MOSFET gate.
25	**UB**	**HP**	U-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and U.
26	**VLO**	**HO**	Output for V-phase low-side MOSFET. Connect to V-phase low-side MOSFET gate.
27	**V**	**HI**	V-Phase input. It should be connected to V-phase high-side MOSFET source and low-side FET drain
28	**VHO**	**HO**	Output for V-phase high-side MOSFET. Connect to V-phase high-side MOSFET gate.
29	**VB**	**HP**	V-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and V.
30	**WLO**	**HO**	Output for W-phase low-side MOSFET. Connect to W-phase low-side MOSFET gate.

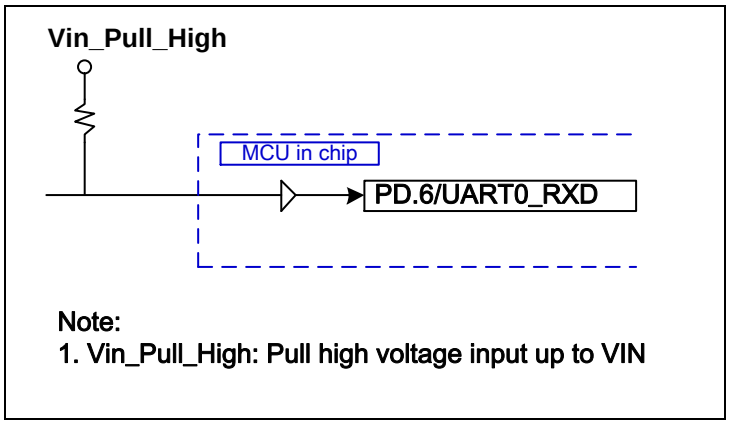
31	**W**	**HI**	W-Phase input. It should be connected to high-side MOSFET source and low-side FET drain.
32	**WHO**	**HO**	Output for W-phase high-side MOSFET. Connect to W-phase high-side MOSFET gate.
33	**VSS**	**P**	Ground pin for digital circuit

Table 3.3-1 QFN33 Pin Description

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

[3] Input only with the following pull high capability.



4 BLOCK DIAGRAM

4.1 NM18101 Block Diagram

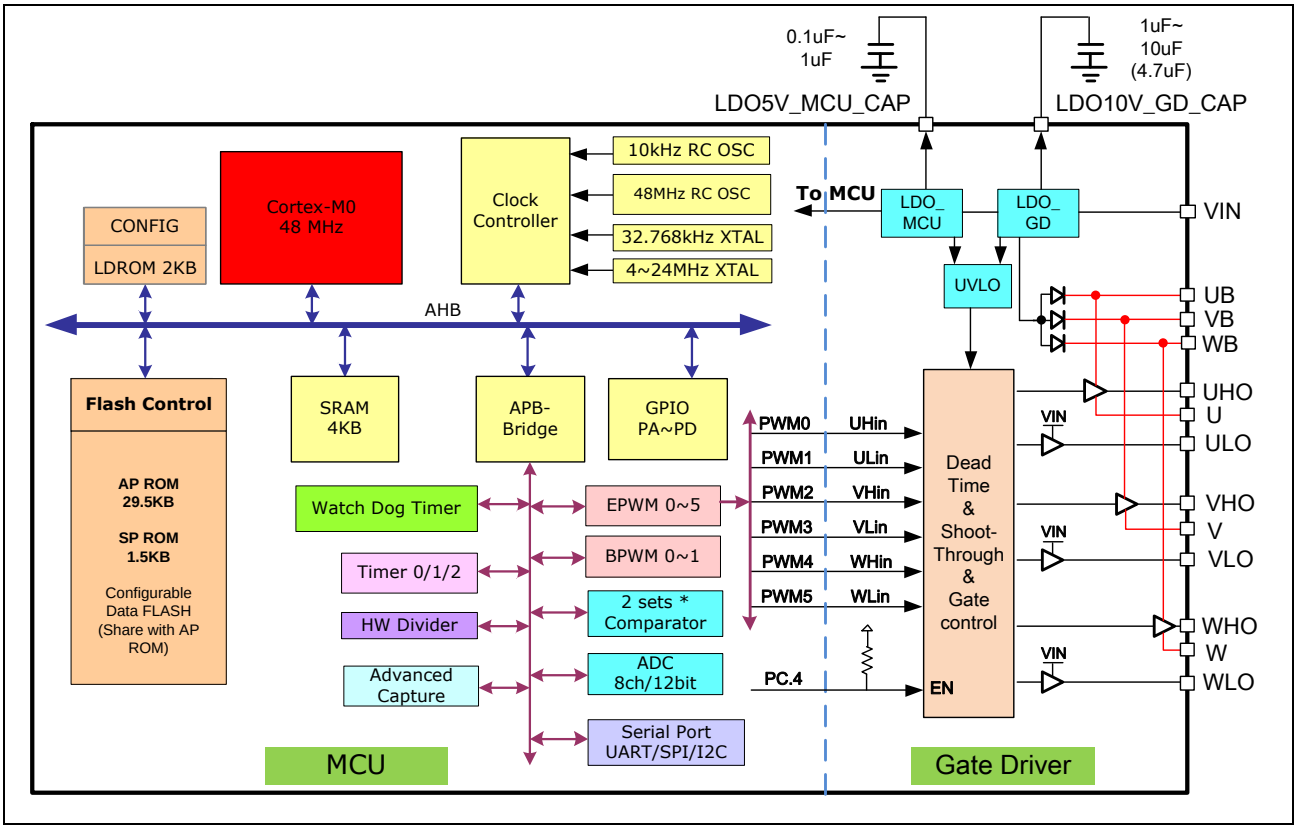


Figure 4.1-1 NM18101 Series Block Diagram

5 NM18101 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
VIN Power Supply		-0.3	40	V
Low voltage I/O pins		-0.3	LDO5V+0.3	V
High voltage I/O pins		-0.3	40	V
Oscillator Frequency		4	24	MHz
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}		-	120	mA
Maximum Current sunk by an low voltage I/O pin		-	35	mA
Maximum Current sourced by an low voltage I/O pin		-	35	mA
Maximum Current sunk by total low voltage I/O pins		-	100	mA
Maximum Current sourced by total low voltage I/O pins		-	100	mA
Supply Output Pulse Current (10ms)			2.5	A
Thermal Resistance, θ_{JA}			40	℃/W
Thermal Resistance, θ_{JC}			10	℃/W
Operating Temperature		-40	105	℃
Storage Temperature		-55	150	℃
ESD Protection	Human Body Mode		4	KV
	Machine Mode		200	V
	Latch-up		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 DC Electrical Characteristics

5.2.1 DC Electrical Characteristic for MCU

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Input power voltage of MCU	2.5	-	LDO5V+0.3	V	V_{DD} = 2.5V ~ 5.5V up to 48 MHz
V_{DD}	Input power voltage of MCU	-0.3	-	-	V	
I_{DD1}	MCU Operating Current Normal Run Mode HCLK = 48MHz while(1){} Executed from Flash	-	17	-	mA	V_{DD} = 5.5V; Internal RC48M = Enable; All digital modules = Enabled
I_{IDLE1}	Operating Current Idle Mode HCLK = 48MHz		10		mA	VDD = 5.5V, PLL on, All digital module on
			5		mA	VDD = 5.5V, PLL on, All digital module off
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)		4.0		μA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{LK}	I/O Input Leakage Current	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD} Open-drain or input only mode
V_{IL1}	I/O Input Low Voltage (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	I/O Input High Voltage (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRST	-0.3	-	0.3 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRST	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRST Pin Pull-up Resistor	17.5		150	kΩ	V_{DD} = 2.1 V ~ 5.5V
T_{SD}	Thermal Shutdown Temperature		165		℃	Thermal Protection
T_{SDHYS}	Thermal Shutdown Hysteresis		50		℃	Thermal Protection

Notes:

1. Pins of PA, PB, PC and PD can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when pin voltage approximates to 2V.

5.2.2 DC Electrical Characteristic for Gate Driver

(-40℃ < TJ < 85℃, and recommended supply voltage unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage						
VIN	Vpower		6		30	V
VIN Under Voltage Lockout	UVLO	VIN Falling			4.1	V
V IN Under Voltage Hysteresis				0.4		V
VIN standby current		At VIN < 4.1V		10		uA
Gate Driver Output (NM18101ZCAE)						
PWM input to output delay	T_{I2O}			500		ns
PWM output matching	T_{MATCH}			50		ns
PWM output low to high	I_{PWM_HI}	At VIN=8V	0.2			A
PWM output high to low	I_{PWM_LO}	At VIN=8V	0.4			A
Internal 10V regulator (LDO10V_GD_CAP)						
Output Current	I_{OUT}	At VIN>12V		35		mA
SLEEP Current	I_{STB}	At VIN < 4.1V		1		mA
Operation Voltage	VLDO	At VIN>12V	-5%	10	+5%	V
LDO dropped volt	V_{DROP}	From VIN to LDO10V output		1		V
Thermal Protection						
Thermal Shutdown Temperature	TSD			165		℃
Thermal Shutdown Hysteresis	TSDHYS			50		℃
Thermal Warning Temperature	TWRN			130		℃

5.3 AC Electrical Characteristics

5.3.1 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
			2%		%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	1090	-	μA	T_A = 25 ℃,V_{DD} = 5 V

5.3.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	
	Oscillator Frequency	-50	-	+50	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃

5.3.3 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	47		μA	V_{DD}=5.5V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	225	-	ns	
V_{HYS}	Hysteresis	-	10	-	mV	ACMPPHYSEN = 01
V_{HYS}	Hysteresis	-	90	-	mV	ACMPPHYSEN = 10
T_{STB}	Stable time	-	1.06	-	μs	

Notes:
Guaranteed by design, not test in production.

5.3.4 PGA(Porgramable Gain Amplifier)

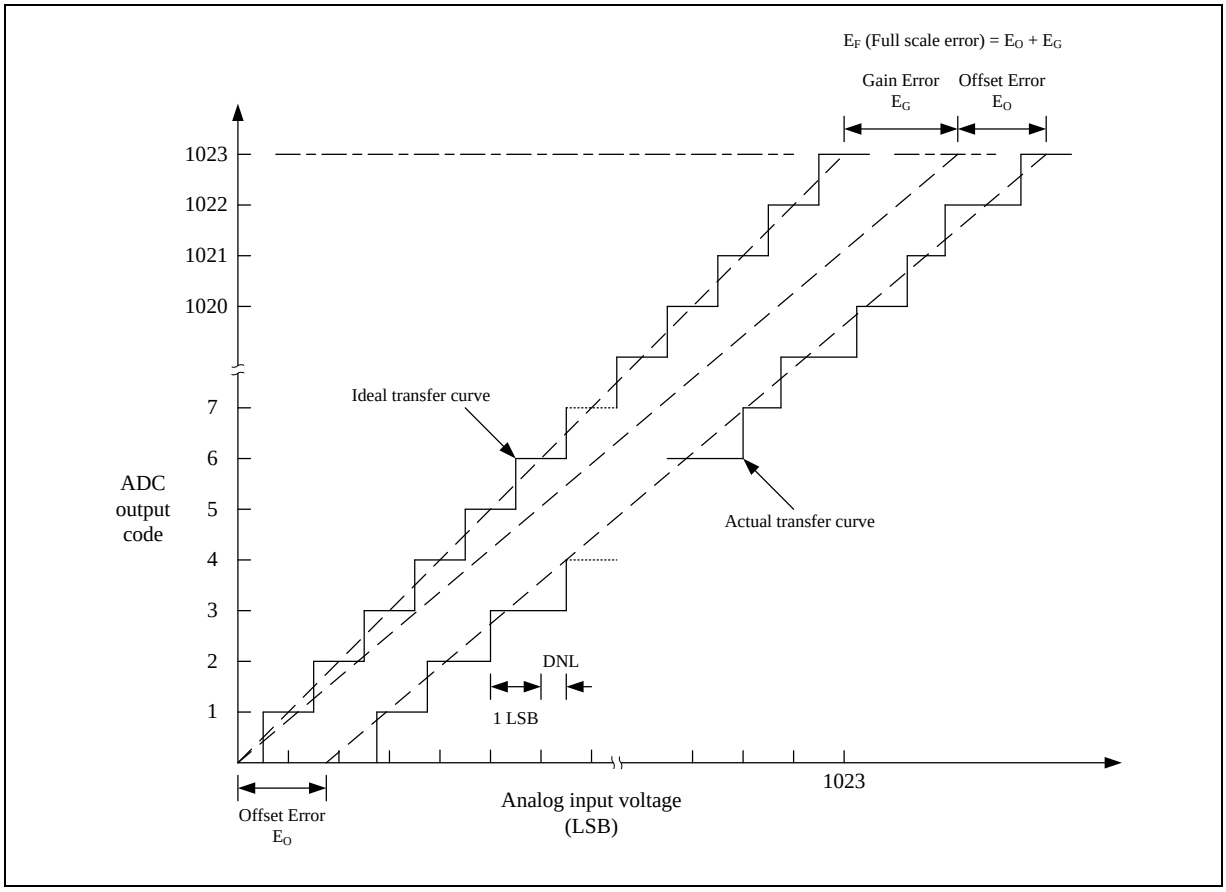
Parameter	Min	Typ	Max	Unit	Test Condition
Operation voltage range	2.5	3.3	5.5	V	
Operating Current			5	mA	V_{DD} = 5V, T=125℃
Operating Temperature	-40	25	125	℃	
Input Offset with calibration Type corner, temp=25,V_{CM}=AV_{DD}/2			+2	mV	
Input Offset Average Drift			1	uV/℃	
Output Swing	0.1		V_{DD} - 0.1	V	
PGA gain accuracy	-1		+1	%	
Input Common Mode Range	0		V_{DD} - 1.5	V	
DC Gain	50	80		dB	
Unity Gain Frequency	7		8.2	MHz	V_{DD} = 5V
Phase Margin	50°			°	
PSRR+	49	90		dB	V_{DD} = 5V
CMRR	69	90		dB	V_{DD} = 5V
Slew Rate+		6.0	7.5	V/us	V_{DD} = 5 V, R_{Load}=1.3K, C_{Load}=100p
Wake Up Time			20	us	

Note: Guaranteed by design, not test in production

5.3.5 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±2	-	LSB	V_{DD} = 5.5V
INL	Integral Nonlinearity Error	-	±1	-	LSB	V_{DD} = 5.5V
E_O	Offset Error	-	-0.33	-	LSB	V_{DD} = 5.5V
E_G	Gain Error (Transfer Gain)	-	0.33	-	LSB	V_{DD} = 5.5V
E_A	Absolute Error	-	-2.62	-	LSB	V_{DD} = 5.5V
	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	12	16	MHz	V_{DD} = 3.0~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0~5.5 V N: sampling clock N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time	-	1000	1050	ns	V_{DD} = 3.0~5.5 V
V_{DD}	Supply Voltage	3.0	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	1.6	-	pF	-
R_{IN}	Input Load	-	2.5	-	kΩ	-

Note: ADC voltage reference is same with V_{DD}


E_F (Full scale error) = E_O + E_G
Gain Error E_G
Offset Error E_O
1023
1022
1021
1020
7
6
5
4
3
2
1
ADC output code
Ideal transfer curve
Actual transfer curve
DNL
1 LSB
1023
Offset Error E_O
Analog input voltage (LSB)

5.3.6 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage		1.25		V	-

5.3.7 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	100	-	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Hysteresis	4.33	4.3	4.39	V	BOV_VL [2:0] = 3
		4.03	4.0	4.10	V	BOV_VL [2:0] = 2
		3.73	3.7	3.79	V	BOV_VL [2:0] = 7
		3.02	3.0	3.09	V	BOV_VL [2:0] = 1
		2.72	2.7	2.79	V	BOV_VL [2:0] = 6
		2.42	2.4	2.49	V	BOV_VL [2:0] = 0
		2.22	2.2	2.30	V	BOV_VL [2:0] = 5
		2.02	2.0	2.09	V	BOV_VL [2:0] = 4
V_{BOD}	Brown-out Detector		4.3		V	BOV_VL [2:0] = 3
			4.0		V	BOV_VL [2:0] = 2
			3.7		V	BOV_VL [2:0] = 7
			3.0		V	BOV_VL [2:0] = 1
			2.7		V	BOV_VL [2:0] = 6
			2.4		V	BOV_VL [2:0] = 0
			2.2		V	BOV_VL [2:0] = 5
			2.0		V	BOV_VL [2:0] = 4

5.3.8 Flash DC Electrical Characteristics

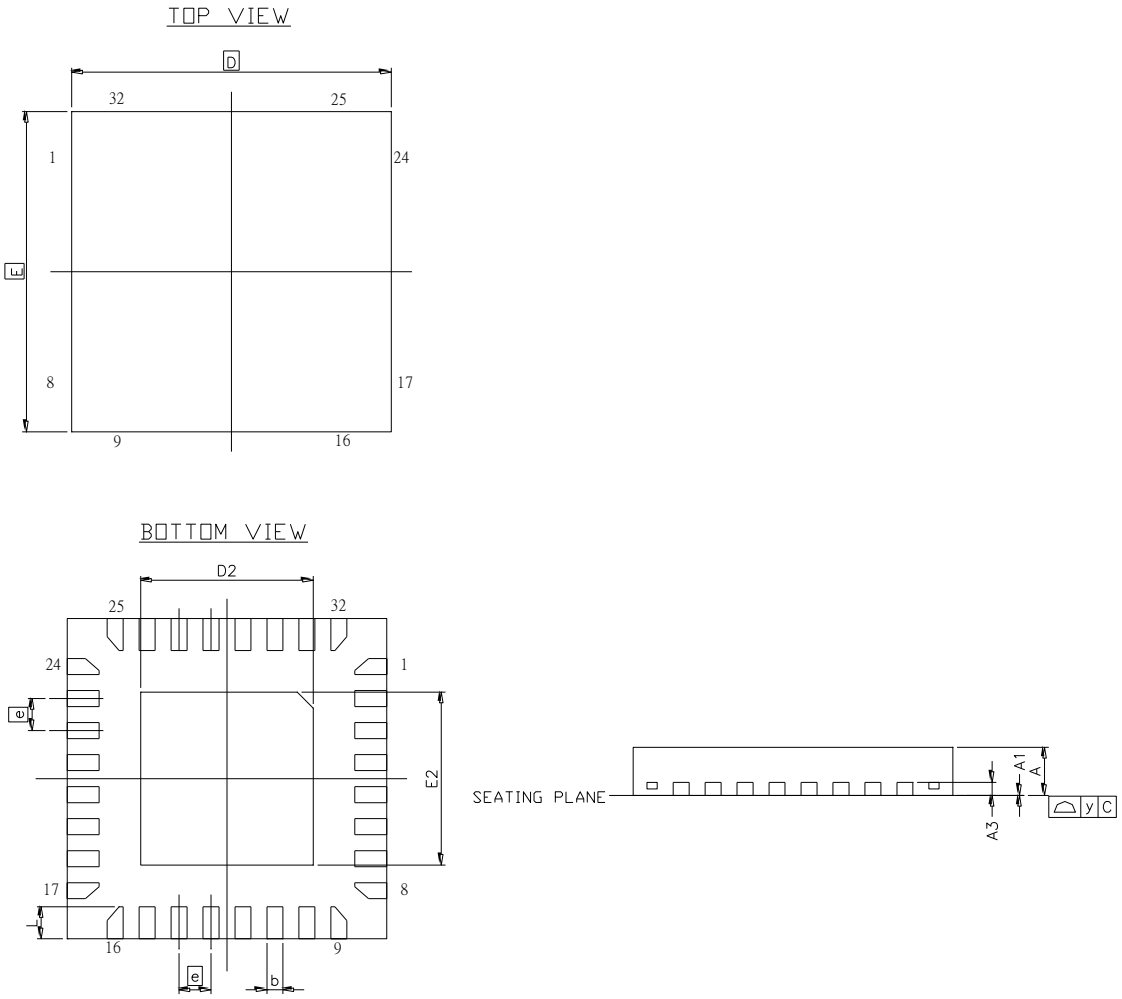
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	-	-	20,000	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A = 85℃
T_{ERASE}	Sector Erase Time	-	6	-	ms	
T_{PROG}	Program Time	-	7.5	-	us	
I_{DD1}	Read Current	-	4	-	mA	
I_{DD2}	Program Current	-	3.5	-	mA	
I_{DD3}	Erase Current	-	2	-	mA	

Notes:

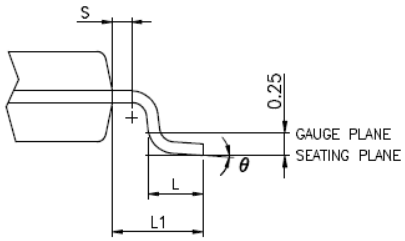
1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

6 PACKAGE DIMENSIONS

6.1 33-pin QFN (5 mm x 5 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		
D2	3.20	3.40	3.60	0.124	0.138	0.142
E2	3.20	3.40	3.60	0.124	0.138	0.142


S
0.25
GAUGE PLANE
SEATING PLANE
θ
L
L1

7 REVISION HISTORY

Revision	Date	Description
0.01	June 6, 2017	Preliminary version
0.02	November 27, 2017	1. In FEATURES : Revise the incorrect content of item Timer and PGA 2. Modify the content of AC Electrical Characteristics

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