ARM Cortex™-M0

32-BIT MICROCONTROLLER

NM1817 Series Product Brief

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1 GENERAL DESCRIPTION

The NM1817 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and three phase half-bridge power MOSFET and IGBT drivers with independent high and low side referenced output channels for motor driver applications which require high performance and integration. The Cortex™-M0 is the ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The MCU of NM1817 series can run up to 48MHz and offers 29.5K-bytes embedded program flash, size configurable Data Flash (shared with program flash), 2K-byte flash for the ISP, 1.5K-byte SPROM for security, and 4K-byte SRAM. Plentiful system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM1817 series in order to reduce component count, board space and system cost. These useful functions make the NM1817 series powerful for a wide range of motor driver applications.

The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts. It's also built-in the temperature sense output signal for MCU detection & one comparator for over current protection

Additionally, the NM1817 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM1817 is the combination of NM1120 and NPT23011 Gate Driver. User may refer to the TRM of NM1120 and the datasheet of NPT23011 for the detailed specification. The NM1120 BSP is also for NM1817 software developing.

2 FEATURES

- Gate Driver
  - Programmable enable/disable gate driver by MCU I/O of PC.4
  - Floating channel designed for bootstrap operation up to + 600V
  - Gate driver supply range from 12 to 18V
  - VCC/VBS Under-voltage lock-out
  - Cross conduction prevention
  - High side output in phase with HIN
- MCU Core
  - ARM® Cortex™-M0 core running up to 48MHz
  - One 24-bit system timer
  - Supports Low Power idle mode.
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Memory
  - 29.5Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2KB Flash memory for loader (LDROM)
  - Three 0.5KB Flash memory for security protection (SPROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - 48MHz internal oscillator (HIRC) (±1% accuracy at 25^0C, 5V)
  - 10kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 15 general-purpose I/O (GPIO) pins
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impedance
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - GPIO built-in Pull-up/Pull-low resistor for selection.
- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-

timer for each timer

- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Supports event counter function
- Supports Toggle Output mode
- Supports wake-up from Idle or Power-down mode

- Continuous Capture
  - Timer0, Timer1 and Systick support Continuous Capture function which can continuously capture at most 4 edges on one signal
- Enhanced Input Capture
  - One unit of 24-bit input capture counter.
  - Capture source:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - ACMP Trigger
    - ADC Trigger
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Support a built-in 16-bit PWM clock generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same clock source, clock divider, period and dead-zone generator
  - Supports group/independent/complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Support Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Supports rising, falling, central, period, and fault break interrupts
  - Supports duty/period trigger A/D conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
  - Gate driver PWM output by MCU PWM control

    if the ENGD pin of NM1817 is set to high level, then the output status of

NM1120 and gate driver is as the following table.

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

Otherwise, if the ENGD pin of NM1817 is set to low level, then the output of gate driver is all off.

- BPWM (Basic PWM Generator)
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - Supports to be configured as UART, SPI, I²C individually
  - Supports programmable baud-rate generator
- ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 1M SPS
  - Supports 2 sample/hold
  - Up to 8-ch single-end inputfrom I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Supports temperature sensor for measureing chip temperature
  - Support Simultaneous and Sequential function to continuous conversion 4 channels maximum.
- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13.
  - Unity gain frequency up to 8MHz
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- Hardware Divider
  - Signed (two's complement) integer calculation

- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Waiting for calculation ready automatically when reading quotient and remainder

- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - 8 programmable threshold levels:4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Packages:
  - 44-pin LQFP (10x10mm)
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

Part Number	Flash(KB)	SRAM(KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48 MHz*	BOD	PWM	Analog Comp.	PGA	ADC(12-Bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI											
							UART*	I²C	SPI									
NM1817NT	29.5	4	2	√	15	2	2	2	2	1	1	6	2	1	8x 12bit	1	√	LQFP44

Table 3.1-1 NM1817 Series Selection Guide

3.2 Pin Configuration

3.2.1 LQFP44-pin

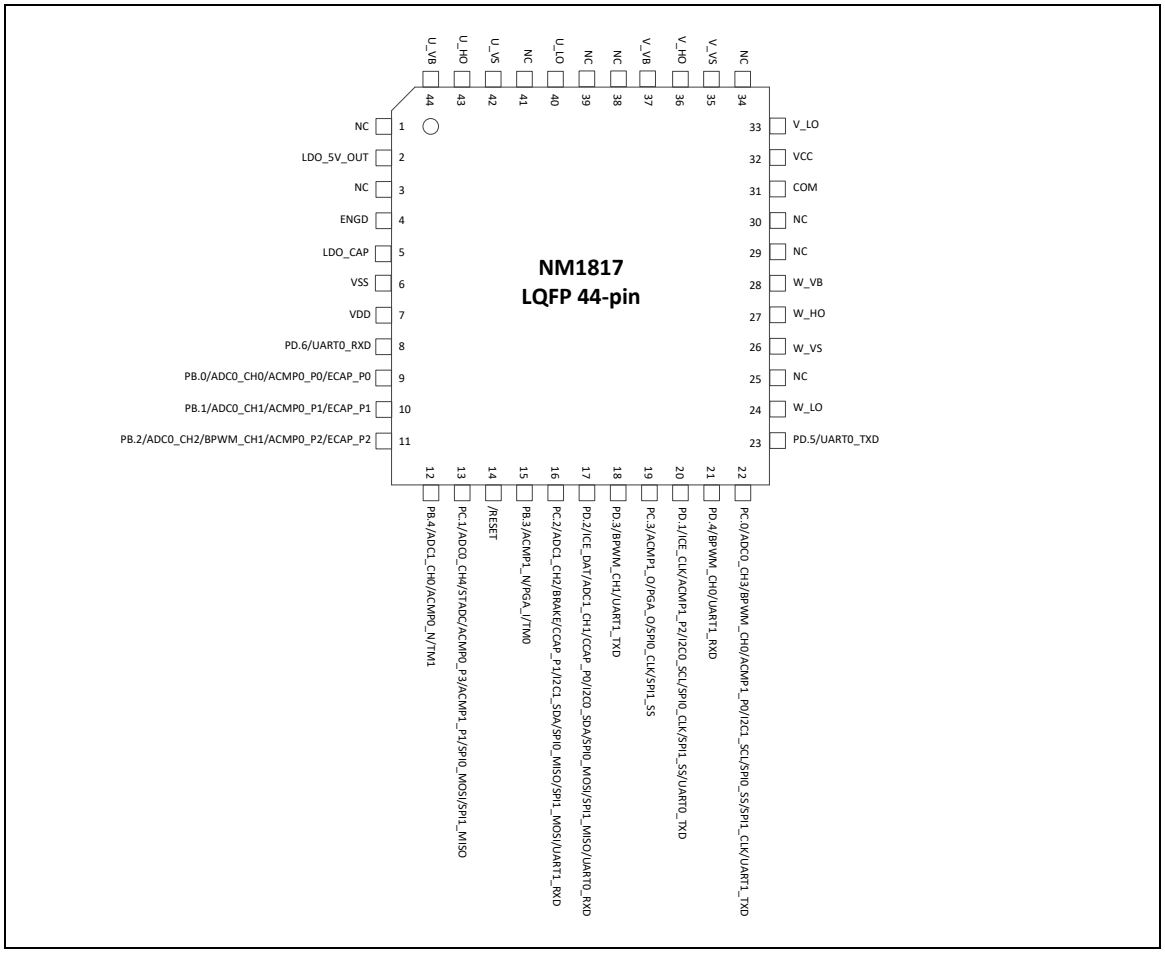


Figure 3.2-1 NM1817 LQFP 44-pin Diagram

3.3 Pin Description

NM1120	NPT23011	NM1817NT	Pin Name	Pin Type	Description
TSSOP28	SOP-20	LQFP 44-pin			
		2	LDO_5V_OUT	A	5V LDO output
26		4	ENGD	I	Gate driver enable pin. The pin is also internally connected to PC.4 of NM1120.
27		5	LDO_CAP	P	LDO output pin
28		6	VSS	P	Ground pin for digital circuit
1		7	VDD	P	Power supply for digital circuit
2		8	PD.6	I/O	General purpose digital I/O pin
			UART0_RXD	I	Data receiver input pin for UART0.
3		9	PB.0	I/O	General purpose digital I/O pin.
			ADC0_CH0	A	ADC0 channel0 analog input.
			ACMP0_P0	A	Analog comparator0 positive input pin.
			ECAP_P0	I	Enhanced Input Capture input pin
4		10	PB.1	I/O	General purpose digital I/O pin.
			ADC0_CH1	A	ADC0 channel1 analog input.
			ACMP0_P1	A	Analog comparator0 positive input pin.
			ECAP_P1	I	Enhanced Input Capture input pin
5		11	PB.2	I/O	General purpose digital I/O pin.
			ADC0_CH2	A	ADC0 channel2 analog input.
			BPWM_CH1	I/O	PWM channel1 output/capture input.
			ACMP0_P2	A	Analog comparator0 positive input pin.
			ECAP_P2	I	Input capture channel 2
6		12	PB.4	I/O	General purpose digital I/O pin.
			ADC1_CH0	A	ADC1 channel0 analog input.
			ACMP0_N	A	Analog comparator0 negative input pin.
			TM1	I/O	Timer1 event counter input / toggle output
7		13	PC.1	I/O	General purpose digital I/O pin.
			ADC0_CH4	A	ADC0 channel4 analog input.
			STADC	I	ADC external trigger input.
			ACMP0_P3	A	Analog comparator0 positive input pin.
			ACMP1_P1	A	Analog comparator1 positive input pin.
			SPI0_MOSI	I/O	SPI0 1st MOSI (Master Out, Slave In) pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.

8		**14**	**nRESET**	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
9		**15**	**PB.3**	**I/O**	General purpose digital I/O pin.
			ACMP1_N	**A**	Analog comparator1 negative input pin.
			PGA_I	**A**	PGA input pin
			TM0	**I/O**	Timer0 event counter input / toggle output
10		**16**	**PC.2**	**I/O**	General purpose digital I/O pin.
			ADC1_CH2	**A**	ADC1 channel2 analog input.
			BRAKE	**I**	Brake input pin of EPWM.
			CCAP_P1	**I**	Timer Continuous Capture input pin
			I2C1_SDA	**I/O**	I2C1 data input/output pin.
			SPI0_MISO	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin.
			SPI1_MOSI	**I/O**	SPI1 MOSI (Master Out, Slave In) pin.
			UART1_RXD	**I**	Data receiver input pin for UART1.
11		**17**	**PD.2**	**I/O**	General purpose digital I/O pin.
			ICE_DAT	**I/O**	Serial wired debugger data pin
			ADC1_CH1	**A**	ADC1 channel1 analog input.
			CCAP_P0	**I**	Timer Continuous Capture input pin
			I2C0_SDA	**I/O**	I2C0 data input/output pin.
			SPI0_MOSI	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin.
			SPI1_MISO	**I/O**	SPI1 MISO (Master In, Slave Out) pin.
			UART0_RXD	**I**	Data receiver input pin for UART0.
12		**18**	**PD.3**	**I/O**	General purpose digital I/O pin.
			BPWM_CH1	**I/O**	PWM channel1 output/capture input.
			UART1_TXD	**O**	Data transmitter output pin for UART1.
18		**19**	**PC.3**	**I/O**	General purpose digital I/O pin.
			ACMP1_O	**O**	Analog comparator1 output.
			PGA_O	**A**	PGA output pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin.
			SPI1_SS	**I/O**	SPI1 slave select pin
17		**20**	**PD.1**	**I/O**	General purpose digital I/O pin.
			ICE_CLK	**I**	Serial wired debugger clock pin
			ACMP1_P2	**A**	Analog comparator1 positive input pin.
			I2C0_SCL	**I/O**	I2C0 clock pin.

			SPI0_CLK	I/O	SPI0 serial clock pin.
			SPI1_SS	I/O	SPI1 slave select pin
			UART0_TXD	O	Data transmitter output pin for UART0.
16		21	PD.4	I/O	General purpose digital I/O pin.
			BPWM_CH0	I/O	PWM channel0 output/capture input.
			UART1_RXD	I	Data receiver input pin for UART1.
15		22	PC.0	I/O	General purpose digital I/O pin.
			ADC0_CH3	A	ADC0 channel3 analog input.
			BPWM_CH0	I/O	PWM channel0 output/capture input.
			ACMP1_P0	A	Analog comparator1 positive input pin.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI0_SS	I/O	SPI0 slave select pin.
			SPI1_CLK	I/O	SPI1 serial clock pin
			UART1_TXD	O	Data transmitter output pin for UART1.
19		23	PD.5	I/O	General purpose digital I/O pin.
			UART0_TXD	O	Data transmitter output pin for UART0.
	7	24	W_LO	HO	Low side gate driver output
	8	26	W_VS	HP	High side floating supply return
	9	27	W_HO	HO	High side gate driver output
	10	28	W_VB	HP	High side floating supply
	11	31	COM	HP	Low side power supply return
	12	32	VCC	HP	Low side and logic fixed power supply
	13	33	V_LO	HO	Low side gate driver output
	14	35	V_VS	HP	High side floating supply return
	15	36	V_HO	HO	High side gate driver output
	16	37	V_VB	HP	High side floating supply
	17	40	U_LO	HO	Low side gate driver output
	18	42	U_VS	HP	High side floating supply return
	19	43	U_HO	HO	High side gate driver output
	20	44	U_VB	HP	High side floating supply
25	1		HIN1		PWM0 connect to HIN1
24	2		LIN1		PWM1 connect to LIN1
23	3		HIN2		PWM2 connect to HIN2
22	4		LIN2		PWM3 connect to LIN2
21	5		HIN3		PWM4 connect to HIN3
20	6		LIN3		PWM5 connect to LIN3

13,14		**1,3,25,29,30, 34,38,39,41**			No connected

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

4 BLOCK DIAGRAM

4.1 NM1817 Block Diagram

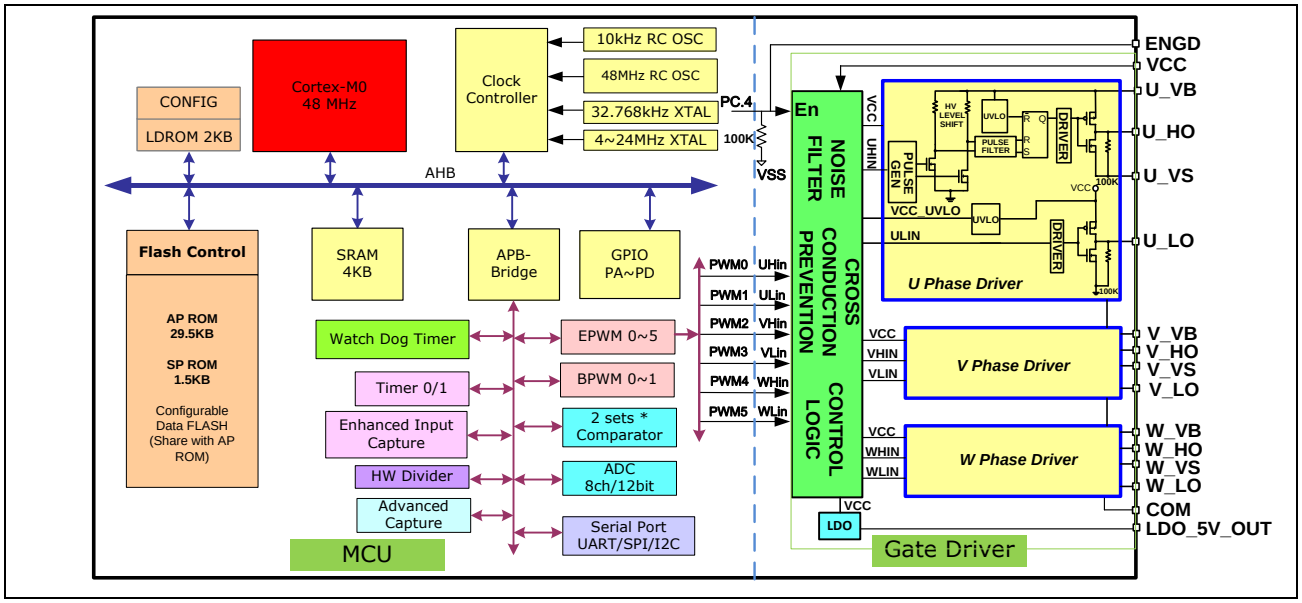


Figure 4.1-1 NM1817 Block Diagram

5 NM1817 ELECTRICAL CHARACTERISTICS

The electrical characteristics refer to both MCU NM1120 and Gate Driver NPT23011.

According to Figure 4.1-1, we can list a table of pin definition in NM1817 as below:

	Alternative function , MFP_0 means setting MFP[3:0]=0x0, MFP_5 means MFP[3:0]=0x5																													
GPIO	ICE XTAL		ADC		PWM_BRAKE		ACMP0		ACMP1		PGA(OP)		TIMER		I2C		SPIO		SPI1		UART									
MFP_0	MFP_1		MFP_2		MFP_3		MFP_4		MFP_5		MFP_6		MFP_7		MFP_8		MFP_9		MFP_A		MFP_B									
GPA0	CLKO	O			EPWM_CH0	O									I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O								
GPA1					EPWM_CH1	O									I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I								
GPA2					EPWM_CH2	O									I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I								
GPA3					EPWM_CH3	O									I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O								
GPA4	XT_IN	A			EPWM_CH4	O																								
GPA5	XT_OUT	A			EPWM_CH5	O	ACMP0_O	O																						
GPB0			ADC0_CH0	A			ACMP0_P0	A					ICAP0	I																
GPB1			ADC0_CH1	A			ACMP0_P1	A					ICAP1	I																
GPB2			ADC0_CH2	A	BPWM_CH1	O	ACMP0_P2	A					ICAP2	I																
GPB3									ACMP1_N	A	PGA_I	A	T0	I/O																
GPB4			ADC1_CH0	A			ACMP0_N	A					T1	I/O																
GPC0			ADC0_CH3	A	BPWM_CH0	O			ACMP1_P0	A					I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O								
GPC1			ADC0_CH4	A	STADC	I	ACMP0_P3	A	ACMP1_P1	A							SPI0_MOSI	I/O	SPI1_MISO	I/O										
GPC2			ADC1_CH2	A	PWM_BRAKE	I							CCAP	I	I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I								
GPC3									ACMP1_O	O	PGA_O	A					SPI0_CLK	I/O	SPI1_SS	I/O										
GPC4													ICAP0	I																
nRESET																														
GPD1	ICE_CLK	I							ACMP1_P2	A					I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O								
GPD2	ICE_DAT	I/O	ADC1_CH1	A									CCAP	I	I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I								
GPD3					BPWM_CH1	O															UART1_TXD	O								
GPD4					BPWM_CH0	O															UART1_RXD	I								
GPD5																					UART0_TXD	O								
GPD6																					UART0_RXD	I								
VDD																														
VSS																														

: Function has been reserved for another usage.

Attention :

a. Some functions would be prohibition because of the limitation of pin definition in NM1817.

b. GPA0 ~ GPA5 should be set as EPWM0 ~ EPWM5, GPC4 should be set as GPIO.

5.1 NM1120 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit

V_{DD}–V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 NM1120 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.1 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

V_{DD}	Operation voltage	2.1	-	5.5	V	V_{DD} = 2.1V ~ 5.5V up to 48 MHz			
V_{SS}/A_{VSS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.14	1.20	1.24	V	V_{DD} = 3.0V ~ 5.5V, T_A = -40°C~105°C			
I_{DD5}	Operating Current Normal Run Mode HCLK = 48 MHz	-	9.7	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD6}		-	7.4	-	mA	5.5V	X	48 MHz	X
I_{DD7}		-	9.7	-	mA	3V	X	48 MHz	V
I_{DD8}		-	7.4	-	mA	3V	X	48 MHz	X
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz	-	5.4	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD2}		-	4.4	-	mA	5.5V	24 MHz	X	X
I_{DD3}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD4}		-	4.4	-	mA	3V	24 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 16 MHz	-	3.7	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD10}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD11}		-	3.7	-	mA	3V	16 MHz	X	V
I_{DD12}		-	3.1	-	mA	3V	16 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz	-	2.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD10}		-	2.3	-	mA	5.5V	12 MHz	X	X
I_{DD11}		-	2.8	-	mA	3V	12 MHz	X	V
I_{DD12}		-	2.3	-	mA	3V	12 MHz	X	X

I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz	-	1.2	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD14}		-	1.0	-	mA	5.5V	4 MHz	X	X
I_{DD15}		-	1.2	-	mA	3V	4 MHz	X	V
I_{DD16}		-	1.0	-	mA	3V	4 MHz	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32 kHz	-	291.7	-	µA	V_{DD}	**LXT	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD18}		-	290.7	-	µA	5.5V	32 KHz	V	X
I_{DD19}		-	280.8	-	µA	3V	32 KHz	V	V[1]
I_{DD20}		-	281.4	-	µA	3V	32 KHz	V	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz	-	248.0	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD18}		-	247.7	-	µA	5.5V	X	10 KHz	X
I_{DD19}		-	237.9	-	µA	3V	X	10 KHz	V[2]
I_{DD20}		-	237.5	-	µA	3V	X	10 KHz	X
I_{IDLE5}	Operating Current Idle Mode HCLK= 48 MHz	-	4.9	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE6}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE7}		-	4.9	-	mA	3V	X	V	V
I_{IDLE8}		-	2.6	-	mA	3V	X	V	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 24 MHz	-	2.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE2}		-	1.9	-	mA	5.5V	24 MHz	X	X
I_{IDLE3}		-	2.8	-	mA	3V	24 MHz	X	V
I_{IDLE4}		-	1.9	-	mA	3V	24 MHz	X	X

I_{IDLE9}	Operating Current Idle Mode HCLK = 16 MHz	-	2.0	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE11}		-	2.0	-	mA	3V	V	X	V
I_{IDLE12}		-	1.4	-	mA	3V	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 12 MHz	-	1.5	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.0	-	mA	5.5V	V	X	X
I_{IDLE11}		-	1.5	-	mA	3V	V	X	V
I_{IDLE12}		-	1.0	-	mA	3V	V	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	0.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE14}		-	0.6	-	mA	5.5V	V	X	X
I_{IDLE15}		-	0.7	-	mA	3V	V	X	V
I_{IDLE16}		-	0.6	-	mA	3V	V	X	X
I_{DD17}	Operating Current Idle Mode HCLK = 32 kHz	-	274.3	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{DD18}		-	273.0	-	µA	5.5V	X	V	X
I_{DD19}		-	265.0	-	µA	3V	X	V	V[1]
I_{DD20}		-	263.9	-	µA	3V	X	V	X
I_{DD17}	Operating Current Idle Mode HCLK = 10 kHz	-	232.6	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{DD18}		-	232.2	-	µA	5.5V	X	V	X
I_{DD19}		-	222.5	-	µA	3V	X	V	V[2]
I_{DD20}		-	222.1	-	µA	3V	X	V	X

I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1.9	-	µA	V_{DD} = 5.5V, All oscillators and analog blocks turned off.
I_{PWD2}		-	1.7	-	µA	V_{DD} = 3V, All oscillators and analog blocks turned off.
I_{LK}	Input Leakage Current PA/PB/PC/PD	-1	-	+1	µA	V_{DD} = 5.5V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage PA/PB/PC/PD (TTL Input)	-0.3	1.33		V	V_{DD} = 5.5 V
		-0.3	1			V_{DD} = 3.3 V
V_{IH1}	Input High Voltage PA/PB/PC/PD (TTL Input)		1.47	V_{DD} + 0.3	V	V_{DD} = 5.5 V
			1.08	V_{DD} + 0.3		V_{DD} = 3.3 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.1 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), PA/PB/PC/PD	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), PA/PB/PC/PD	$0.7V_{DD}$	-	-	V	-
I_{IL}	Logic 0 Input Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-63.65		µA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current PA/PB/PC/PD	-	-566.7	-	µA	V_{DD} = 5.5 V
I_{SR11}	Source Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-372	-	µA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR12}		-	-76.8	-	µA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR13}		-	-37.3	-	µA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SR21}	Source Current PA/PB/PC/PD	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR22}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V

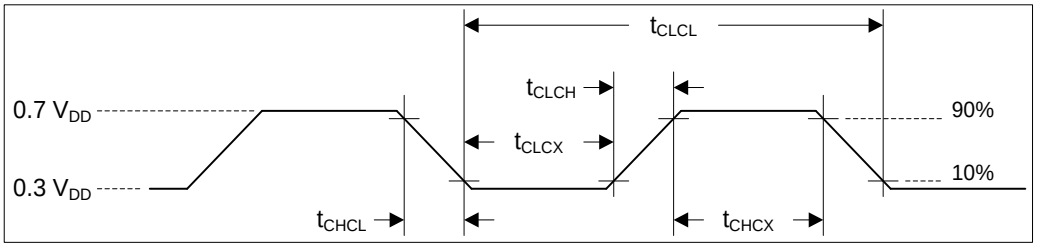
I_{SR23}	(Push-pull Mode)	-	-2	-	mA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SK11}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK12}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.1 V, V_{IN} = 0.4 V

Notes:
1. Only enable modules which support 32kHz LIRC clock source
2. Only enable modules which support 10kHz LIRC clock source
3. Guaranteed by design, not test in production.

** : The function has been reserved in NM1817.

5.3 NM1120 AC Electrical Characteristics

5.3.1 **External Input Clock (function has been reserved in NM1817)



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

5.3.2 **External 4~24MHz High Speed Crystal (HXT)(function has been reserved in NM1817)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.1	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	414	-	uA	12MHz, V_{DD} = 5.5V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

5.3.3 **Typical Crystal Application Circuits (function has been reserved in NM1817)

Crystal	C1	C2
4MHz ~ 24MHz	10~20 pF	10~20pF

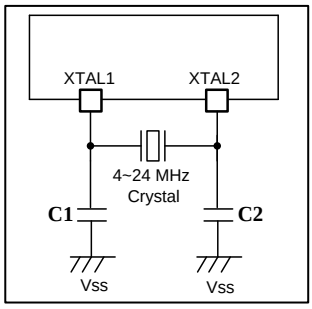


Figure 5-1 NM1120 Typical Crystal Application Circuit

5.3.4 48MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
			2%		%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	1090	-	μA	T_A = 25 ℃,V_{DD} = 5 V

5.3.5 10kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-50[1]	-	+50[1]	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃
I_{LRC}	Operating Current	-	0.4	-	μA	T_A = 25 ℃,V_{DD} = 5 V

Note1: These parameters are characterized but not tested.

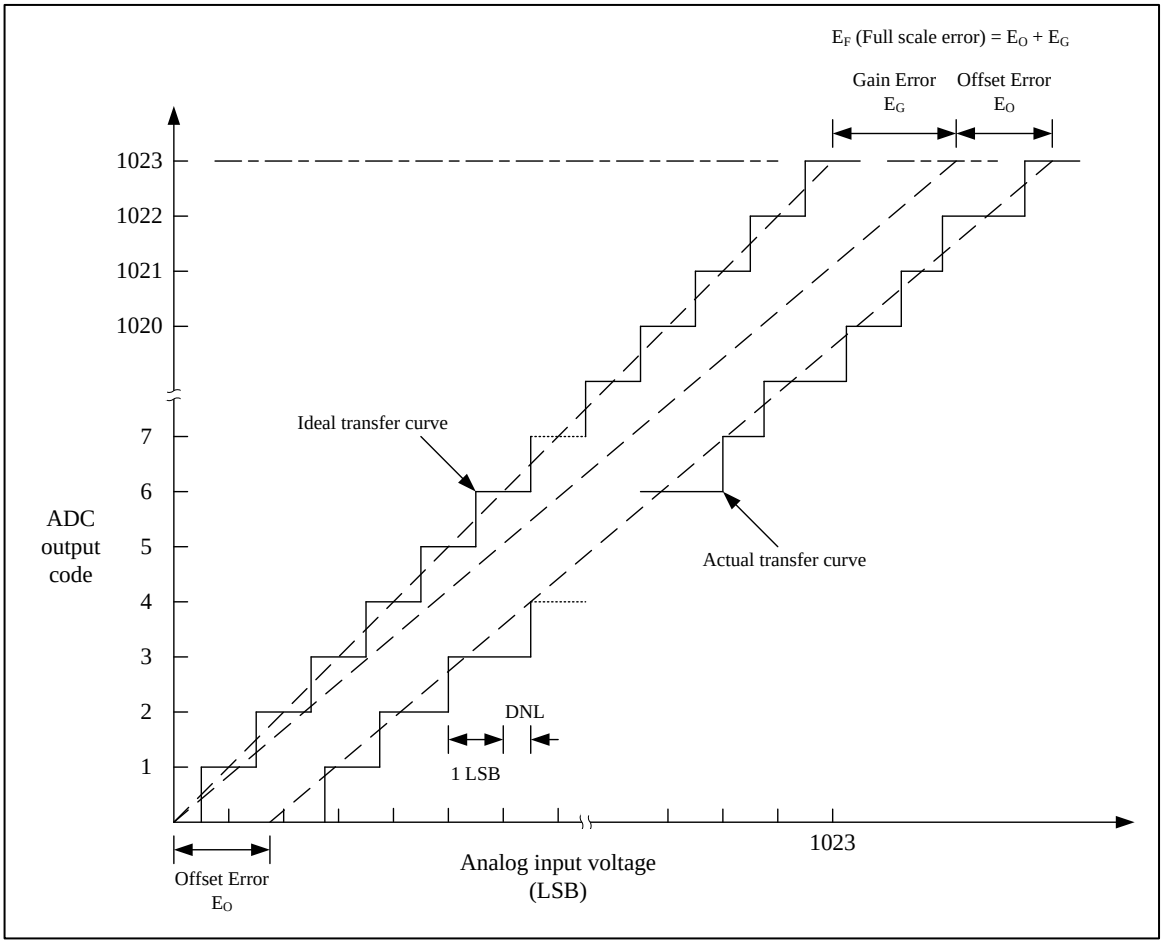
5.4 NM1120 Analog Characteristics

5.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±2	-	LSB	VDD = 5.5V
INL	Integral Nonlinearity Error	-	±1	-	LSB	VDD = 5.5V
E_O	Offset Error	-	-0.33	-	LSB	VDD = 5.5V
E_G	Gain Error (Transfer Gain)	-	0.33	-	LSB	VDD = 5.5V
E_A	Absolute Error	-	-2.62	-	LSB	VDD = 5.5V
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency		12	16	MHz	V_{DD} = 3.0 ~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			1/F_{ADC}	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]		1000	1050	ns	V_{DD} = 3.0~5.5 V
V_{DD}	Supply Voltage	3.0	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-
R_{IN}	Input Load[2]	-	2.5	-	kΩ	-

Note:

1. ADC voltage reference is the same with V_{DD}.
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of CIN is less than about 10% of typical value and the variation of RIN is less about 20% of typical value.
3. Guaranteed by design, not test in production.The conversion time is up to auto-completion of analog comparison in ADC IP and the typical value is about 1000ns at V_{DD} = 5V.



5.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.1	-	5.5	V	-
V_{LDO}	Output Voltage		1.5		V	-
T_A	Temperature	-40	25	105	℃	

Notes:
It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

5.4.3 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	100	-	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Hysteresis	4.33	4.3	4.39	V	BOV_VL [2:0] = 3
		4.03	4.0	4.10	V	BOV_VL [2:0] = 2
		3.73	3.7	3.79	V	BOV_VL [2:0] = 7
		3.02	3.0	3.09	V	BOV_VL [2:0] = 1
		2.72	2.7	2.79	V	BOV_VL [2:0] = 6
		2.42	2.4	2.49	V	BOV_VL [2:0] = 0

		2.22	2.2	2.30	V	BOV_VL [2:0] = 5
		2.02	2.0	2.09	V	BOV_VL [2:0] = 4
V_{BOD}	Brown-out Detector		4.3		V	BOV_VL [2:0] = 3
			4.0		V	BOV_VL [2:0] = 2
			3.7		V	BOV_VL [2:0] = 7
			3.0		V	BOV_VL [2:0] = 1
			2.7		V	BOV_VL [2:0] = 6
			2.4		V	BOV_VL [2:0] = 0
			2.2		V	BOV_VL [2:0] = 5
			2.0		V	BOV_VL [2:0] = 4

5.4.4 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage		1.75		V	-

5.4.5 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	47		μA	V_{DD}=5.5V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	225	-	ns	
V_{HYS}	Hysteresis	-	10	-	mV	ACMPPHYSEN = 01
V_{HYS}	Hysteresis	-	90	-	mV	ACMPPHYSEN = 10
T_{STB}	Stable time	-	1.06	-	μs	

Notes:
Guaranteed by design, not test in production.

5.4.6 PGA

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
	Operation voltage range	2.5	3.3	5.5	V	
	Operating Current			5	mA	VDD5V=5V, T=125□

	Operating Temperature	-40	25	125	℃	
	Input Offset with calibration Type corner, temp=25, VCM=AVDD/2			+2	mV	
	Input Offset Average Drift			3.5	uV/℃	
	Output Swing	0.1		VDD5V- 0.1	V	
	PGA gain accuracy	-1		+1	%	
	Input Common Mode Range	0		VDD5V- 1.5	V	
	DC Gain	50	80		dB	
	Unity Gain Frequency	7		8.2	MHz	VDD = 5V
	Phase Margin	50°			°	
	PSRR+	49	90		dB	VDD = 5V
	CMRR	69	90		dB	VDD = 5V
	Slew Rate+		6.0	7.5	V/us	VDD=5V, RLoad=1.3K, CLoad=100p
	Wake Up Time			20	us	

Notes:
Guaranteed by design, not test in production.

5.4.7 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain[1]	-	-1.81	-	mV/℃	
-	Offset[1,2]	-	725	-	mV	TA = 0 ℃

Note:
1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation. Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

5.5 NPT23011 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	600	V
V_S	High side floating supply offset voltage	V_B – 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	- 0.3	25	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage	- 0.3	V_{CC} + 0.3	

dV_S / dt	Allowable offset supply voltage transient	—	50	V / ns
P_D	Package power dissipation @ TA ≤ + 25 ℃ (20 lead SOIC)	—	1.5	W
R_{thJA}	Thermal resistance, junction to ambient (20 lead SOIC)	—	60	℃ / W
T_J	Junction temperature	—	150	℃
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

5.6 NPT23011 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply absolute voltage	V_S + 12	V_S + 18	V
V_S	High side floating supply offset voltage	- 6	450	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	12	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
tdead	HIN & LIN dead time (depends on MCU control)	1	-	us
T_A	Ambient temperature	- 40	125	℃

5.7 NPT23011 Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, T_A = 25 ºC, unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
**V_{IH}	Logic " 1 " input voltage	V_{CC} = 10V to 15V	2.4	-	-	V
**V_{IL}	Logic " 0 " input voltage	V_{CC} = 10V to 15V	-	-	0.8	
I_{LK}	Offset supply leakage current (one phase)	V_B = V_S = 600 V	-	-	60	uA
I_{QBS}	Quiescent V_{BS} supply current (one phase)	V_{IN} = 0 V or 5 V	-	-	250	
I_{QCC}	Quiescent V_{CC} supply current	V_{IN} = 0 V or 5 V	-	-	1000	
I_{IN+}	Logic " 1 " input bias current	V_{IN} = 5 V	-	50	100	
I_{IN-}	Logic " 0 " input bias current	V_{IN} = 0 V	-	0	1	
V_{CCUV+}	V_{CC} supply under voltage positive going threshold		8	9	10	V
V_{BSUV+}	V_{BS} supply under voltage positive going threshold		7.7	8.7	9.7	

V_{CCUV-}	V_{CC} supply under voltage negative going threshold		7	8	9	
V_{BSUV-}	V_{BS} supply under voltage negative going threshold		6.8	7.8	8.8	
I_{O+}	Souring peak current	C_L=0.22uF, 20KHz	-	300	-	mA
I_{O-}	Sink peak current	C_L=0.22uF, 20KHz	-	600	-	mA
**R_{IN}	HIN, LIN pin pull low resistor		-	100	-	KΩ
R_{OUT}	HO, LO pin pull low resistor(Applied between LO - COM, HO - VS)		-	100	-	KΩ
R_{EN}	EN pin pull low resistor		-	100	-	KΩ

Note:
1. Different versions decided by metal layers change.
2. ESD device; MM>200V; HBM>2KV; power bus holding voltage should be > 20V

** : EPWMx of NM1120 and HINx/LINx of NPT23011 are bonded inside NM1817, so specification are characterized but not tested. The item is only for reference.

5.8 NPT23011 Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1nF, T_A = 25 ºC, unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
**ton	Turn-on propagation delay	-	330	-	ns	VS = 0V
**toff	Turn-off propagation delay	-	250	-	ns	VS = 0V
tr	Turn on rise time	-	50	-	ns	
tf	Turn off fall time	-	30	-	ns	
DT	Dead Time	-	500	-	ns	

Note： 1. Input PWM pulse width must be ≧ 1 μsec for HO & LO normally output.

** : EPWMx of NM1120 and HINx/LINx of NPT23011 are bonded inside NM1817, so specification are characterized but not tested. The item is only for reference.

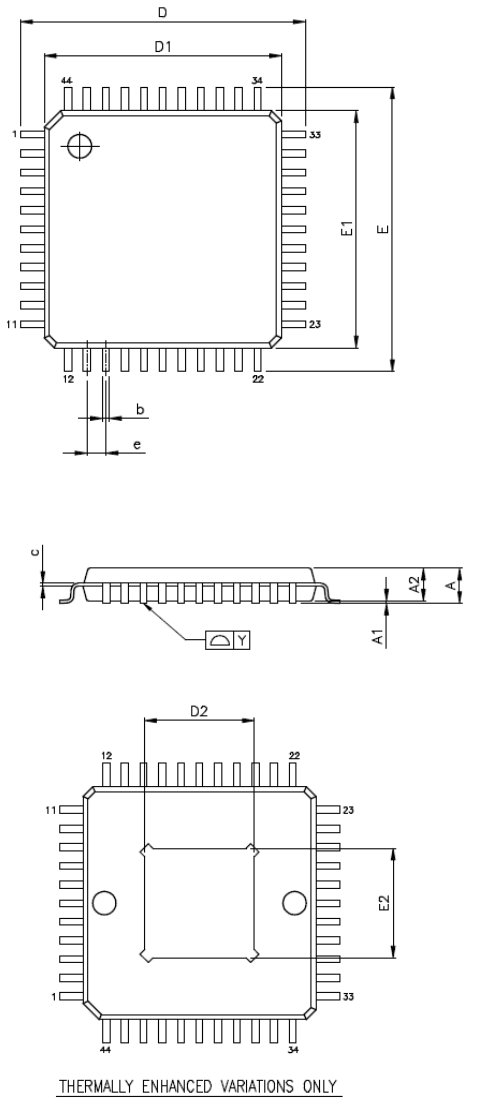
5.9 DC Electrical Characteristic for LDO_5V_OUT

V_{BIAS}(V_{CC}, V_{BS}) = 15 V, T_A= 25ºC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{5V}	5V Output Voltage		4.75	5	5.25	V
I_{5V}	5V Output Current		-	30	-	mA

6 PACKAGE DIMENSION

6.1 LQFP 44-pin(10mm x 10mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	–	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
Y	0.10		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
18*X18*	4.50	4.85	4.50	4.85

5 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,
實際的字元請參照bonding diagram所示.

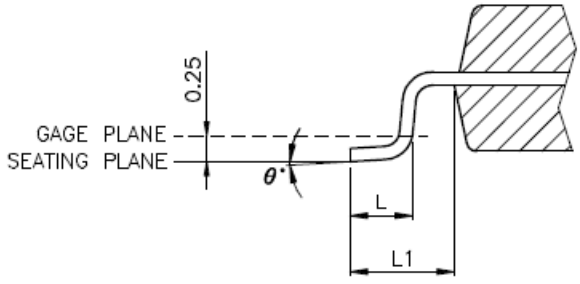
5 "*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:

1.JEDEC OUTLINE:
MS-026 BCB
MS-026 BCB-HD(THERMALLY ENHANCED VARIATIONS ONLY)

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.



7 ORDERING INFORMATION

Part Number	Supplied As	Package Type	Operating Temperature
NM1817NT	1500 units/ T&R	LQFP44, Green Package	Commercial, -40℃~105℃

8 REVISION HISTORY

Revision	Date	Description
0.1	March 9, 2017	Preliminary version
0.2	April 6, 2017	1. Revised the typo of V_B and V_{CC} in section 5.2.
0.3	August 1, 2017	1. Update the following content 5.2 Absolute Maximum Ratings for Gate Driver 5.3.2 DC Electrical Characteristic for Gate Driver 5.4.9 Dynamic Electrical Characteristics for Gate Driver.
0.4	December 5, 2017	1. In FEATURES: Revise “three Timers” to “two Timers”. 2. Modify AC Electrical Characteristics.
0.5	March 15,2018	1.Chapter 1: adding description of the composition of NM1817. 2. Chapter 2: a. Revise the description in clock control. b. Revise the description in 12-bit ADC c. Revise the description in reliability. d. Modify the description in " Gate driver PWM output by MCU PWM control" 3.Chapter 3.2: a. Removes PC.4 and adds the description of ENGDpin to pin description section. b. Adds the function "ECAP_P2" to Pin 11. 4. Chapter 4: Revise Block Diagram 5 .Chapter 5.3.2: Change the Typ value of the I_{O+}/I_{O-} from 200/350 mA to 350/650 mA in the DC Electrical Characteristic for Gate Driver section. 6.Add the LDO parameters in the DC Electrical Characteristic for Gate Driver section 7. Chapter 5.4.9: Change the Typ value of the $t_{on}/t_{off}/t_r/t_{EN}$/DTfrom420/420/150/430/300us to 300/300/100/300/600us in the Dynamic Electrical Characteristics for Gate Driver section. 8. Chapter 3.1.1: Modify the function of pin 4.
0.6	May 15,2018	Revise the content of the chapter 5 Electronic characteristics. Replace the original content with a note. Chapter 1: Modify NPT2301 to NPT23011.
0.7	May 22,2018	Chapter 2: a. Remove the feature description of "LIN".

		b. Modify the ADC channel counts from IO. Chapter 5.1: add the specification of LDO_5V. Chapter 7: Add ordering information.
0.8	Oct. 8,2018	1. Chapter 2: a. Update GPIO no. from 16 pins to 15 pins b. Add BPWM c. Modify EPWM: remove sync mode/ adds clock source description d. Modify ECAP: Capture source description e. Remove Reliability description f. Add "Programmable enable/disable gate driver by MCU I/O of PC.4" to Gate Driver Feature. g. Change Gate driver supply voltage range from”10V to 18V” to “12V to 18V” 2. Chapter 5: Add the content of AC/DC Electrical Characteristics 3. Chapter 3: a. Add selection guide. b. Modify Pin Description.
0.9	Mar. 27,2020	1. Modify the table in Chapter 5.7 and Chapter 5.8.
0.91	Nov. 8,2022	1. Add compliance statement of International Environmental Regulations.

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