ARM Cortex®-M0

32-BIT MICROCONTROLLER

NM18107 Series Product Brief

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1 GENERAL DESCRIPTION

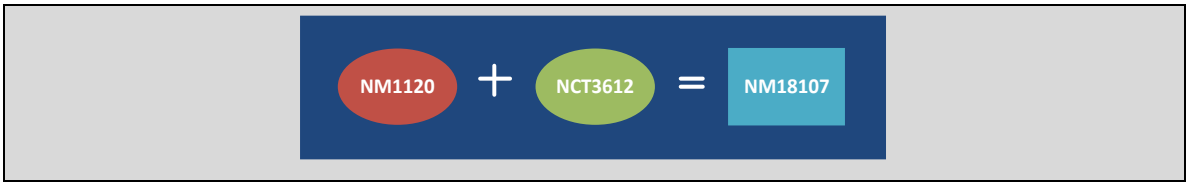
The NM18107 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and monolithic half-bridge gate driver for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The MCU of NM18107 series can run up to 48 MHz and offers 29.5K-bytes embedded program flash, size configurable Data Flash (shared with program flash), 2K-byte flash for the ISP, 1.5K-byte SPROM for security, and 4K-byte SRAM. Plentiful system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM18107 series in order to reduce component count, board space and system cost. These useful functions make the NM18107 series powerful for a wide range of motor driver applications.

The power supply input of NM18107 is up to 35V. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component.

Additionally, the NM18107 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM18107 is the combination of MCU NM1120 and Gate Driver NCT3612.User may refer to the TRM of NM1120 and the datasheet of NCT3612 for the detailed specification. The NM1120 BSP is also for NM18107 software developing.



2 FEATURES

- Recommended operation Supply Voltage VIN Range from 8 to 35V
- Gate Driver
  - Programmable enable/disable gate driver by MCU I/O of PC.4
  - 8 ~ 35V Operate Supply Voltage Range
  - 250mA Source & 500mA Sink Gate Drive Current Capability @VIN > 20V
  - Integrated 2 LDO
    - 5V, 35mA, LDO Output for MCU power supply(Note1)
    - 12V, LDO for internal use
  - Sleep Mode Support (< 100uA)
  - Integrated bootstrap diode
  - 3 or 6 PWM Input Mode Supported
  - Direction Control for Motor Forward / Reverse sequence by PWM input signal
  - Protection:
    - UVLO (Under Voltage Lockout)
    - Thermal Shutdown Protection (typically @165℃)
- MCU Core
  - ARM® Cortex™-M0 core running up to 48 MHz
  - One 24-bit system tick timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Memory
  - 29.5KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2KB Flash memory for loader (LDROM)
  - Three 0.5KB Flash memory for security protection (SPROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25^0C, 5V)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 14 general-purpose I/O (GPIO) pins and 1 input-only pin (HVIN)
  - Four I/O modes:

- Quasi-bidirectional input/output
- Push-Pull output
- Open-Drain output
- Input only with high impendence

- Optional TTL/Schmitt trigger input
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink I/O mode
- GPIO built-in Pull-up/Pull-low resistor for selection
- The input-only pin with high voltage capability upto VIN voltage

- Timer
  - Provides two Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides four operation modes: One-shot, Periodic, Toggle and Continuous
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
- Continuous Capture
  - Timer0, Timer1 and Systick support Continuous Capture function which can continuously capture 4 edges on one signal
- Enhanced Input Capture
  - One 24-bit input capture up-counter
  - Capture surce:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - Outputs of ACMP0 and ACMP1
    - ADC compare result
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Support a built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot PWM function

- Supports Edge-aligned and Center-aligned PWM type
- Support Asymmetric mode
- Programmable dead-zone insertion between complementary channels
- Each output has independent polarity setting control
- Hardware fault brake and software brake protections
- Supports rising, falling, central, period, and fault break interrupts
- Supports duty/period trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function
- Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

- BPWM (Basic PWM Generator)
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - Supports to configure as UART, SPI, I²C individually
  - Supports programmable baud-rate generator
- 12-bit ADC (Analog-to-Digital Converter)
  - 1us conversion time at minimum
  - Supports 2 sample/hold
  - Up to 8-ch single-end input from I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Support temperature sensor for measurement chip temperature
  - Support Simultaneous and Sequential function to continuous conversion 4 channels maximum.

- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13.
  - Unity gain frequency up to 8MHz
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: ESD HBM pass 2 kV; ESD 2 kV
- Packages:
  - 33-pin, QFN, 5mm x 5mm
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Note:

1. Higher LDO output current causes the higher IC temperature. Refer to section 5.8 NCT3612 DC Electrical Characteristics

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NM18107 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48 MHz*	BOD	PWM	Analog Comp.	PGA	ADC (12-Bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI											
							UART*	I^2C	SPI									
NM18107Y	29.5	4	2	√	14	2	2	2	1/1	1	1	6	2	1	8x 12bit	1	√	QFN 33 (5x5mm)

Table 3.1-1 NM18107 Base Series Selection Guide

3.2 Pin Configuration

3.2.1 NM18107Y Series QFN 33-Pin Diagram

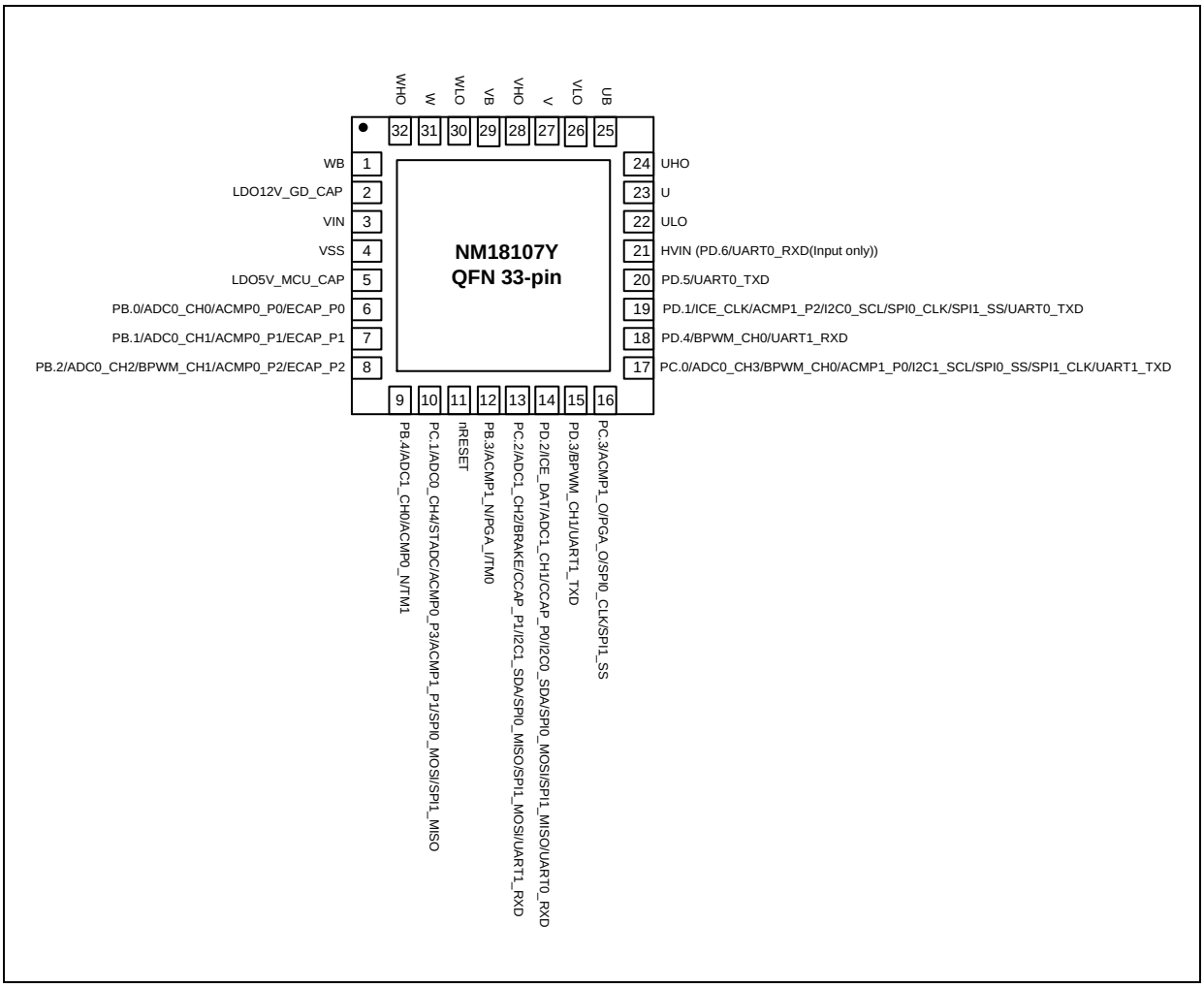


Figure 3.2-1 NM18107Y QFN 33-pin Diagram

3.3 Pin Description

3.3.1 NM18107Y Series QFN 33-Pin Description

NM1120 TSSOP28	NCT3612 QFN28 4x4	NM18107Y QFN33 5x5	Pin Name	Pin Type	Description
	3	1	WB	HP	W-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and W.
	4	2	LDO12V_GD_CAP	P	12V LDO OUT for gate driver(VR12V). Recommend connect an at least 4.7uF capacitor to GND.
	5	3	VIN	HP	Power supply for internal control circuit. Recommend connect a capacitor to GND to stable the input power.
28	6	4	VSS	P	Ground pin for digital circuit
1	7	5	LDO5V_MCU_CAP	P	5V LDO OUT for MCU(5VOUT). Recommend connect a 1uF capacitor to GND.
3		6	PB.0	I/O	General purpose digital I/O pin.
			ADC0_CH0	A	ADC0 analog input channel 0.
			ACMP0_P0	A	Comparator0 positive input pin.
			ECAP_P0	I	Input capture channel 0
4		7	PB.1	I/O	General purpose digital I/O pin.
			ADC0_CH1	A	ADC0 analog input channel 1.
			ACMP0_P1	A	Comparator0 positive input pin.
			ECAP_P1	I	Input capture channel 1
5		8	PB.2	I/O	General purpose digital I/O pin.
			ADC0_CH2	A	ADC0 analog input channel 2.
			BPWM_CH1	O	Basic PWM channel 1 output
			ACMP0_P2	A	Comparator0 positive input pin.
			ECAP_P2	I	Input capture channel 2
6		9	PB.4	I/O	General purpose digital I/O pin.
			ADC1_CH0	A	ADC1 analog input channel 0.
			ACMP0_N	A	Comparator0 negative input pin.
			TM1	I	Timer1 event counter input / toggle output
7		10	PC.1	I/O	General purpose digital I/O pin.
			ADC0_CH4	A	ADC0 analog input channel 4.
			STADC	I	External ADC trigger input pin.

			ACMP0_P3	A	Comparator0 positive input pin.
			ACMP1_P1	A	Comparator1 positive input pin.
			SPI0_MOSI	I/O	SPI0 1st MOSI (Master Out, Slave In) pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
8		11	nRESET	I	External reset pin, internal pull-high.
9		12	PB.3	I/O	General purpose digital I/O pin.
			ACMP1_N	A	Comparator1 negative input pin.
			PGA_I	A	PGA analog input pin.
			TM0	I	Timer0 event counter input / toggle output
10		13	PC.2	I/O	General purpose digital I/O pin.
			ADC1_CH2	A	ADC1 channel2 analog input.
			BRAKE	I	Brake input pin of EPWM.
			CCAP_P1	I	Timer Continuous Capture input pin
			I2C1_SDA	I/O	I2C1 data input/output pin.
			SPI0_MISO	I/O	SPI0 1st MISO (Master In, Slave Out) pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			UART1_RXD	I	Data receiver input pin for UART1.
11		14	PD.2	I/O	General purpose digital I/O pin.
			ICE_DAT	I/O	Serial wired debugger data pin
			ADC1_CH1	A	ADC1 analog input channel 1.
			CCAP_P0	I	Continuous Capture Input
			I2C0_SDA	I/O	I2C0 data pin.
			SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin
			UART0_RXD	I	UART0 data receiver input pin.
12		15	PD.3	I/O	General purpose digital I/O pin.
			BPWM_CH1	I/O	PWM channel1 output/capture input.
			UART1_TXD	O	Data transmitter output pin for UART1.
18		16	PC.3	I/O	General purpose digital I/O pin.
			ACMP1_O	O	Analog comparator1 output
			PGA_O	A	PGA output pin
			SPI0_CLK	I/O	SPI0 clock pin.

			SPI1_SS	I/O	SPI1 Slave Select
15		17	PC.0	I/O	General purpose digital I/O pin.
			ADC0_CH3	A	ADC0 analog input channel 3.
			BPWM_CH0	O	Basic PWM channel 0 output
			ACMP1_P0	A	Comparator1 positive input pin.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI0_SS	I	SPI0 slave selection pin.
			SPI1_CLK	I/O	SPI1 clock pin.
			UART1_TXD	O	UART1 data transmitter output pin.
16		18	PD.4	I/O	General purpose digital I/O pin.
			BPWM_CH0	I/O	PWM chanel0 output/capture input.
			UART1_RXD	I	Data receiver input pin for UART1
17		19	PD.1	I/O	General purpose digital I/O pin.
			ICE_CLK	I	Serial wired debugger clock pin
			ACMP1_P2	A	Analog comparator1 positive input pin
			I2C0_SCL	I/O	I2C0 clock pin
			SPI0_CLK	I/O	SPI0 serial clock pin
			SPI1_SS	I/O	SPI1 slave select pin
			UART0_TXD	O	Data transmitter output pin for UART0
19		20	PD.5	I/O	General purpose digital I/O pin.
			UART0_TXD	O	Data transmitter output pin for UART0
	18	21	HVIN	I	High voltage input-only pin[3].
			PD.6	I	General purpose digital input pin
			UART0_RXD	I	Data receiver input pin for UART0
	20	22	ULO	HO	Output for U-phase low-side MOSFET. Connect to U-phase low-side MOSFET gate.
	21	23	U	HI	U-Phase input. It should be connected to U-phase high-side MOSFET source and low-side FET drain.
	22	24	UHO	HO	Output for U-phase high-side MOSFET. Connect to U-phase high-side MOSFET gate.
	23	25	UB	HP	U-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and U.
	24	26	VLO	HO	Output for V-phase low-side MOSFET. Connect to V-phase low-side MOSFET gate.
	25	27	V	HI	V-Phase input. It should be connected to V-phase high-side MOSFET source and low-side FET drain
	26	28	VHO	HO	Output for V-phase high-side MOSFET. Connect to V-phase high-side MOSFET gate.
	7	29	VB	HP	V-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and V.
	28	30	WLO	HO	Output for W-phase low-side MOSFET. Connect to W-phase low-side MOSFET gate.

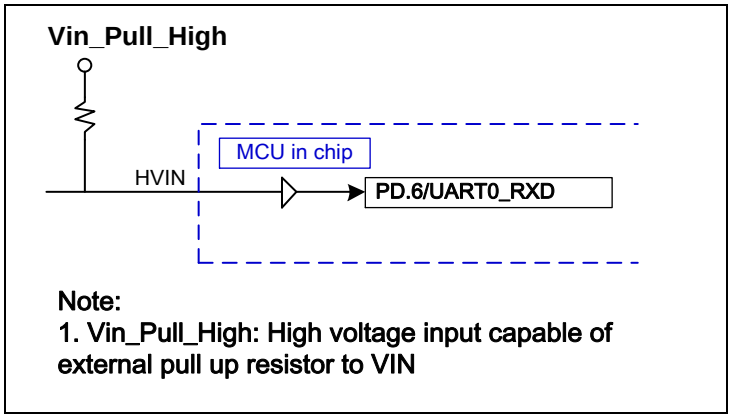
	1	31	W	HI	W-Phase input. It should be connected to high-side MOSFET source and low-side FET drain.
	2	32	WHO	HO	Output for W-phase high-side MOSFET. Connect to W-phase high-side MOSFET gate.
28	6	33	VSS	P	Ground pin for digital circuit
2	8				PD.6 connect to LV_O
26	10				PC.4 connect to RSTB
25	11				PWM0 connect to UHin
24	12				PWM1 connect to ULin
23	13				PWM2 connect to VHin
22	14				PWM3 connect to VLin
21	15				PWM4 connect to WHin
20	16				PWM5 connect to WLin
	9				LV_I of gate drive is no bonding
	17				DIR of gate driver is no bonding
27					LDO_CAP of NM1120 is no bonding
13,14	19				no connect

Table 3.3-1 QFN33 Pin Description

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

[3] Input-only with the following pull high capability.



3.3.2 Pin Description Overview in NM18107Y

Table of pin description in NM18107

	Alternative function , MFP_0 means setting MFP[3:0]=0x0, MFP_5 means MFP[3:0]=0x5																															
GPIO	ICE XTAL		ADC		PWM_BRAKE		ACMP0		ACMP1		PGA(OP)		TIMER		I2C		SPIO		SPI1		UART											
MFP_0	MFP_1		MFP_2		MFP_3		MFP_4		MFP_5		MFP_6		MFP_7		MFP_8		MFP_9		MFP_A		MFP_B											
GPA0	CLKO	O			EPWM_CH0	O									I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O										
GPA1					EPWM_CH1	O									I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I										
GPA2					EPWM_CH2	O									I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I										
GPA3					EPWM_CH3	O									I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O										
GPA4	XT_IN	A			EPWM_CH4	O																										
GPA5	XT_OUT	A			EPWM_CH5	O	ACMP0_O	O																								
GPB0			ADC0_CH0	A			ACMP0_P0	A					ICAP0	I																		
GPB1			ADC0_CH1	A			ACMP0_P1	A					ICAP1	I																		
GPB2			ADC0_CH2	A	BPWM_CH1	O	ACMP0_P2	A					ICAP2	I																		
GPB3									ACMP1_N	A	PGA_I	A	T0	I/O																		
GPB4			ADC1_CH0	A			ACMP0_N	A					T1	I/O																		
GPC0			ADC0_CH3	A	BPWM_CH0	O			ACMP1_P0	A					I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O										
GPC1			ADC0_CH4	A	STADC	I	ACMP0_P3	A	ACMP1_P1	A							SPI0_MOSI	I/O	SPI1_MISO	I/O												
GPC2			ADC1_CH2	A	PWM_BRAKE	I							CCAP	I	I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I										
GPC3									ACMP1_O	O	PGA_O	A					SPI0_CLK	I/O	SPI1_SS	I/O												
GPC4													ICAP0	I																		
nRESET																																
GPD1	ICE_CLK	I							ACMP1_P2	A					I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O										
GPD2	ICE_DAT	I/O	ADC1_CH1	A									CCAP	I	I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I										
GPD3					BPWM_CH1	O															UART1_TXD	O										
GPD4					BPWM_CH0	O															UART1_RXD	I										
GPD5																					UART0_TXD	O										
GPD6																					UART0_RXD	I										
VDD																																
VSS																																

: Function has been reserved for another usage.

Attention :

a. Some functions would be prohibition of use because of the limitation of pin definition in NM18107.

b. GPA0 ~ GPA5 should be set as EPWM0 ~ EPWM5, GPC4 should be set as GPIO.

4 BLOCK DIAGRAM

4.1 NM18107 Block Diagram

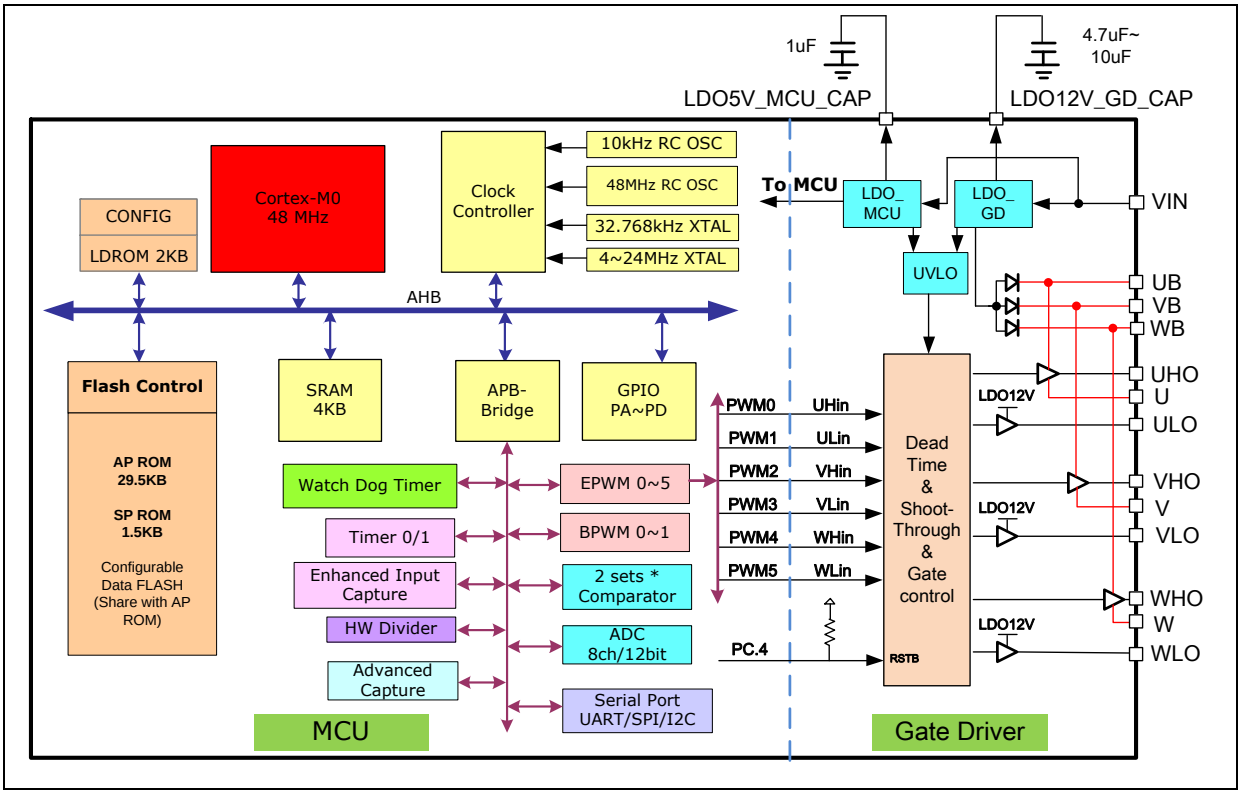


Figure 4.1-1 NM18107 Series Block Diagram

4.2 NM18107 Application Circuit

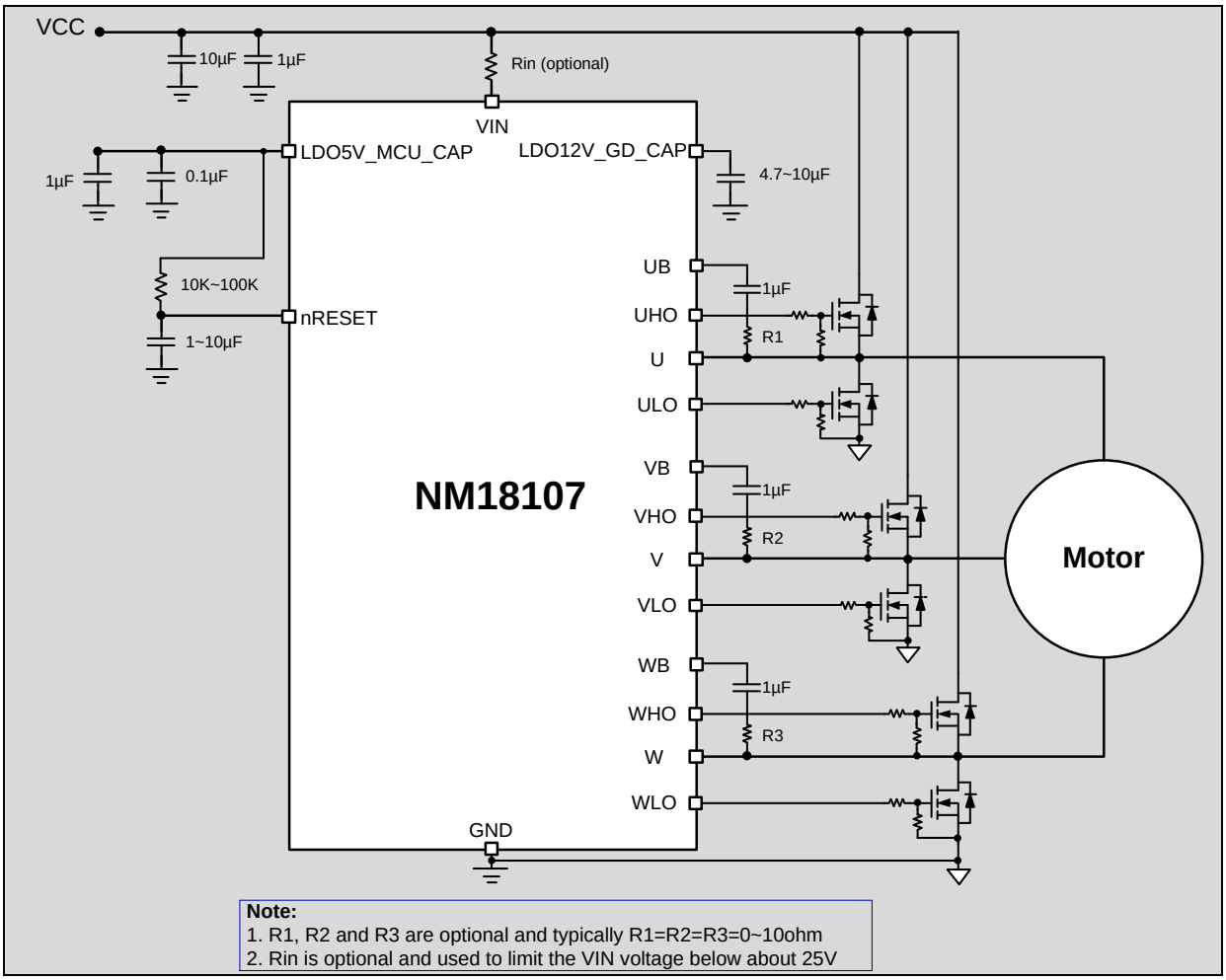


Figure 4.2-1 NM18107 Application Circuit

4.3 Built-in V_{BG} and LDO5V measurement

The NM18107 has built-in V_{BG} A/D conversion value (as pin LDO5V is forced at 5000mV) when chip is shipped from the factory. With the built-in V_{BG} A/D conversion value and the current V_{BG} A/D conversion value, user can calculated the current LDO5V with more accuracy. Note that the LDO5V is internally short to MCU VDD in NM18107Y series. The NM18107 also has built-in LDO5V value(unit is mV) at Vin=30V for user's reference when chip is shipped from the factory with room temperature at about 25℃.

The built-in V_{BG} A/D conversion value(stored in bit[31:16]) and built-in LDO5V value(stored in bit[15:0]) are read through FMC ISP Command = FMC_ISPCMD_READ_UID(0x04) and set the address Addr_Builtin_VBG_LDO5V = 0x00300120.

Example code to set FCM ISP command	Example code to read bilt-in V_{BG} A/D conversion value and LDO5V value

uint32_t FMC_Read_VBG_LDO5V(uint32_t u32Addr)
{
FMC->ISPCMD = FMC_ISPCMD_READ_UID;
FMC->ISPADDR = u32Addr;
FMC->ISPTRG = FMC_ISPTRG_ISPGO_Msk;
 	
while (FMC->ISPTRG & FMC_ISPTRG_ISPGO_Msk) ;
 	
return FMC->ISPDAT;
}
	int main()
	{
	SYS_UnlockReg(); /* Unlock protected registers */
	SYS_Init();
	SYS_LockReg(); /* Lock protected registers */
	
	SYS_UnlockReg();
	FMC_Open(); /* Enable FMC ISP function */
	u32ReadData1 = FMC_Read_VBG_LDO5V(Addr_Builtin_VBG_LDO5V);
	ADC_VBG_5V_Builtin = u32ReadData1 >> 16;
	LDO_5V_Builtin = u32ReadData1 & 0x0000FFFF;
	FMC_Close(); /* Disable FMC ISP function */
	SYS_LockReg();

5 NM18107 ELECTRICAL CHARACTERISTICS

The data is for reference only. Please refer to the TRM of NM1120 and the datasheet of NCT3612 for the detailed electrical characteristics.

5.1 NM1120 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 NM1120 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.1 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.1	-	5.5	V	V_{DD} = 2.1V ~ 5.5V up to 48 MHz			
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.14	1.20	1.26	V	V_{DD} = 3.0V ~ 5.5V, T_A = -40°C~105°C			
I_{DD5}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	9.7	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD6}		-	7.4	-	mA	5.5V	X	48 MHz	X
I_{DD7}		-	9.7	-	mA	3V	X	48 MHz	V
I_{DD8}		-	7.4	-	mA	3V	X	48 MHz	X
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD2}		-	4.4	-	mA	5.5V	24 MHz	X	X
I_{DD3}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD4}		-	4.4	-	mA	3V	24 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.7	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD10}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD11}		-	3.7	-	mA	3V	16 MHz	X	V
I_{DD12}		-	3.1	-	mA	3V	16 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	2.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD10}		-	2.3	-	mA	5.5V	12 MHz	X	X
I_{DD11}		-	2.8	-	mA	3V	12 MHz	X	V
I_{DD12}		-	2.3	-	mA	3V	12 MHz	X	X

I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.2	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD14}		-	1.0	-	mA	5.5V	4 MHz	X	X
I_{DD15}		-	1.2	-	mA	3V	4 MHz	X	V
I_{DD16}		-	1.0	-	mA	3V	4 MHz	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	291.7	-	µA	V_{DD}	**LXT	LIRC	All Digital Modules
						5.5V	32 kHz	V	V[1]
I_{DD18}		-	290.7	-	µA	5.5V	32 kHz	V	X
I_{DD19}		-	280.8	-	µA	3V	32 kHz	V	V[1]
I_{DD20}		-	281.4	-	µA	3V	32 kHz	V	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	248.0	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	10 kHz	V[2]
I_{DD18}		-	247.7	-	µA	5.5V	X	10 kHz	X
I_{DD19}		-	237.9	-	µA	3V	X	10 kHz	V[2]
I_{DD20}		-	237.5	-	µA	3V	X	10 kHz	X
I_{IDLE5}	Operating Current Idle Mode HCLK= 48 MHz	-	4.9	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE6}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE7}		-	4.9	-	mA	3V	X	V	V
I_{IDLE8}		-	2.6	-	mA	3V	X	V	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 24 MHz	-	2.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE2}		-	1.9	-	mA	5.5V	24 MHz	X	X
I_{IDLE3}		-	2.8	-	mA	3V	24 MHz	X	V
I_{IDLE4}		-	1.9	-	mA	3V	24 MHz	X	X
I_{IDLE9}	Operating Current Idle Mode	-	2.0	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules

	HCLK = 16 MHz					5.5V	V	X	V
I_{IDLE10}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE11}		-	2.0	-	mA	3V	V	X	V
I_{IDLE12}		-	1.4	-	mA	3V	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 12 MHz	-	1.5	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.0	-	mA	5.5V	V	X	X
I_{IDLE11}		-	1.5	-	mA	3V	V	X	V
I_{IDLE12}		-	1.0	-	mA	3V	V	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	0.8	-	mA	V_{DD}	**HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE14}		-	0.6	-	mA	5.5V	V	X	X
I_{IDLE15}		-	0.7	-	mA	3V	V	X	V
I_{IDLE16}		-	0.6	-	mA	3V	V	X	X
I_{DD17}	Operating Current Idle Mode HCLK = 32 kHz	-	274.3	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{DD18}		-	273.0	-	µA	5.5V	X	V	X
I_{DD19}		-	265.0	-	µA	3V	X	V	V[1]
I_{DD20}		-	263.9	-	µA	3V	X	V	X
I_{DD17}	Operating Current Idle Mode HCLK = 10 kHz	-	232.6	-	µA	V_{DD}	**HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{DD18}		-	232.2	-	µA	5.5V	X	V	X
I_{DD19}		-	222.5	-	µA	3V	X	V	V[2]
I_{DD20}		-	222.1	-	µA	3V	X	V	X
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1.9	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD2}		-	1.7	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current PA/PB/PC/PD	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			

V_{IL1}	Input Low Voltage PA/PB/PC/PD (TTL Input)	-0.3	1.33		V	V_{DD} = 5.5 V
		-0.3	1			V_{DD} = 3.3 V
V_{IH1}	Input High Voltage PA/PB/PC/PD (TTL Input)		1.47	V_{DD} + 0.3	V	V_{DD} = 5.5 V
			1.08	V_{DD} + 0.3		V_{DD} = 3.3 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.1 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), PA/PB/PC/PD	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), PA/PB/PC/PD	$0.7V_{DD}$	-	-	V	-
I_{IL}	Logic 0 Input Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-63.65		μA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current PA/PB/PC/PD	-	-566.7	-	μA	V_{DD} = 5.5 V
I_{SR11}	Source Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-372	-	μA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR12}		-	-76.8	-	μA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR13}		-	-37.3	-	μA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SR21}	Source Current PA/PB/PC/PD (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR22}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR23}		-	-2	-	mA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SK11}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK12}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.1 V, V_{IN} = 0.4 V

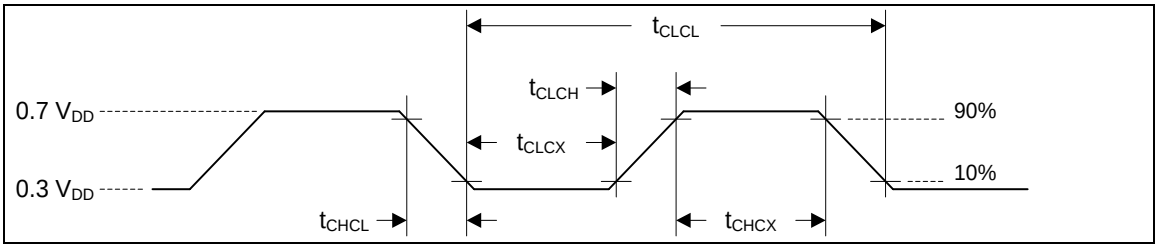
Notes:

1. Only enable modules which support 32 kHz LIRC clock source
2. Only enable modules which support 10 kHz LIRC clock source
3. Guaranteed by design, not test in production.

**: The function has been reserved in NM18107.

5.3 NM1120 AC Electrical Characteristics

5.3.1 **External Input Clock (function has been reserved in NM18107)



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

5.3.2 **External 4~24 MHz High Speed Crystal (HXT) (function has been reserved in NM18107)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.1	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	414	-	uA	12 MHz, V_{DD} = 5.5V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

5.3.3 **Typical Crystal Application Circuits (function has been reserved in NM18107)

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

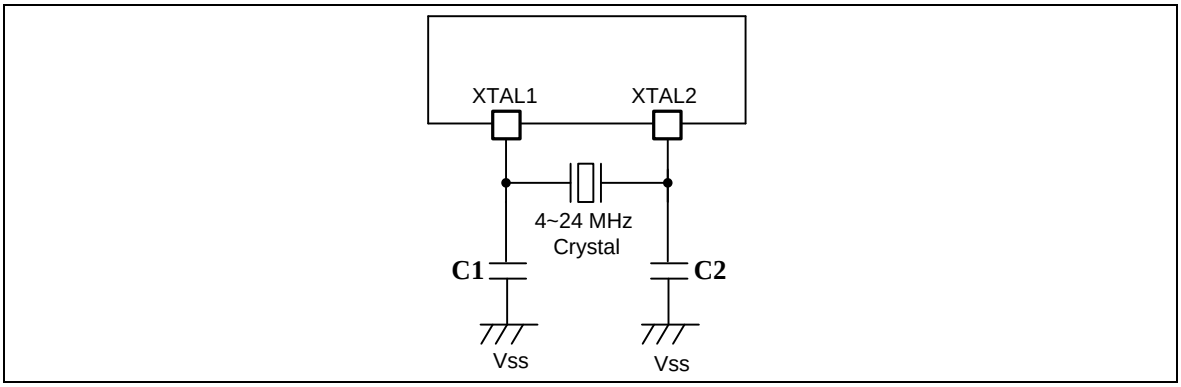


Figure 5-1 NM1120 Typical Crystal Application Circuit

5.3.4 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
			2%		%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	1090	-	μA	T_A = 25 ℃,V_{DD} = 5 V

5.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-50[1]	-	+50[1]	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃
I_{LRC}	Operating Current	-	0.4	-	μA	T_A = 25 ℃,V_{DD} = 5 V

Note1: These parameters are characterized but not tested.

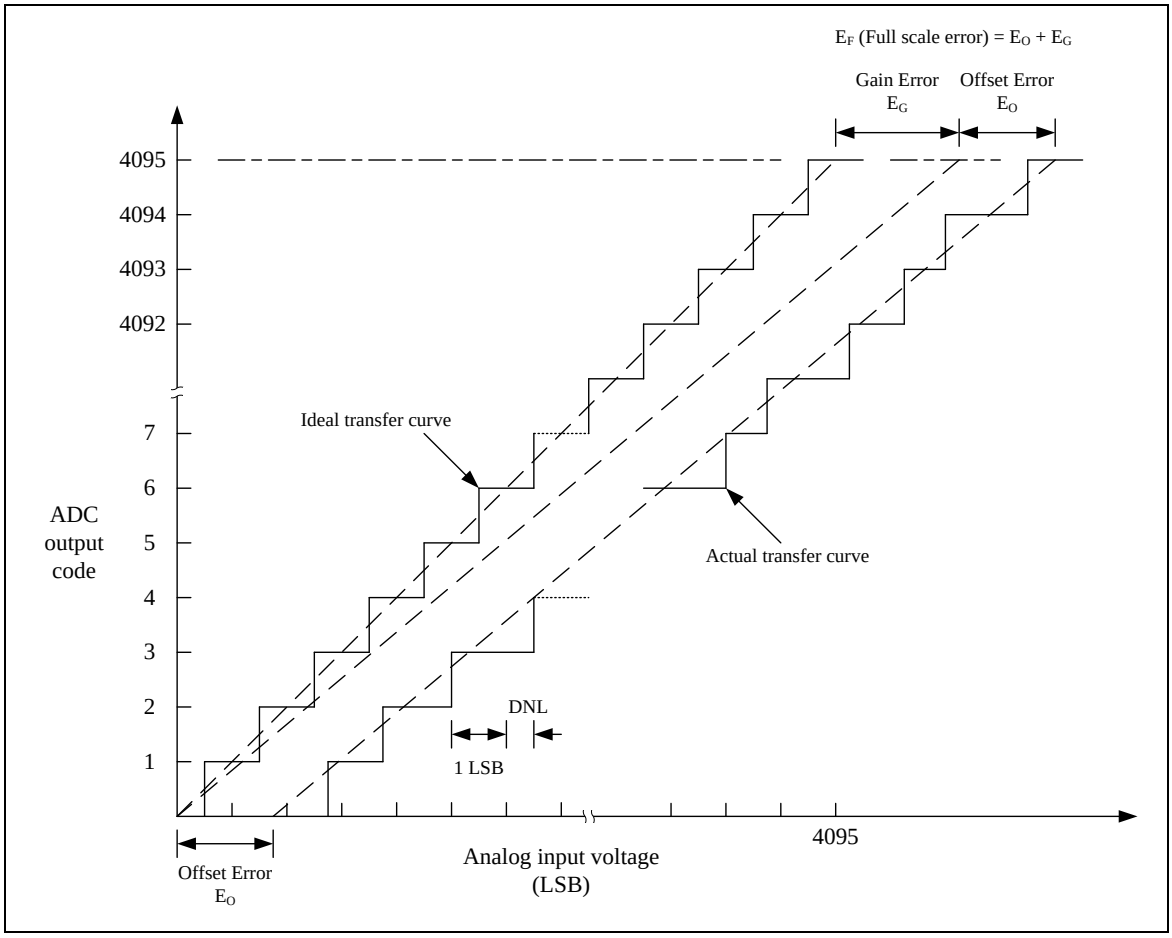
5.4 NM1120 Analog Characteristics

5.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency		12	16	MHz	V_{DD} = 3.0 ~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			1/F_{ADC}	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]	-	1000	1500	ns	V_{DD} = 3.0~5.5 V
V_{DD}	Supply Voltage	3.0	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-
R_{IN}	Input Load[2]	-	2.5	-	kΩ	-

Note:

1. ADC voltage reference is same with V_{DD}.
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of CIN is less than about 10% of typical value and the variation of RIN is less about 20% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 1000ns at V_{DD} = 5V.



5.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.1	-	5.5	V	-
V_{LDO}	Output Voltage		1.5		V	-
T_A	Temperature	-40	25	105	℃	

Notes:
It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

5.4.3 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	100	-	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Detector	4.2	4.3	4.4	V	BOV_VL [2:0] = 7
		3.9	4.0	4.1	V	BOV_VL [2:0] = 6
		3.6	3.7	3.8	V	BOV_VL [2:0] = 5

		2.9	3.0	3.1	V	BOV_VL [2:0] = 4
		2.6	2.7	2.8	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

5.4.4 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage		1.75		V	-

5.4.5 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	47		μA	V_{DD}=5.5V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	225	-	ns	
V_{HYS}	Hysteresis	-	10	-	mV	ACMPPHYSEN = 01
V_{HYS}	Hysteresis	-	90	-	mV	ACMPPHYSEN = 10
T_{STB}	Stable time	-	1.06	-	μs	

Notes:
Guaranteed by design, not test in production.

5.4.6 PGA

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
	Operation voltage range	2.5	3.3	5.5	V	
	Operating Current			5	mA	VDD=5V, T=125℃
	Operating Temperature	-40	25	125	℃	
	Input Offset Voltage	-9.5	-3	9.5	mV	TA= -40~105 ℃,VDD=5V VCM=VDD/2, Gain=2
	Output Swing	0.1		VDD - 0.1	V	
	PGA gain accuracy	-1		+1	%	
	Input Common Mode Range	0		VDD - 1.5	V	
	DC Gain	50	80		dB	
	Unity Gain Frequency	7		8.2	MHz	VDD=5V
	Phase Margin	50°			°	
	PSRR+	49	90		dB	VDD=5V
	CMRR	69	90		dB	VDD=5V
	Slew Rate+		6.0	7.5	V/us	VDD=5V, RLoad=1.3K, CLoad=100p
	Wake Up Time			20	us	
	Maximum output voltage swing from rail		40		mV	VDD=5.5V, RL=50K
			200		mV	VDD=5.5V, RL=10K

Notes:
Guaranteed by design, not test in production.

5.4.7 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1,]	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	725	-	mV	TA = 0 ℃

Note:

1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

5.5 NCT3612 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VCC	Input supply voltage.	-0.3 to 40	V
VR12V	Linear regulator voltage output (LDO12V_GD_CAP) for gate driver.	-0.3 to 15	V
VB	High-side floating supply absolute voltage.	-0.3 to VS+VR12V	V
VS	High-side floating supply offset voltage.	-2 to VCC+2	V
HO	High-side floating output voltage.	VS-0.3 to VB+0.3	V
LO	Low-side output voltage.	-0.3 to VR12V+0.3	V
Other pins	5VOUT (LDO5V_MCU_CAP), RSTB, HIN, LIN.	-0.3 to 6	V
θ_{JA}	Thermal Resistance,	40	℃/W
θ_{JC}	Thermal Resistance,	10	℃/W
θ_{STG}	Storage Temperature	-50 to 150	℃
θ_{J}	Junction Temperature	150	℃
ESD Rating	Human Body Mode(all pins)	±2	KV
	Charge Device Mode	±500	V
	Latch-up	±100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.6 NCT3612 Recommended Operating Conditions

PARAMETER	RATING	UNIT
Low side and logic fixed supply voltage	8 to 25	V
LDO5V Supply Output Current	20	mA
Operating Temperature	-40 to 105	℃
Junction Temperature	-40 to 125	℃

Note: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

5.7 NCT3612 DC Electrical Characteristics

(VCC= 35V, TA = TJ = 25° C, unless otherwise specified)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Input supply voltage	VCC		8	---	35	V
VCC UVLO turn-on threshold	UVLO+		---	4	---	V
VCC UVLO turn-off threshold	UVLO-		---	3.6	---	V
VCC UVLO threshold hysteresis			---	0.4	---	V
VCC operation current		PWM=20KHz, Duty=50%	---	20	---	mA
VCC sleep mode current		RSTB=Low	---	100		uA
Gate Driver Output						
Souring peak current	I_{O+}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.25	---	A
Sinking peak current	I_{O-}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.5	---	A
Turn-on propagation delay	t_{on}	VCC=35，C_L=1nF	---	50	---	nS
Turn-off propagation delay	t_{off}	VCC=35，C_L=1nF	---	50	---	nS
Turn-on rise time	t_r	C_L=1nF	---	50	---	nS
Turn-off fall time	t_f	C_L=1nF	---	30	---	nS
PWM delay matching	MT		---	50	---	nS
Pull low resistance	R_o		---	100	---	KΩ
Logic Input						
Voltage high Level	VIH		2.4	---	---	V
Voltage low Level	VIL		---	---	0.8	V
HIN/LIN pull low Resistance			---	100	---	KΩ
Internal 5V/12V regulator						
5V output voltage	$5V_{OUT}$		4.75	5	5.25	V
5V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
12V output voltage	V_{R12V}		---	12	---	V
12V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
Bootstrapped Power Supply Section						

VS_U/V/W leakage current		VB_U/V/W=VS_U/V/W=40V	---	---	50	uA
Bootstrap diode ON resistance	R_{BD}		---	150	---	Ω
Thermal Protection						
Thermal shutdown temperature	TSD		---	165	---	℃
Thermal shutdown hysteresis	TSDHYS		---	50	---	℃

5.8 NCT3612 DC Electrical Characteristics

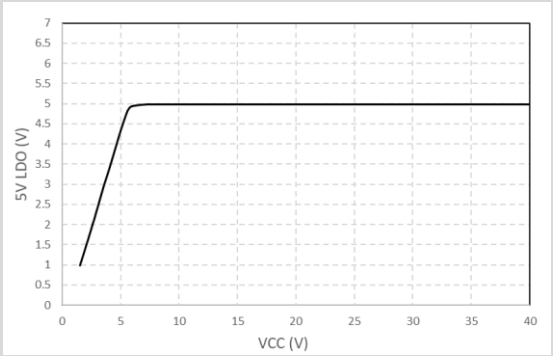


Figure 5.8-1 VCC vs. 5V LDO Voltage

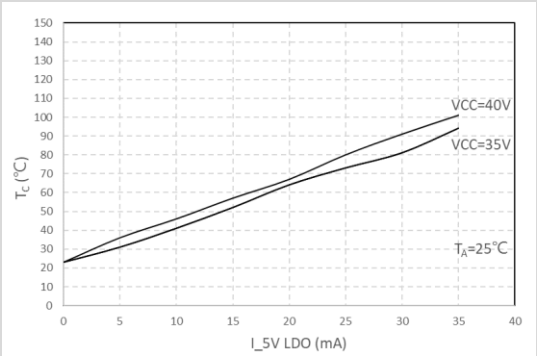


Figure 5.8-2 5V LDO Current vs. IC temperature

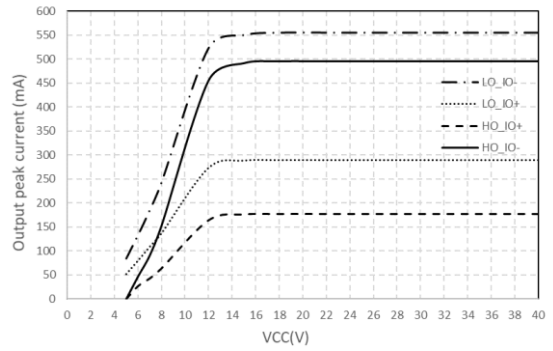


Figure 5.8-3 VCC vs. Output peak current

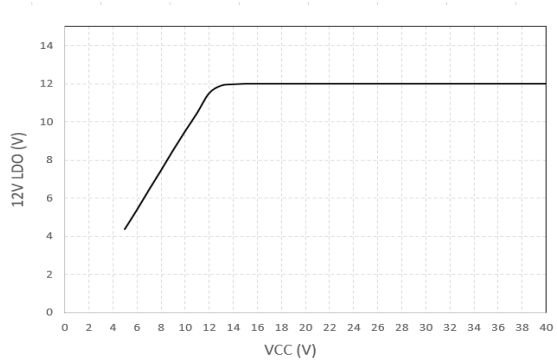


Figure 5.8-4. VCC vs. 12VLDO Voltage

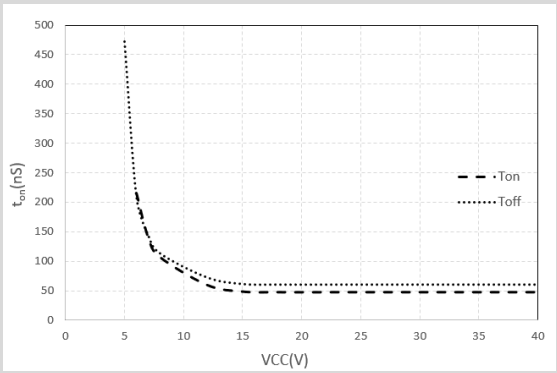


Figure 5.8-5 VCC vs. Ton/Toff propagation delay

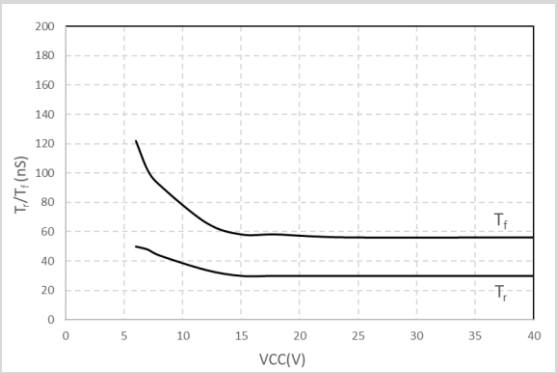
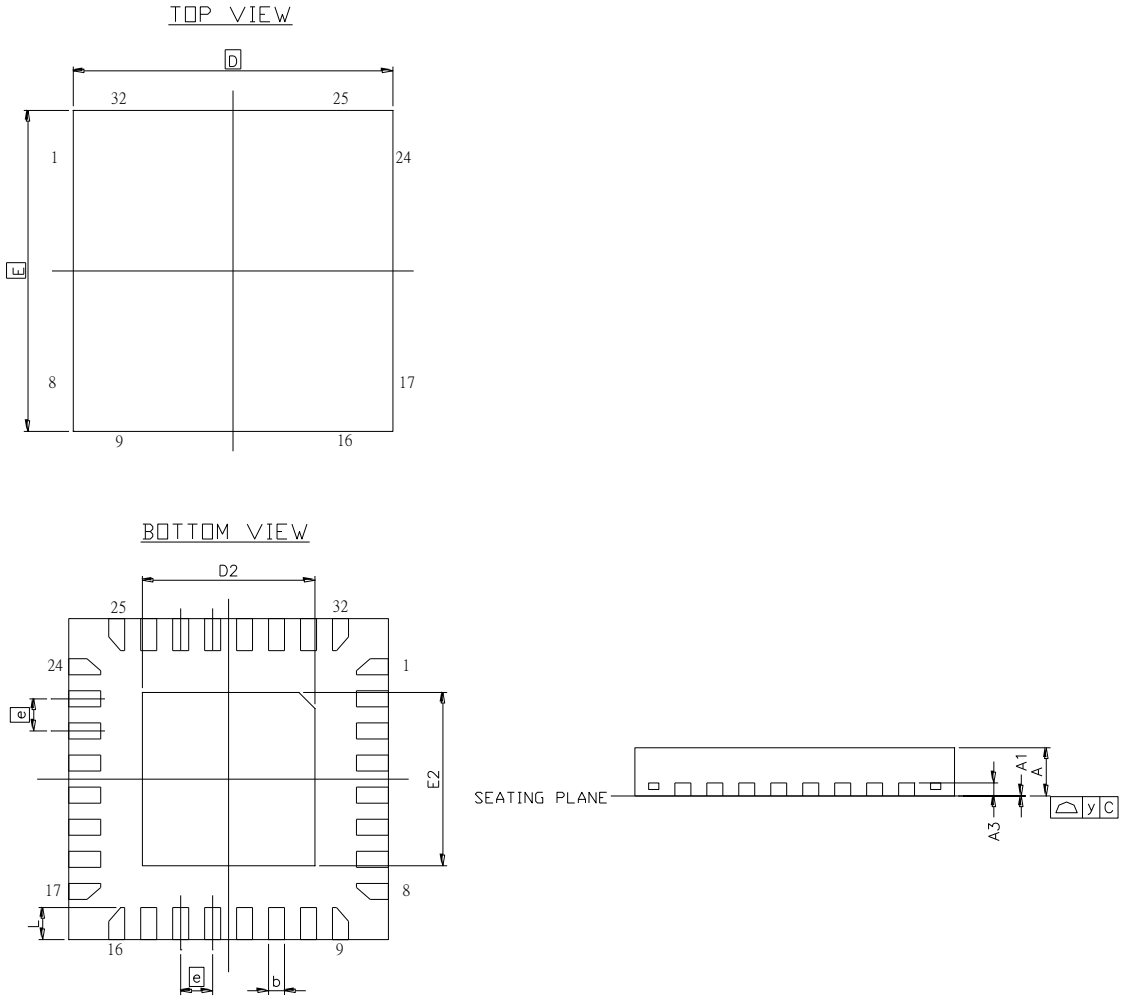


Figure 5.8-6 VCC vs. Turn-on/off rise time

6 PACKAGE DIMENSIONS

6.1 33-pin QFN (5 mm x 5 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		
D2	3.20	3.40	3.60	0.124	0.138	0.142
E2	3.20	3.40	3.60	0.124	0.138	0.142

7 ORDERING INFORMATION

Part Number	Supplied As	Package Type	Operating Temperature
NM18107Y	4000 units/ T&R	QFN33, Green Package	Commercial, -40℃~105℃

8 REVISION HISTORY

Revision	Date	Description
0.01	February 07, 2020	1. Preliminary version 0.01
0.02	April 06, 2020	1. Update the content of section 5.4.6 PGA
0.02	June 19, 2020	1. Modify the Figure 4.1-1 NM18107 Series Block Diagram
0.02	November 08, 2022	1. Add compliance statement of International Environmental Regulations.