ARM Cortex™-M0

32-BIT MICROCONTROLLER

NM18202 Series Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NM18202 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and monolithic half-bridge gate driver for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The MCU of NM18202 series can run up to 48 MHz and offers 17.5K-bytes embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM. Many system level peripheral functions, such as I/O Port, Timer, UART, I^2C, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM18202 series in order to reduce component count, board space and system cost. These useful functions make the NM18202 series powerful for a wide range of motor driver applications.

The power supply input of NM18202 is up to 35V. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component.

Additionally, the NM18202 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM18202 is the combination of MCU NM1200 and Gate Driver NCT3612. User may refer to the TRM of NM1200 and the datasheet of NCT3612 for the detailed specification. The NM1200 BSP is also for NM18202 software developing.

2 FEATURES

- Recommended operation Supply Voltage VIN Range from 8 to 35V
- Gate Driver
  - Programmable enable/disable gate driver by MCU I/O of PC.4
  - 8 ~ 35V Operate Supply Voltage Range
  - 250mA Source & 500mA Sink Gate Drive Current Capability @VIN > 20V
  - Integrated 2 LDO
    - 5V, 35mA, LDO Output for MCU power supply(Note1)
    - 12V, LDO for internal use
  - Sleep Mode Support (< 100uA)
  - Integrated bootstrap diode
  - 3 or 6 PWM Input Mode Supported
  - Direction Control for Motor Forward / Reverse sequence by PWM input signal
  - Protection:
    - UVLO (Under Voltage Lockout)
    - Thermal Shutdown Protection (typically @165℃)
- MCU Core
  - ARM® Cortex™-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- Memory
  - 17.5 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control

- 48 MHz internal oscillator (HIRC) (±1% accuracy at 25°C, 5V)
  - Dynamically calibrating the HIRC OSC to 48 MHz ±2% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
- 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up

- Timer
  - Supports external capture pin (T1EX) for interval measurement
  - Support advanced capture function(P3.0) can continuous capture 4 edge on one signal
  - Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous operation modes
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Provides event counter function
  - Supports wake-up from Idle or Power-down mode
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Support Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Supports rising, falling, central, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
  - Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF

H	H	OFF	OFF

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- UART (Universal Asynchronous Receiver/Transmitters)
  - Two UART devices
  - Buffered receiver and transmitter, each with 16-byte FIFO for first UART (UART0), each with 4-byte FIFO for second UART (UART1)
  - Programmable baud-rate generator up to 1/16 system clock
- I^2C (For QFN-48 only)
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports multiple address recognition (four slave addresses with mask option)
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 500K SPS
  - Up to 7-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Support sequential mode to continuous conversion 2 channel
- Analog Comparator
  - one analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- I/O Port
  - Up to 10 general-purpose I/O (GPIO) pins for TSSOP-28 package
  - Up to 23 general-purpose I/O (GPIO) pins for QFN-48 package
  - Four I/O modes:
    - Input-only with high impendence

- Push-pull output
- Open-drain output
- Quasi-bidirectional

- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink I/O mode
- Configurable default I/O mode of all pins after POR

- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels:
    4.4V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V/1.7V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Packages:
  - Green package (RoHS)
  - 48-pin QFN (7x7), 28-pin TSSOP

Note:

1. Higher LDO output current causes the higher IC temperature. Refer to section 5.9 NCT3612 DC Electrical Characteristics

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NM18202 Series Product Selection Guide

Part No.	AP ROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer 32-bit	UART/ I^2C	Comp.	ADC	ISP ICP IAP	IRC 48MHz	Package
NM18202S	17.5 KB	2 KB	Configurable	2 KB	up to 10	2x 32-bit	2/0	2	7 x10-bit	v	v	TSSOP 28pin
NM18202Y	17.5 KB	2 KB	Configurable	2 KB	up to 23	2x 32-bit	2/1	2	12 x10-bit	v	v	QFN 48pin 7x7mm

Table 3.1-1 NM18202 Series Product Selection Guide

3.2 PIN CONFIGURATION

TSSOP 28-pin

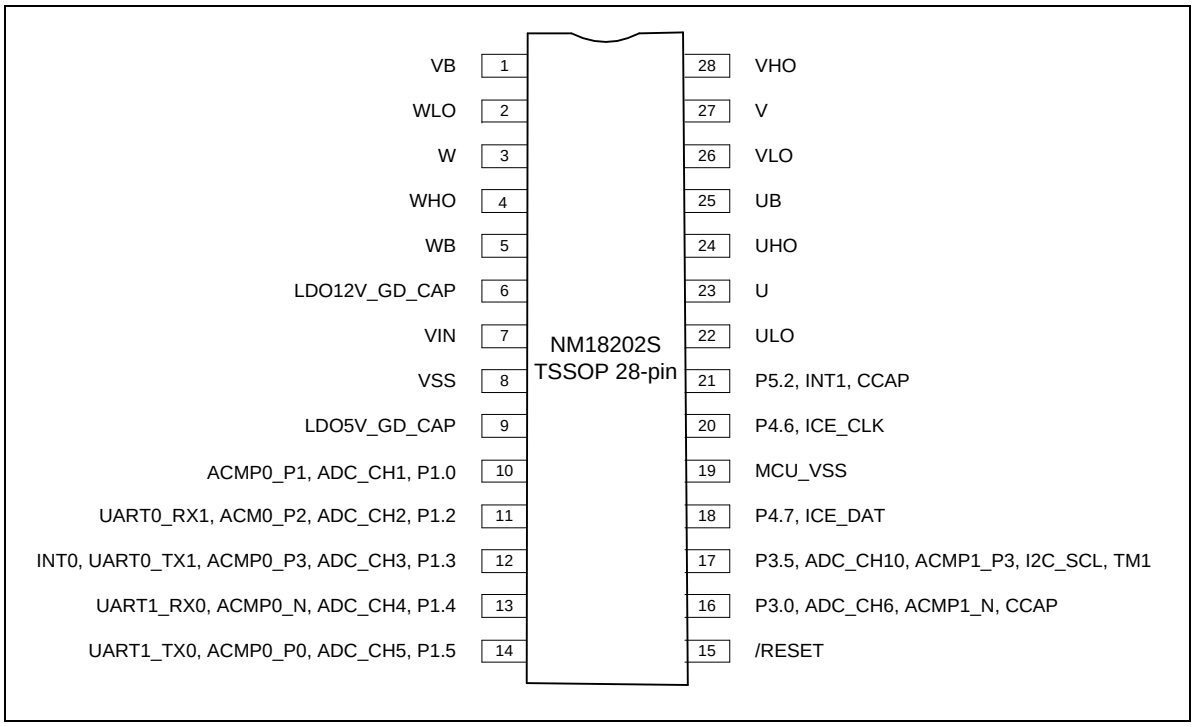


Figure 3.2-1 NM18202S TSSOP 28-pin Diagram

QFN 48-pin

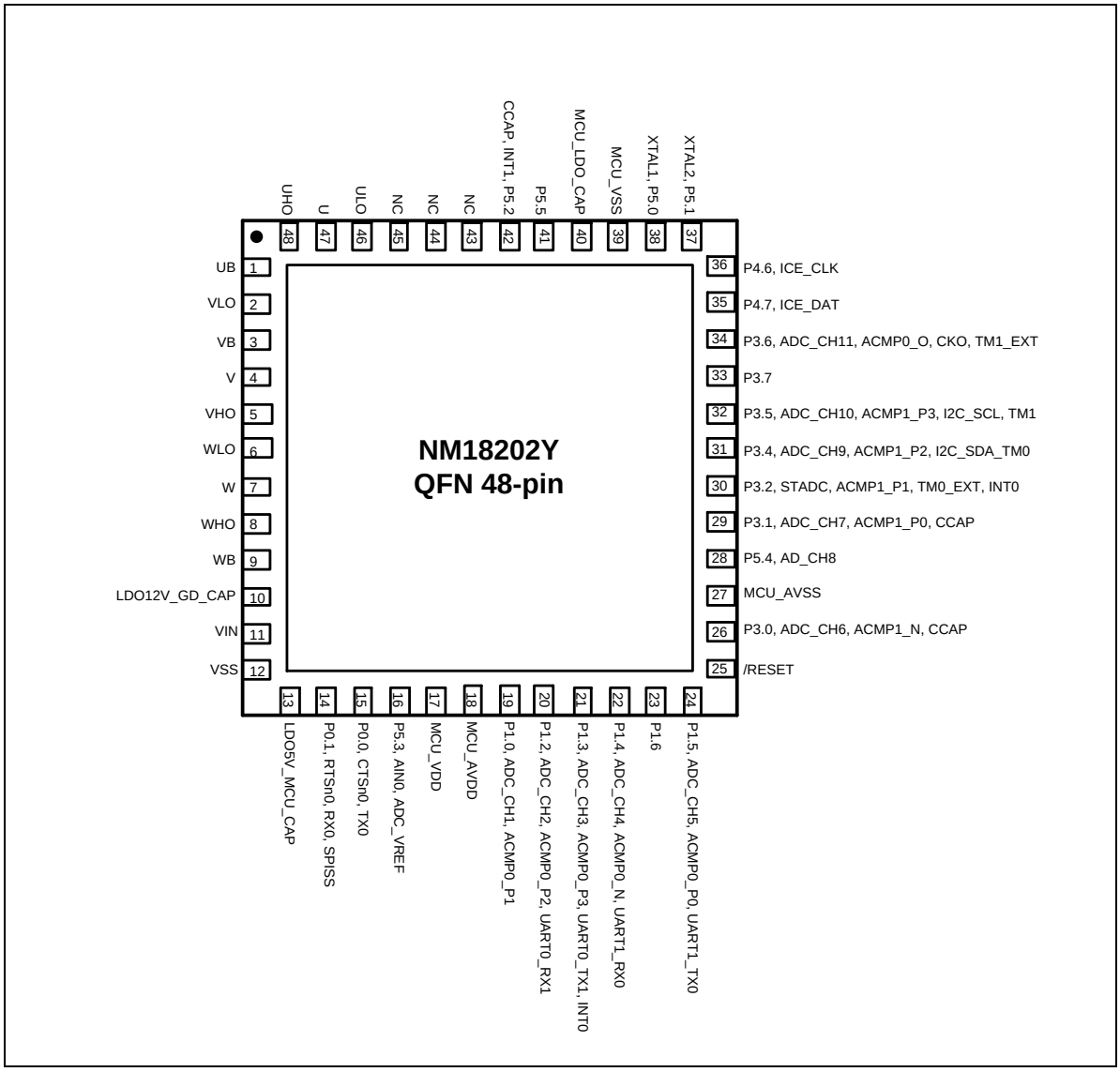


Figure 3.2-2 NM18202Y QFN 48-pin Diagram

3.3 Pin Description of NM18202 (QFN 48-pin)

NM18202 QFN 48-pin 7x7		Pin Name	Pin Type	Description
1	25	UB	HP	U-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and U.
2	26	VLO	HO	Output for V-phase low-side MOSFET. Connect to V-phase low-side MOSFET gate.
3	1	VB	HP	V-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and V.
4	27	V	HI	V-Phase input. It should be connected to V-phase high-side MOSFET source and low-side FET drain
5	28	VHO	HO	Output for V-phase high-side MOSFET. Connect to V-phase high-side MOSFET gate.
6	2	WLO	HO	Output for W-phase low-side MOSFET. Connect to W-phase low-side MOSFET gate.
7	3	W	HI	W-Phase input. It should be connected to high-side MOSFET source and low-side FET drain.
8	4	WHO	HO	Output for W-phase high-side MOSFET. Connect to W-phase high-side MOSFET gate.
9	5	WB	HP	W-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and W.
10	6	LDO12V_GD_CAP	P	12V LDO OUT for gate driver(VR12V). Recommend connect an at least 4.7uF capacitor to GND.
11	7	VIN	HP	Power supply for internal control circuit. Recommend connect a capacitor to GND to stable the input power.
12	8	VSS	P	Ground pin for digital circuit
13	9	LDO5V_MCU_CAP	P	5V LDO OUT for MCU(5VOUT). Recommend connect 1uF and 0.1uF capacitors to GND.
14		P0.1	I/O	General purpose digital I/O pin
		nRTS	O	UART0 RTS pin
		UART0_RX0	I	UART0 data receiver input pin
		SPI_SS	I/O	SPI slave select pin
15		P0.0	I/O	General purpose digital I/O pin
		nCTS	I	UART0 CTS pin
		UART0_TX0	O	UART0 transmitter output pin
16		P5.3	I/O	General purpose digital I/O pin
		ADC_CH0	AI	ADC analog input pin
		ADC VREF	AI	External voltage reference of ADC
17		MCU_VDD	P	Power supply for digital circuit
18		MCU_AVDD	P	Power supply for analog circuit

19	10	**P1.0**	**I/O**	General purpose digital I/O pin
		ADC_CH1	**AI**	ADC analog input pin
		ACMP0_P1	**AI**	Analog comparator positive input pin
20		**P1.2**	**I/O**	General purpose digital I/O pin
		ADC_CH2	**AI**	ADC analog input pin
		UART0_RX1	**I**	UART0 data receiver input pin
		ACMP0_P2	**AI**	Analog comparator positive input pin
21	11	**P1.3**	**I/O**	General purpose digital I/O pin
		ADC_CH3	**AI**	ADC analog input pin
		UART0_TX1	**O**	UART0 transmitter output pin
		ACMP0_P3	**AI**	Analog comparator positive input pin
		INT0	**I**	External interrupt 0 input pin
22	13	**P1.4**	**I/O**	General purpose digital I/O pin
		ADC_CH4	**I/O**	ADC analog input pin
		ACMP0_N	**AI**	Analog comparator negative input pin
		UART1_RX0	**I**	UART1 data receiver input pin
23		**P1.6**	**I/O**	General purpose digital I/O pin
24	14	**P1.5**	**I/O**	General purpose digital I/O pin
		ADC_CH5	**AI**	ADC analog input pin
		ACMP0_P0	**AI**	Analog comparator positive input pin
		UART1_TX0	**O**	UART1 transmitter output pin
25	15	**/RESET**	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A “Low” on this pin for 768 clock counter of Internal HIRC while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	16	**P3.0**	**I/O**	General purpose digital I/O pin
		ADC_CH6	**AI**	ADC analog input pin
		ACMP1_N	**AI**	Analog comparator negative input pin
		CCAP	**I**	Continuous Capture input pin
27		**MCU_AVSS**	**P**	Ground pin for digital circuit
28		**P5.4**	**I/O**	General purpose digital I/O pin
		ADC_CH8	**AI**	ADC analog input pin
		P3.1	**I/O**	General purpose digital I/O pin

29		**ADC_CH7**	**AI**	ADC analog input pin
		ACMP1_P0	**AI**	Analog comparator positive input pin
		CCAP	**I**	Continuous Capture input pin
30		**P3.2**	**I/O**	General purpose digital I/O pin
		INT0	**I**	External interrupt 0 input pin
		STADC	**I**	ADC external trigger input pin
		TM0_EXT	**I**	Timer 0 external capture/reset trigger input pin
		ACMP1_P1	**AI**	Analog comparator positive input pin
31		**P3.4**	**I/O**	General purpose digital I/O pin
		TM0	**I/O**	Timer 0 external event counter input pin
		I2C_SDA	**I/O**	I2C data I/O pin
		ACMP1_P2	**AI**	Analog comparator positive input pin
		ADC_CH9	**AI**	ADC analog input pin
32	**17**	**P3.5**	**I/O**	General purpose digital I/O pin
		TM1	**I/O**	Timer 1 external event counter input pin
		I2C_SCL	**I/O**	I2C clock I/O pin
		ACMP1_P3	**AI**	Analog comparator positive input pin
		ADC_CH10	**AI**	ADC analog input pin
33		**P3.7**	**I/O**	General purpose digital I/O pin
34		**P3.6**	**I/O**	General purpose digital I/O pin
		ACMP0_O	**O**	Analog comparator output pin
		CKO	**O**	Frequency divider output pin
		TM1_EXT	**I**	Timer 1 external capture/reset trigger input pin
		ADC_CH11	**AI**	ADC analog input pin
35	**18**	**P4.7**	**I/O**	General purpose digital I/O pin
		ICE_DAT	**I/O**	Serial wired debugger data pin
36	**20**	**P4.6**	**I/O**	General purpose digital I/O pin
		ICE_CLK	**I**	Serial wired debugger clock pin
37		**P5.1**	**I/O**	General purpose digital I/O pin
		XTAL2	**O**	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
38		**P5.0**	**I/O**	General purpose digital I/O pin

		XTAL1	**I**	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
39	**19**	**MCU_VSS**	**P**	Ground pin for digital circuit
40		**MCU_LDO_CAP**	**P**	MCU LDO output pin. Recommend connect a 1uF capacitor to GND.
41		**P5.5**	**I/O**	General purpose digital I/O pin
42	**21**	**P5.2**	**I/O**	General purpose digital I/O pin
		INT1	**I**	External interrupt 1 input pin
		CCAP	**I**	Continuous Capture input pin
43		**NC**		Not connected
44		**NC**		Not connected
45		**NC**		Not connected
46	**22**	**ULO**	**HO**	Output for U-phase low-side MOSFET. Connect to U-phase low-side MOSFET gate.
47	**23**	**U**	**HI**	U-Phase input. It should be connected to U-phase high-side MOSFET source and low-side FET drain.
48	**24**	**UHO**	**HO**	Output for U-phase high-side MOSFET. Connect to U-phase high-side MOSFET gate.

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

4 BLOCK DIAGRAM

4.1 NM18202 Block Diagram

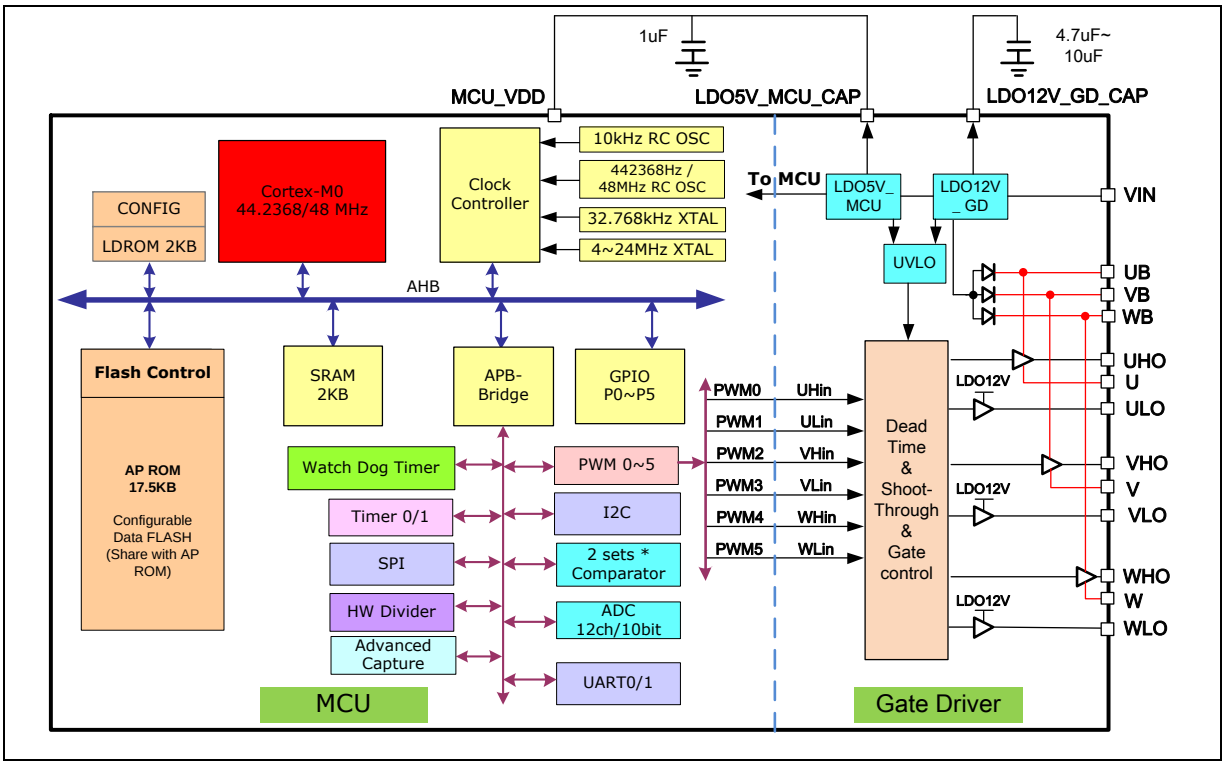


Figure 4.1-1 NM18202 Series Block Diagram

4.2 NM18202 Application Circuit

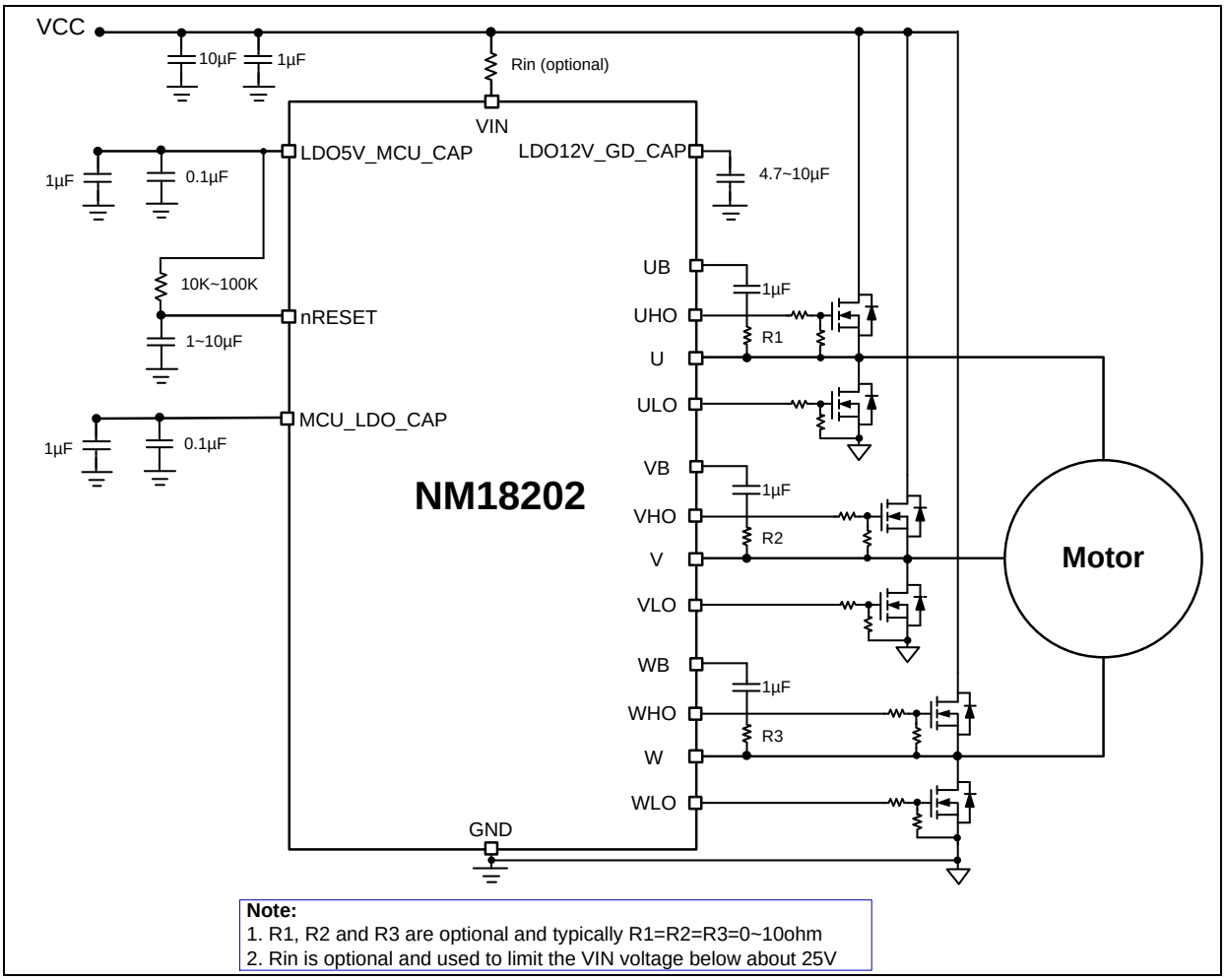


Figure 4.2-1 NM18202 Application Circuit

4.3 Built-in V_{BG} and LDO5V measurement

The NM18202 has built-in V_{BG} A/D conversion value (as pin LDO5V is forced at 5000mV) when chip is shipped from the factory. With the built-in V_{BG} A/D conversion value and the current V_{BG} A/D conversion value, user can calculated the current LDO5V with more accuracy. Note that the LDO5V is internally short to MCU VDD in NM18202Y series. The NM18202 also has built-in LDO5V value(unit is mV) at Vin=30V for user's reference when chip is shipped from the factory with room temperature at about 25℃.

The built-in V_{BG} A/D conversion value(stored in bit[15:0]) and built-in LDO5V value(stored in bit[31:16]) are read through FMC ISP Command = FMC_ISPCMD_READ_UID(0x04) and set the address Addr_Builtin_VBG_LDO5V = 0x00300130.

Example code to set FCM ISP command	Example code to read bilt-in V_{BG} A/D conversion value and LDO5V value

uint32_t FMC_Read_VBG_LDO5V(uint32_t u32Addr)
{
FMC->ISPCMD = FMC_ISPCMD_READ_UID;
FMC->ISPADDR = u32Addr;
FMC->ISPTRG = FMC_ISPTRG_ISPGO_Msk;
 	
while (FMC->ISPTRG & FMC_ISPTRG_ISPGO_Msk) ;
 	
return FMC->ISPDAT;
}
	int main()
	{
	SYS_UnlockReg(); /* Unlock protected registers */
	SYS_Init();
	SYS_LockReg(); /* Lock protected registers */
	
	SYS_UnlockReg();
	FMC_Open(); /* Enable FMC ISP function */
	u32ReadData1 = FMC_Read_VBG_LDO5V(Addr_Builtin_VBG_LDO5V);
	LDO_5V_Builtin = u32ReadData1 >> 16;
	ADC_VBG_5V_Builtin = u32ReadData1 & 0x0000FFFF;
	FMC_Close(); /* Disable FMC ISP function */
	SYS_LockReg();

5 NM18202 ELECTRICAL CHARACTERISTICS

The data is for reference. Please refer to the TRM of NM1200 and the datasheet of NCT3612 for the electrical characteristics.

5.1 NM1200 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDD – VSS	DC Power Supply	-0.3	+7.0	V
VIN	Input Voltage	VSS - 0.3	VDD + 0.3	V
1/tCLCL	Oscillator Frequency	4	24	MHz
TA	Operating Temperature	-40	+105	℃
TST	Storage Temperature	-55	+150	℃
IDD	Maximum Current into VDD	-	120	mA
ISS	Maximum Current out of VSS	-	120	mA
IIO	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 NM1200 DC Electrical Characteristics

(VDD - VSS = 2.5 ~ 5.5 V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
VDD	Operation voltage	2.5	-	5.5	V	VDD = 2.5V ~ 5.5V up to 48 MHz			
VSS / AVSS	Power Ground	-0.3	-	-	V				
VLDO	LDO Output Voltage	1.62	1.8	1.98	V	VDD ≥ 2.5 V			
VBG	Band-gap Voltage		1.2		V	VDD = 3.0V ~ 5.5V, TA = -40°C~105°C			
VDD-AVDD	Allowed Voltage Difference for VDD and AVDD	-0.3	0	0.3	V	-			
IDD5	Operating Current Normal Run Mode HCLK =48 MHz while(1){} Executed from Flash	-	17	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IDD6		-	12	-	mA	5.5V	X	V	X
IDD7		-	17	-	mA	3.3V	X	V	V
IDD8		-	12	-	mA	3.3V	X	V	X
IDD5	Operating Current Normal Run Mode HCLK =44.2368 MHz while(1){} Executed from Flash	-	16	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IDD6		-	11	-	mA	5.5V	X	V	X
IDD7		-	16	-	mA	3.3V	X	V	V
IDD8		-	11	-	mA	3.3V	X	V	X
IDD5	Operating Current Normal Run Mode HCLK =24 MHz while(1){} Executed from Flash	-	10.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IDD6		-	7.5	-	mA	5.5V	X	V	X
IDD7		-	10.5	-	mA	3.3V	X	V	V
IDD8		-	7.5	-	mA	3.3V	X	V	X

IDD5	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	9.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IDD6		-	6.5	-	mA	5.5V	X	V	X
IDD7		-	9.5	-	mA	3.3V	X	V	V
IDD8		-	6.5	-	mA	3.3V	X	V	X
IDD1	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	8.0	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
IDD2		-	6.5	-	mA	5.5V	24 MHz	X	X
IDD3		-	8.0	-	mA	3.3V	24 MHz	X	V
IDD4		-	6.5	-	mA	3.3V	24 MHz	X	X
IDD9	Operating Current Normal Run Mode HCLK = 12MHz while(1){} Executed from Flash	-	4.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
IDD10		-	3.5	-	mA	5.5V	12 MHz	X	X
IDD11		-	4.5	-	mA	3.3V	12 MHz	X	V
IDD12		-	3.5	-	mA	3.3V	12 MHz	X	X
IDD13	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	2.0	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
IDD14		-	1.6	-	mA	5.5V	4 MHz	X	X
IDD15		-	2.0	-	mA	3.3V	4 MHz	X	V
IDD16		-	1.6	-	mA	3.3V	4 MHz	X	X
IDD17	Operating Current Normal Run Mode HCLK = 10 kHz	-	100	-	µA	VDD	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[4]

IDD18	while(1){} Executed from Flash	-	100	-	µA	5.5V	X	V	X
IDD19		-	90	-	µA	3.3V	X	V	V[4]
IDD20		-	90	-	µA	3.3V	X	V	X
IIDLE5	Operating Current Idle Mode HCLK=48 MHz	-	10	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IIDLE6		-	5	-	mA	5.5V	X	V	X
IIDLE7		-	10	-	mA	3.3V	X	V	V
IIDLE8		-	5	-	mA	3.3V	X	V	X
IIDLE5	Operating Current Idle Mode HCLK=44.2368 MHz	-	9.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IIDLE6		-	4.5	-	mA	5.5V	X	V	X
IIDLE7		-	9.5	-	mA	3.3V	X	V	V
IIDLE8		-	4.5	-	mA	3.3V	X	V	X
IIDLE5	Operating Current Idle Mode HCLK=24 MHz	-	6.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IIDLE6		-	3.5	-	mA	5.5V	X	V	X
IIDLE7		-	6.5	-	mA	3.3V	X	V	V
IIDLE8		-	3.5	-	mA	3.3V	X	V	X
IIDLE5	Operating Current Idle Mode HCLK=22.1184 MHz	-	6.0	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
IIDLE6		-	3.0	-	mA	5.5V	X	V	X
IIDLE7		-	6.0	-	mA	3.3V	X	V	V
IIDLE8		-	3.0	-	mA	3.3V	X	V	X
IIDLE1	Operating Current Idle Mode	-	4.0	-	mA	VDD	HXT	HIRC	All Digital Modules

	HCLK = 24MHz					5.5V	24 MHz	X	V
IIDLE2		-	2.2	-	mA	5.5V	24 MHz	X	X
IIDLE3		-	4.0	-	mA	3.3V	24 MHz	X	V
IIDLE4		-	2.2	-	mA	3.3V	24 MHz	X	X
IIDLE9	Operating Current Idle Mode HCLK =12 MHz	-	2.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
IIDLE10		-	1.5	-	mA	5.5V	V	X	X
IIDLE11		-	2.5	-	mA	3.3V	V	X	V
IIDLE12		-	1.5	-	mA	3.3V	V	X	X
IIDLE13	Operating Current Idle Mode HCLK = 4 MHz	-	1.5	-	mA	VDD	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
IIDLE14		-	1.0	-	mA	5.5V	V	X	X
IIDLE15		-	1.5	-	mA	3.3V	V	X	V
IIDLE16		-	1.0	-	mA	3.3V	V	X	X
IDD17	Operating Current Idle Mode HCLK = 10 kHz	-	90	-	µA	VDD	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[4]
IDD18		-	90	-	µA	5.5V	X	V	X
IDD19		-	80	-	µA	3.3V	X	V	V[4]
IDD20		-	80	-	µA	3.3V	X	V	X
IPWD1	Standby Current Power-down Mode (Deep Sleep Mode)	-	1.5	-	µA	VDD = 5.5 V, All oscillators and analog blocks turned off.			
IPWD2		-	1.4	-	µA	VDD = 3.3 V, All oscillators and analog blocks turned off.			

IIL	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-		-75	μA	VDD = 5.5 V, VIN = 0V
ITL	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-		-750	μA	VDD = 5.5 V, VIN = 2.0V
ILK	Input Leakage Current P0/1/2/3/4	-1	-	+1	μA	VDD = 5.5 V, 0 < VIN< VDD Open-drain or input only mode
VIL1	Input Low Voltage P0/1/2/3/4 (TTL Input)	-0.3	-	0.8	V	VDD = 4.5 V
		-0.3	-	0.6		VDD = 2.5 V
VIH1	Input High Voltage P0/1/2/3/4 (TTL Input)	2.0	-	VDD + 0.3	V	VDD = 5.5 V
		1.5	-	VDD + 0.3		VDD = 3.0 V
VIL3	Input Low Voltage XTAL1[*2]	0	-	0.8	V	VDD = 4.5 V
		0	-	0.4		VDD = 2.5 V
VIH3	Input High Voltage XTAL1[*2]	3.5	-	VDD + 0.3	V	VDD = 5.5 V
		2.4	-	VDD + 0.3		VDD = 3.0 V
VILS	Negative-going Threshold (Schmitt Input), nRESET	-0.3	-	0.2 VDD	V	-
VIHS	Positive-going Threshold (Schmitt Input), nRESET	0.7 VDD	-	VDD + 0.3	V	-
RRST	Internal nRESETPin Pull-up Resistor	17.5		150	kΩ	VDD = 2.1 V ~ 5.5V
VILS	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3 VDD	V	-
VIHS	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 VDD	-	VDD + 0.3	V	-

ISR11	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	μA	VDD = 4.5 V, VS = 2.4 V
ISR12		-50	-80	-	μA	VDD = 2.7 V, VS = 2.2 V
ISR13		-40	-73	-	μA	VDD = 2.5 V, VS = 2.0 V
ISR21	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	VDD = 4.5 V, VS = 2.4 V
ISR22		-3	-5	-	mA	VDD = 2.7 V, VS = 2.2 V
ISR23		-2.5	-5	-	mA	VDD = 2.5 V, VS = 2.0 V
ISK11	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-Drain and Push-pull Mode)	10	15	-	mA	VDD = 4.5 V, VS = 0.45 V
ISK12		6	9	-	mA	VDD = 2.7 V, VS = 0.45 V
ISK13		5	8	-	mA	VDD = 2.5 V, VS = 0.45 V

Notes:

1. nRST pin is a Schmitt trigger input.

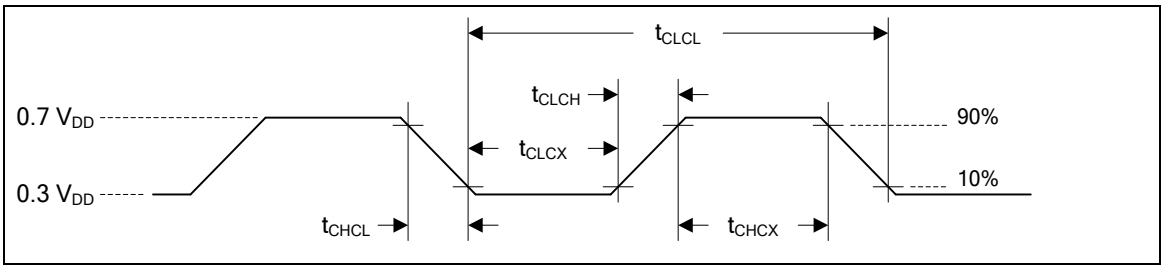
2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3 , P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

4. Only enable modules which support 10 kHz LIRC clock source

5.3 NM1200 AC Electrical Characteristics

5.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tCHCX	Clock High Time	10	-	-	ns	-
tCLCX	Clock Low Time	10	-	-	ns	-
tCLCH	Clock Rise Time	2	-	15	ns	-
tCHCL	Clock Fall Time	2	-	15	ns	-

5.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
VHXT	Operation Voltage	2.5	-	5.5	V	-
TA	Temperature	-40	-	105	℃	-
IHXT	Operating Current	-	410	-	uA	12 MHz, VDD = 5.5V
fHXT	Clock Frequency	4	-	24	MHz	-

5.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

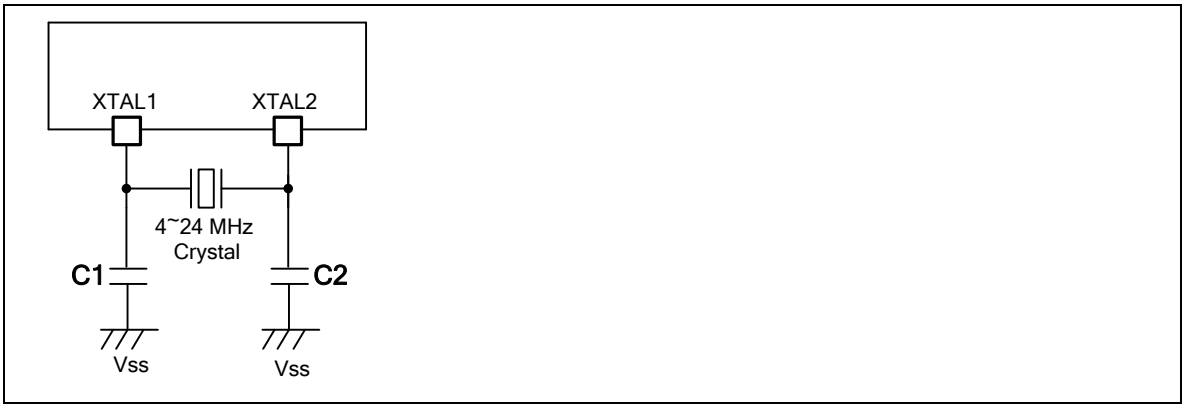


Figure 5.3-1 NM1200/NM1100 Typical Crystal Application Circuit

5.3.4 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VHRC	Supply Voltage	1.62	1.8	1.98	V	-
fHRC	Center Frequency	-	48		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	TA = 25 ℃ VDD = 5 V
		-3[1]	-	+3[1]	%	TA = -40℃~105℃ VDD=2.5 V~ 5.5 V
IHRC	Operating Current	-	700	-	μA	TA = 25 ℃,VDD = 5 V

Note1: These parameters are characterized but not tested.

5.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VLRC	Supply Voltage	2.5	-	5.5	V	-
fLRC	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-50[1]	-	+50[1]	%	VDD = 2.1 V ~ 5.5 V TA = -40℃ ~ +105℃

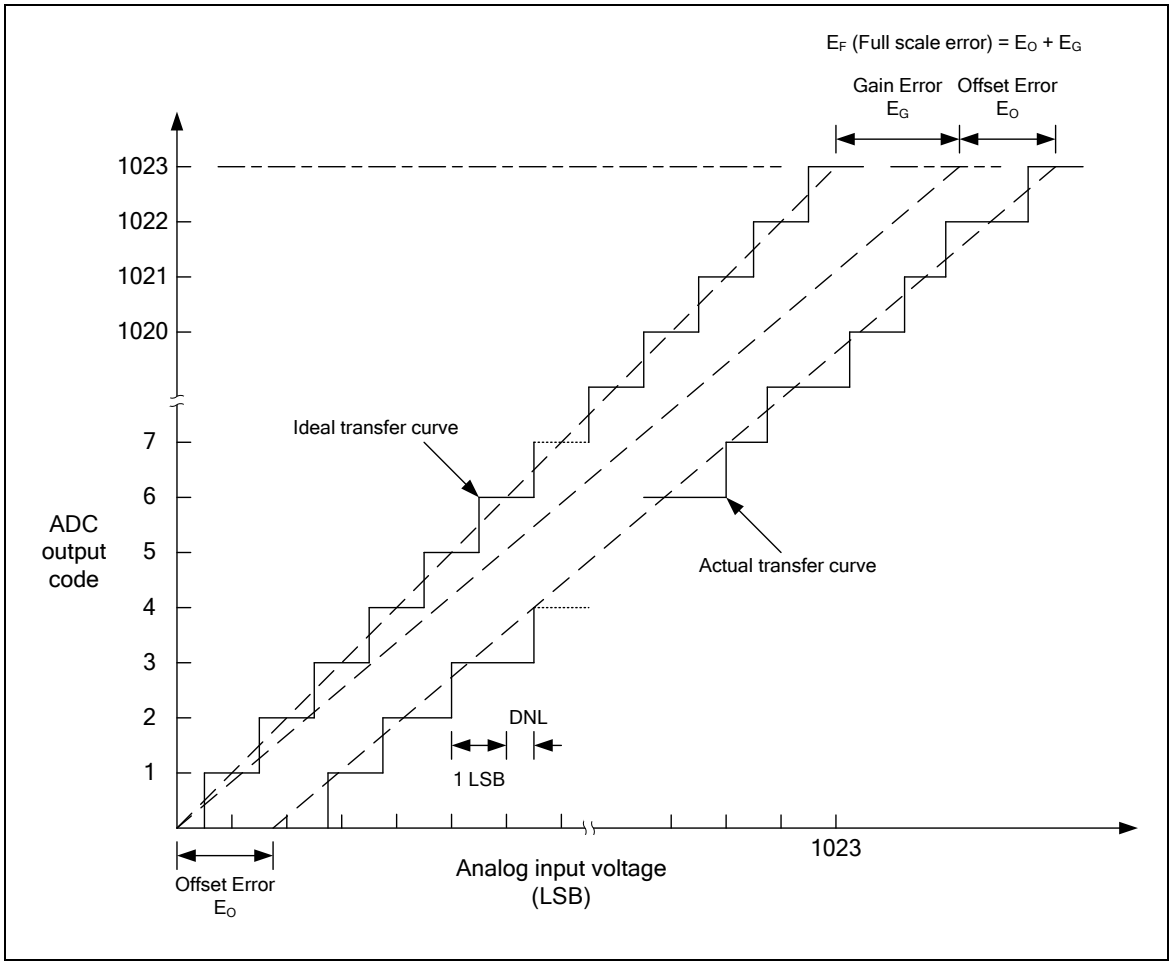
Note1: These parameters are characterized but not tested.

5.4 NM1200 Analog Characteristics

5.4.1 10-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+3	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
EO	Offset Error	-	1	2	LSB	-
EG	Gain Error (Transfer Gain)	-	-1	-1.5	LSB	-
EA	Absolute Error	-	3	5	LSB	-
-	Monotonic	Guaranteed			-	-
FADC	ADC Clock Frequency	-	-	8	MHz	AVDD = 4.5~5.5 V
		-	-	5.4		AVDD =2.5~5.5 V
FS	Sample Rate (FADC/TCONV)	-	-	500	kSPS	AVDD = 4.5~5.5 V
		-	-	300	kSPS	AVDD = 2.5~5.5 V
TACQ	Acquisition Time (Sample Stage)	N+1			1/FADC	N is sampling counter, N=6,7,8,10,14,22,38,70,134,262,1030
TCONV	Total Conversion Time	N+12			1/FADC	
AVDD	Supply Voltage	2.5	-	5.5	V	-
IDDA	Supply Current (Avg.)	-	200	-	μA	AVDD = 5.5 V
VIN	Analog Input Voltage	0	-	AVDD	V	-
CIN	Input Capacitance	-	12	-	pF	-
RIN	Input Load	-	7	-	kΩ	-

Note: ADC voltage reference is same with AVDD



5.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
VDD	DC Power Supply	2.5	-	5.5	V	-
VLDO	Output Voltage	1.62	1.8	1.98	V	-
TA	Temperature	-40	25	105	℃	

Notes:

It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest VSS pin of the device.

5.4.3 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AVDD	Supply Voltage	0	-	5.5	V	-
TA	Temperature	-40	25	105	℃	-

IBOD	Quiescent Current	-	100	-	μA	AVDD =5.5V
VBOD	Brown-out Detector (Falling edge)		4.3		V	BOV_VL [2:0] = 3
			3.7		V	BOV_VL [2:0] = 2
			3.0		V	BOV_VL [2:0] = 7
			2.7		V	BOV_VL [2:0] = 1
			2.4		V	BOV_VL [2:0] = 6
			2.2		V	BOV_VL [2:0] = 0
			2.0		V	BOV_VL [2:0] = 5
			1.7		V	BOV_VL [2:0] = 4

5.4.4 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	25	105	℃	-
VPOR	Reset Voltage		1.25		V	-

5.4.5 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
VCMP	Supply Voltage	2.5	-	5.5	V	
TA	Temperature	-40	25	105	℃	-
ICMP	Operation Current	-	40	80	μA	AVDD=5V
VOFF	Input Offset Voltage		10	20	mV	-
VSW	Output Swing	0.1	-	AVDD – 0.1	V	-
VCOM	Input Common Mode Range	0.1	-	AVDD – 0.1	V	-
-	DC Gain	-	60	-	dB	-
TPGD	Propagation Delay	-	200	-	ns	VCOM=1.2 V, VDIFF=0.1 V
VHYS	Hysteresis	-	±30	-	mV	VCOM=1.2 V
TSTB	Stable time	-	-	1.2	μs	

5.5 NM1200 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
VFLA[2]	Supply Voltage	1.62	1.8	1.98	V	
NENDUR	Endurance	20,000	-	-	cycles[1]	
TRET	Data Retention	10	-	-	year	TA =85℃
TERASE	Sector Erase Time	-	6	-	ms	
TPROG	Program Time	-	7.5	-	us	
IDD1	Read Current	-	4	-	mA	
IDD2	Program Current	-	3.5	-	mA	
IDD3	Erase Current	-	2	-	mA	

Notes:

Number of program/erase cycles.

VFLA is source from chip LDO output voltage.

Guaranteed by design, not test in production.

5.6 NCT3612 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VCC	Input supply voltage.	-0.3 to 40	V
VR12V	Linear regulator voltage output (LDO12V_GD_CAP) for gate driver.	-0.3 to 15	V
VB	High-side floating supply absolute voltage.	-0.3 to VS+VR12V	V
VS	High-side floating supply offset voltage.	-2 to VCC+2	V
HO	High-side floating output voltage.	VS-0.3 to VB+0.3	V
LO	Low-side output voltage.	-0.3 to VR12V+0.3	V
Other pins	5VOUT (LDO5V_MCU_CAP), RSTB, HIN, LIN.	-0.3 to 6	V
θ_{JA}	Thermal Resistance,	40	℃/W
θ_{JC}	Thermal Resistance,	10	℃/W
θ_{STG}	Storage Temperature	-50 to 150	℃
θ_{J}	Junction Temperature	150	℃
ESD Rating	Human Body Mode(all pins)	±2	KV
	Charge Device Mode	±500	V
	Latch-up	±100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.7 NCT3612 Recommended Operating Conditions

PARAMETER	RATING	UNIT
Low side and logic fixed supply voltage	8 to 25	V
LDO5V Supply Output Current	20	mA
Operating Temperature	-40 to 105	℃
Junction Temperature	-40 to 125	℃

Note: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

5.8 NCT3612 DC Electrical Characteristics

(VCC= 35V, TA = TJ = 25° C, unless otherwise specified)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Input supply voltage	VCC		8	---	35	V
VCC UVLO turn-on threshold	UVLO+		---	4	---	V
VCC UVLO turn-off threshold	UVLO-		---	3.6	---	V
VCC UVLO threshold hysteresis			---	0.4	---	V
VCC operation current		PWM=20KHz, Duty=50%	---	20	---	mA
VCC sleep mode current		RSTB=Low	---	100		uA
Gate Driver Output						
Souring peak current	I_{O+}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.25	---	A
Sinking peak current	I_{O-}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.5	---	A
Turn-on propagation delay	t_{on}	VCC=35，C_L=1nF	---	50	---	nS
Turn-off propagation delay	t_{off}	VCC=35，C_L=1nF	---	50	---	nS
Turn-on rise time	t_r	C_L=1nF	---	50	---	nS
Turn-off fall time	t_f	C_L=1nF	---	30	---	nS
PWM delay matching	MT		---	50	---	nS
Pull low resistance	R_o		---	100	---	KΩ
Logic Input						
Voltage high Level	VIH		2.4	---	---	V
Voltage low Level	VIL		---	---	0.8	V
HIN/LIN pull low Resistance			---	100	---	KΩ
Internal 5V/12V regulator						
5V output voltage	$5V_{OUT}$		4.75	5	5.25	V
5V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
12V output voltage	V_{R12V}		---	12	---	V
12V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
Bootstrapped Power Supply Section						
VS_U/V/W leakage current		VB_U/V/W=VS_U/V/W=40V	---	---	50	uA

Bootstrap diode ON resistance	R_{BD}		---	150	---	Ω
Thermal Protection						
Thermal shutdown temperature	TSD		---	165	---	℃
Thermal shutdown hysteresis	TSDHYS		---	50	---	℃

5.9 NCT3612 DC Electrical Characteristics

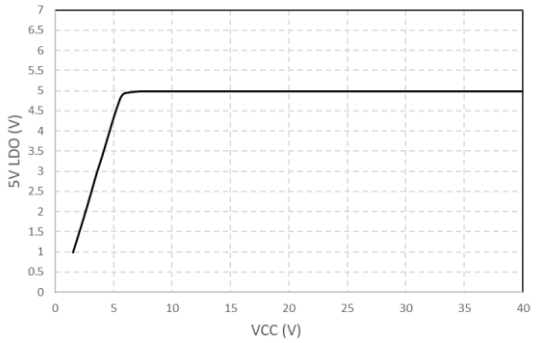


Figure 5.9-1 VCC vs. 5V LDO Voltage

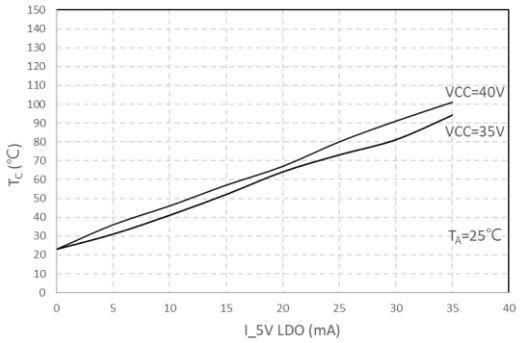


Figure 5.9-2 5V LDO Current vs. IC temperature

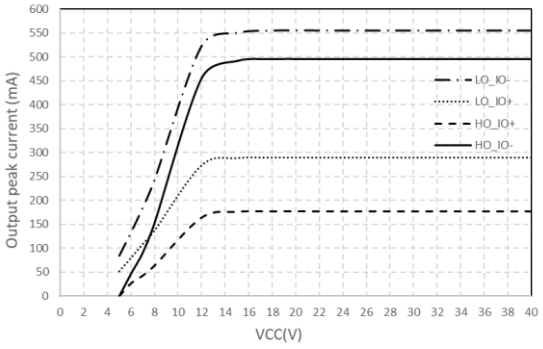


Figure 5.9-3 VCC vs. Output peak current

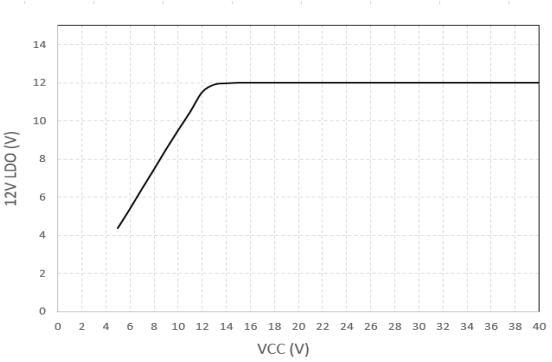


Figure 5.9-4. VCC vs. 12VLDO Voltage

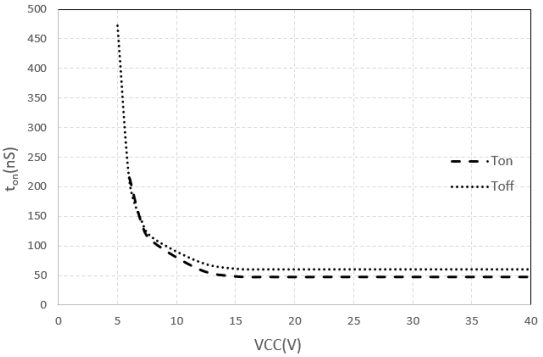


Figure 5.9-5 VCC vs. Ton/Toff propagation delay

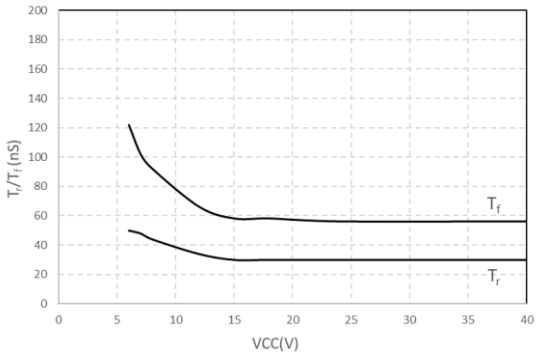
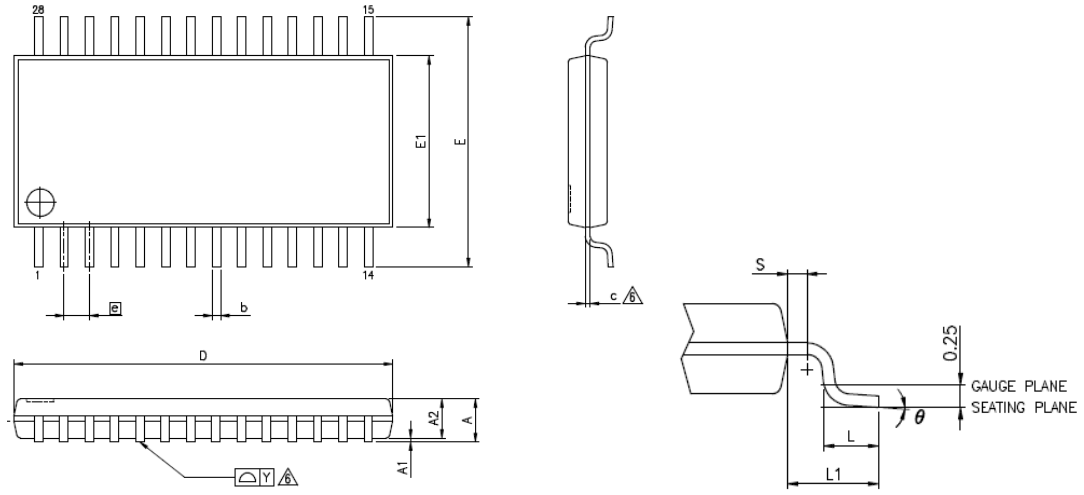


Figure 5.9-6 VCC vs. Turn-on/off rise time

6 PACKAGE DIMENSION

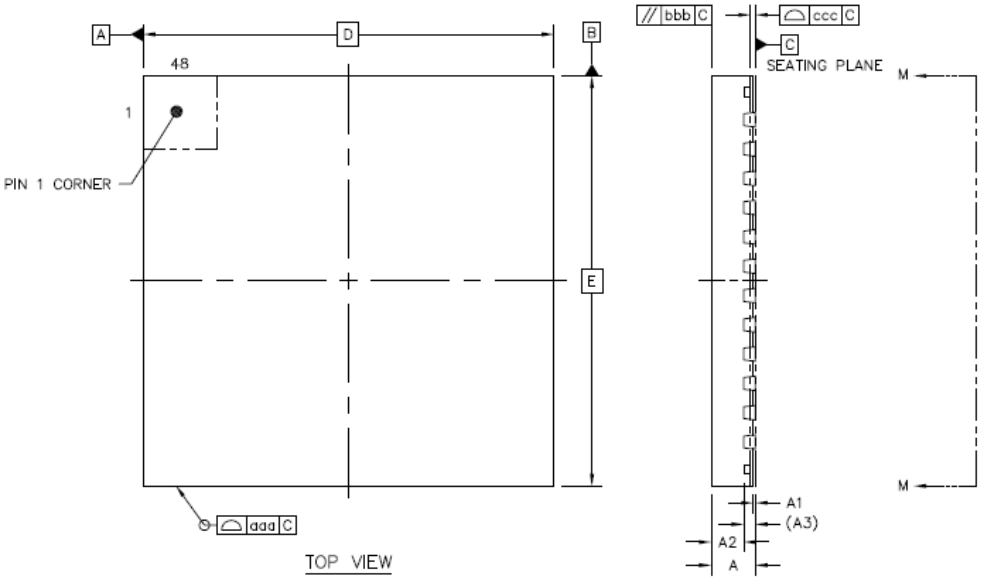
6.1 TSSOP 28-pin (4.4mm x 9.7mm)

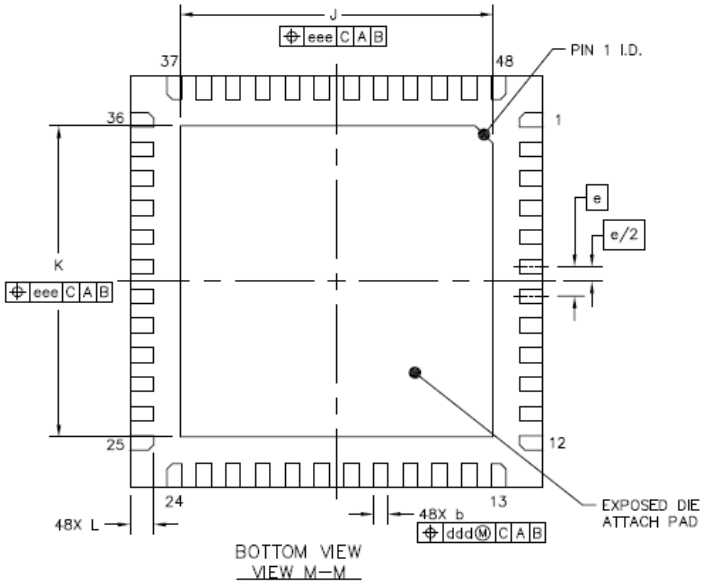


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

6.2 QFN 48L (7.0mm x 7.0mm)





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

7 REVISION HISTORY

Revision	Date	Description
0.01	November 14, 2019	1. Preliminary version 0.01

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