ARM Cortex® -M0

32-bit Microcontroller

NuMicro® Family
NM1240 Series
Data Brief

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1 GENERAL DESCRIPTION

The NuMicro® NM1240 series 32-bit microcontrollers are embedded with ARM® Cortex®-M0 core for industrial applications which need high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NM1240 series can run up to 48(60) MHz and operate at 2.2V(3.3V) ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NM1240 offers 64 Kbytes embedded program Flash, size configurable Data Flash (shared with program flash), 7.5 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 8Kbytes SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, OP, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM1240 to reduce component count, board space and system cost. These useful functions make the NM1240 powerful for a wide range of applications.

Additionally, the NM1240 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48/60 MHz by internal RC oscillator
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.2 V to 5.5 V
- Memory
  - 64 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 7.5 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM0, 1, 2)
  - 8 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - Up to 24 MHz External Clock input (EXT_CLK)
  - 48(60) MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 44 general-purpose I/O (GPIO) pads and 1 Reset pad
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - GPIO built-in Pull-up/Pull-low resistor for selection.
- Timer
  - Provides three channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer

- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Supports event counter function
- Supports Toggle Output mode
- Supports wake-up from Idle or Power-down mode
- Continuous Capture
- Timer0, Timer1, Timer2 and Systick provided with continuous capture function to capture at most 4 edges continuously on one signal

- ECAP (Enhanced Input Capture)
  - One units of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP ports(ECAP0, ECAP1 and ECAP2)
    - ACMP Trigger
- GDMA (General Direct Memory Access
  - Two channels
  - Memory to/from memory or APB device
  - Memory to/from USCI TX/RX buffer which supports the hardware trigger
  - Supports “4-data burst” mode to boost performance
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM
  - Supports a built-in 16-bit PWM clock generators, providing SIX PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/independent/complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Supports Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Support three of hardware Brake pin
  - Supports rising, falling, central, period, and fault break interrupts

- Supports duty/period trigger A/D conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function

- BPWM
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
  - Synchronous mode for BPWM and EPWM
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - USCI1 Supports to be configured as UART, SPI or I²C individually
  - USCI2 Supports to be configured as UART and I²C individually
  - Supports programmable baud-rate generator
  - Supports GDMA trasfer
- ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 800ns conversion time
  - Supports 2 S/H (sample/hold)
  - Up to 16-ch single-end input from I/O and one internal input from band-gap.
  - Each input channel has own data register
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Supports temperature sensor for measurement chip temperature
  - Supports Simultaneous and Sequential continuous conversion.
- OP Amplifier
  - Rail-to-rail OPA x 1
  - Slew rate 6 V/us at least
  - Supports OP1 output as input of ADC and ACMP
- DAC
  - Built-in two 12-bit DAC,
  - Be the reference voltage for ACMP, ADC or output to pins.
- Analog Comparator
  - One analog comparators with 4 reference voltage source
    - Built-in 12-bit DAC0 and DAC1 for comparator reference voltage

- Band-gap voltage
- External voltage from port pin

  - Supports Hysteresis function 0/20/90/150mV at V_{DD} = 5V
  - Interrupt when compared result changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
  - Support 3 group of independent dividend, divisor, quotient and remainder registers for three times of calculation capacity
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP(7x7mm), 48-pin QFN(7x7mm), 32-pin QFN(4x4mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAC	Digital -to-Analog Converter
DAP	Debug Access Port
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
EXT_CLK	External Clock Input
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
GDMA	Gerneal direct memory access
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Selection Guide

4.1.1 NuMicro® NM1240 Series Selection Guide

Note: LQFP48: 7x7mm、QFN48: 7x7mm、QFN33: 4x4mm

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48/60 MHz	PWM	BPWM	Analog Comp.	OPA	ADC (12-bit)	DAC (12-bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI												
							UART	I²C	SPI										
NM1244D48	64	8	7.5	√	44	3	2	2	1	1	6	2	1	1	20	2	1	√	LQFP48
NM1244Y48	64	8	7.5	√	44	3	2	2	1	1	6	2	1	1	20	2	1	√	QFN48
NM1244Y	64	8	7.5	√	29	3	2	2	1	1	6	2	1	1	16	2	1	√	QFN33

Table 4.1-1 NuMicro® NM1240 Base Series Selection Guide

4.2 Pin Configuration

4.2.1 NuMicro® NM1240 Series LQFP48 Diagram

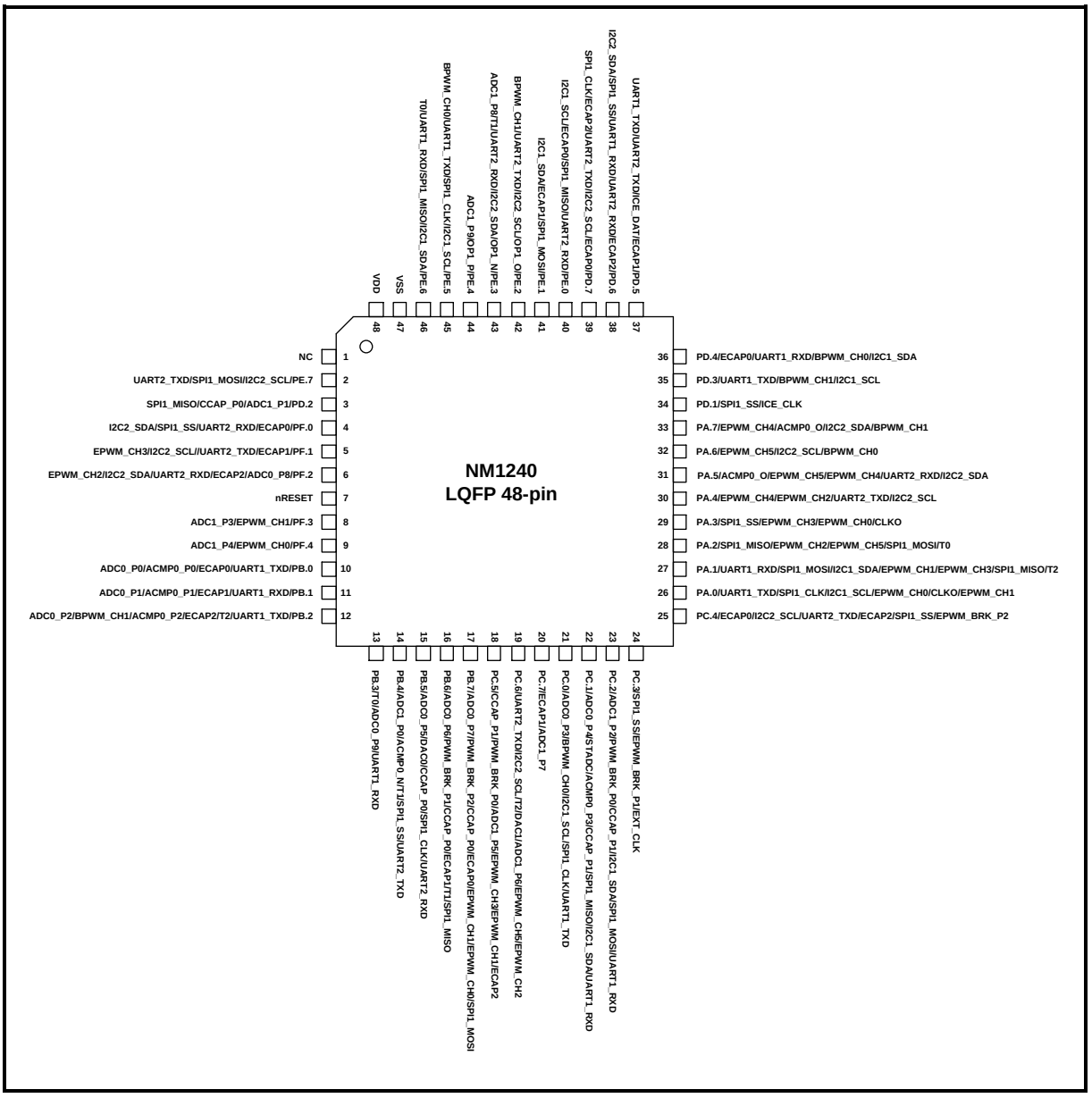


Figure 4.2-1 NuMicro® NM1240 Base Series LQFP 48-pin Diagram

4.2.2 NuMicro® NM1240 Series QFN48 Pin Diagram

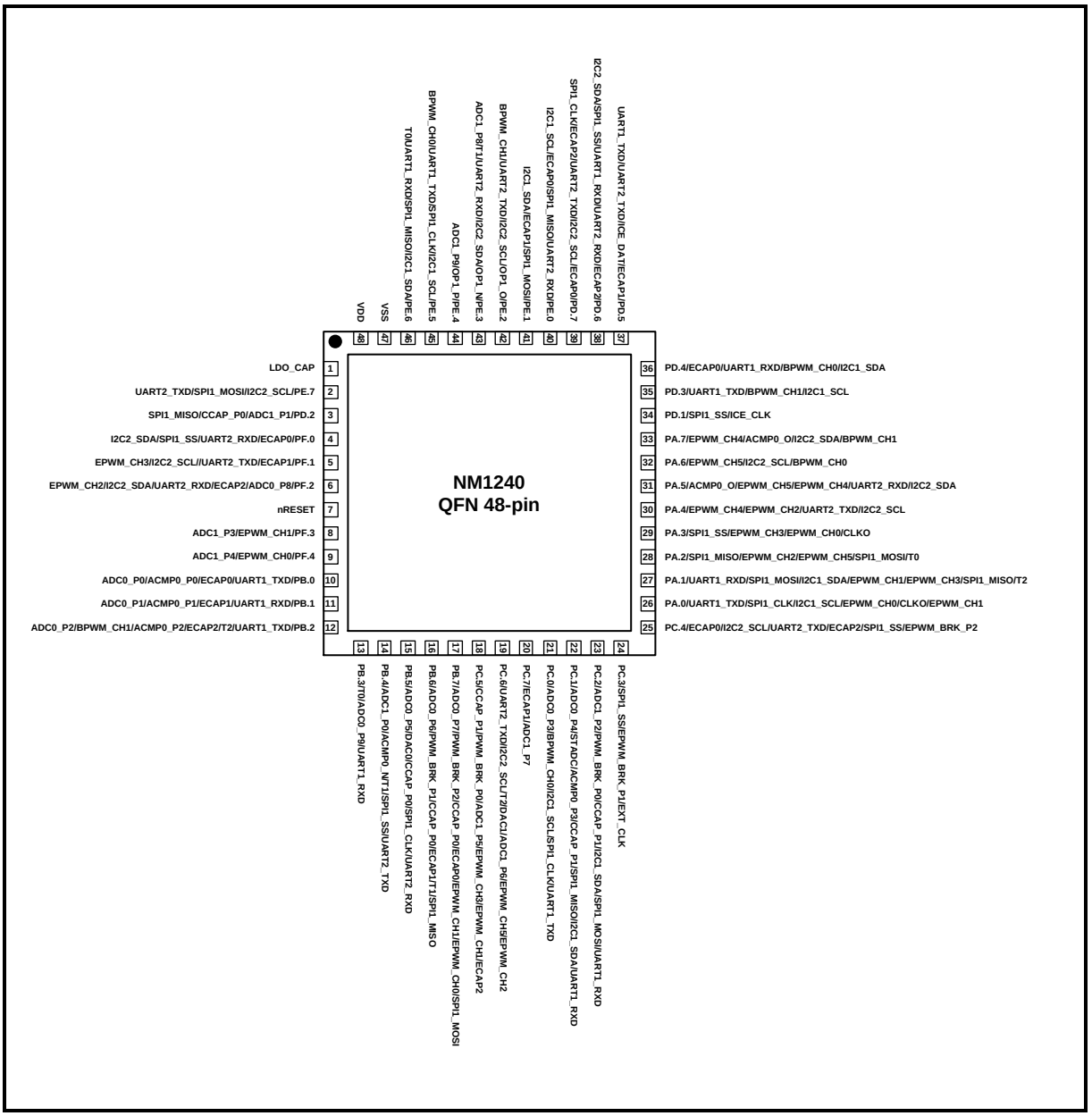


Figure 4.2-2 NuMicro® NM1240 Base Series QFN 48-pin Diagram

4.2.3 NuMicro® NM1240 Series QFN33 Pin Diagram

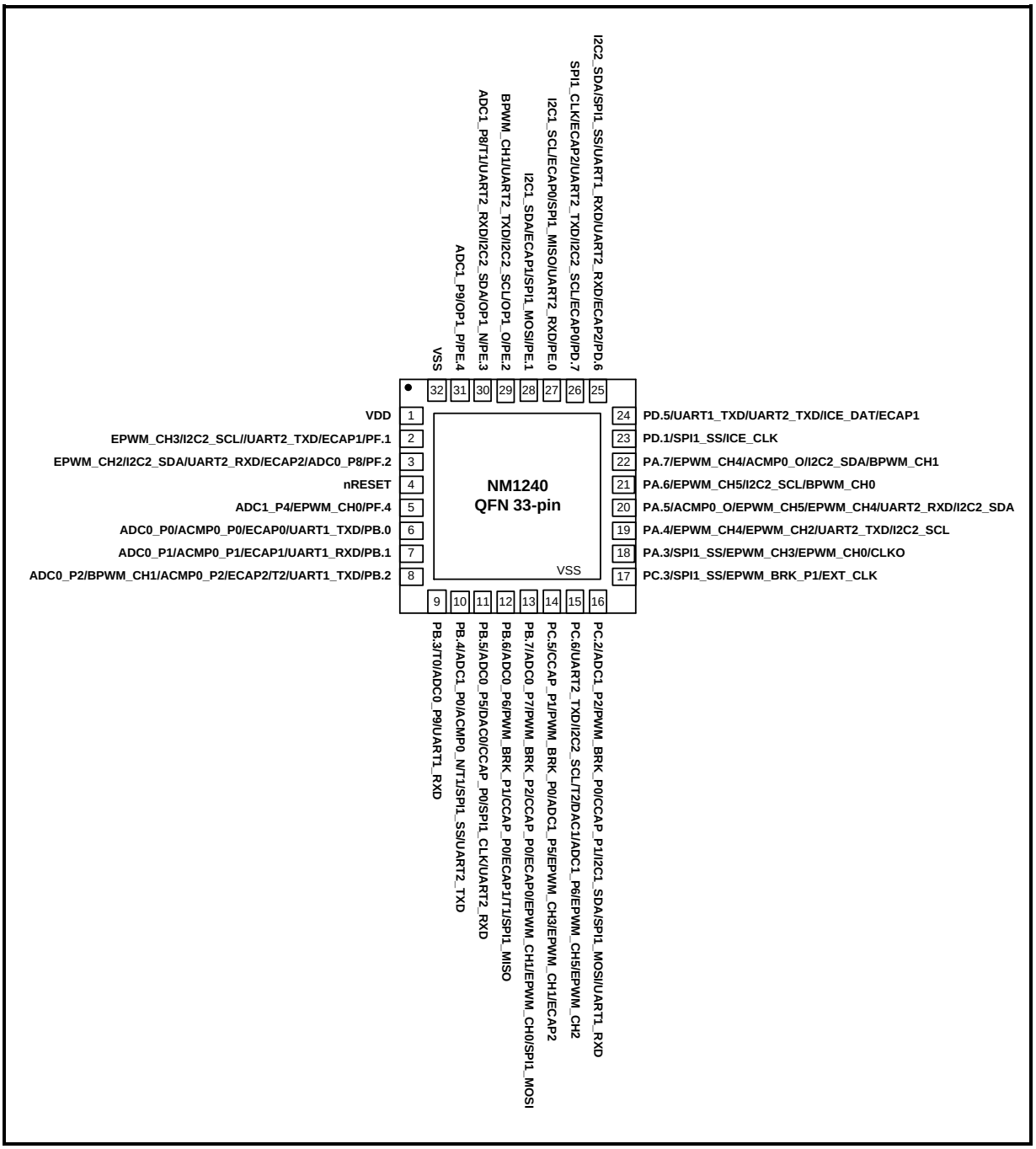


Figure 4.2-3 NuMicro® NM1240 Base Series QFN 33-pin Diagram

4.3 Pin Description

4.3.1 NM1240 Series Pin Description Overview

GPIO	ICE XTAL		ADC		PWM		ACMP0		ACMP1		PGA(OP)		TIMER		I2C		SPI1		UART		ECAP		NM1240		NM1240	
MFP0	MFP1		MFP2		MFP3		MFP4		MFP5		MFP6		MFP7		MFP8		MFPA		MFPB		MFPC		MFPE		MFPF	
GPA0	CLKO	O			EPWM_CH0	O									I2C1_SCL	IO	SPI1_CLK	IO	UART1_TXD	O					EPWM_CH1	O
GPA1					EPWM_CH1	O							T2	IO	I2C1_SDA	IO	SPI1_MOSI	IO	UART1_RXD	I			SPI1_MISO	IO	EPWM_CH3	O
GPA2					EPWM_CH2	O							T0	IO			SPI1_MISO	IO					SPI1_MOSI	IO	EPWM_CH5	O
GPA3	CLKO	O			EPWM_CH3	O											SPI1_SS	IO							EPWM_CH0	O
GPA4					EPWM_CH4	O									I2C2_SCL	IO			UART2_TXD	IO					EPWM_CH2	O
GPA5					EPWM_CH5	O	ACMP0_O	O							I2C2_SDA	IO			UART2_RXD	IO					EPWM_CH4	O
GPA6					EPWM_CH5	O																	I2C2_SCL	IO	BPWM_CH0	O
GPA7					EPWM_CH4		ACMP0_O	O															I2C2_SDA	IO	BPWM_CH1	O
GPB0			ADC0_P0	A			ACMP0_P0	A					ECAP0	I					UART1_TXD	O	ECAP0	I				
GPB1			ADC0_P1	A			ACMP0_P1	A					ECAP1	I					UART1_RXD	I	ECAP1	I				
GPB2			ADC0_P2	A	BPWM_CH1	O	ACMP0_P2	A					ECAP2	I					UART1_TXD	O	ECAP2	I	T2	IO		
GPB3			ADC0_P9	A									T0	IO					UART1_RXD	I						
GPB4			ADC1_P0	A			ACMP0_N	A					T1	IO			SPI1_SS	IO	UART2_TXD	IO						
GPB5			ADC0_P5	A			DAC0	A					CCAP_P0	I			SPI1_CLK	IO	UART2_RXD	IO						
GPB6			ADC0_P6	A	PWM_BRK_P1	I							CCAP_P0	I			SPI1_MISO	IO			ECAP1	I	T1	IO		
GPB7			ADC0_P7	A	PWM_BRK_P2	I							CCAP_P0	I			SPI1_MOSI	IO			ECAP0	I	EPWM_CH0	O	EPWM_CH1	O
GPC0			ADC0_P3	A	BPWM_CH0	O									I2C1_SCL	IO	SPI1_CLK	IO	UART1_TXD	O						
GPC1			ADC0_P4	A	STADC	I	ACMP0_P3	A					CCAP_P1	I	I2C1_SDA	IO	SPI1_MISO	IO	UART1_RXD	I						
GPC2			ADC1_P2	A	PWM_BRK_P0	I							CCAP_P1	I	I2C1_SDA	IO	SPI1_MOSI	IO	UART1_RXD	I						
GPC3	REF_CLK	I			PWM_BRK_P1	I											SPI1_SS	IO								
GPC4					PWM_BRK_P2	I							ECAP0	I	I2C2_SCL	IO	SPI1_SS	IO	UART2_TXD	IO	ECAP2	I				
GPC5			ADC1_P5	A	PWM_BRK_P0	I							CCAP_P1	I							ECAP2	I	EPWM_CH1	O	EPWM_CH3	O
GPC6			ADC1_P6	A	EPWM_CH2	O			DAC1	O			T2	IO	I2C2_SCL	IO			UART2_TXD	IO					EPWM_CH5	O
GPC7			ADC1_P7	A																	ECAP1	I				
GPD1	ICE_CLK	I															SPI1_SS	IO								
GPD2			ADC1_P1	A									CCAP_P0	I			SPI1_MISO	IO								
GPD3					BPWM_CH1	O									I2C1_SCL	IO			UART1_TXD	O						
GPD4					BPWM_CH0	O									I2C1_SDA	IO			UART1_RXD	I	ECAP0	I				
GPD5	ICE_DAT	IO																			ECAP1	I	UART1_TXD	O	UART2_TXD	O
GPD6															I2C2_SDA	IO	SPI1_SS	IO			ECAP2	I	UART1_RXD	I	UART2_RXD	I
GPD7													ECAP0	I	I2C2_SCL	IO	SPI1_CLK	IO	UART2_TXD	IO	ECAP2	I				
GPE0															I2C1_SCL	IO	SPI1_MISO	IO	UART2_RXD	IO	ECAP0	I				
GPE1															I2C1_SDA	IO	SPI1_MOSI	IO			ECAP1	I				
GPE2					BPWM_CH1	O					OP1_O	A			I2C2_SCL	IO			UART2_TXD	O						
GPE3			ADC1_P8	A							OP1_N	A	T1	IO	I2C2_SDA	IO			UART2_RXD	I						
GPE4			ADC1_P9	A							OP1_P	A														
GPE5					BPWM_CH0	O									I2C1_SCL	IO	SPI1_CLK	IO	UART1_TXD	O						
GPE6													T0	IO	I2C1_SDA	IO	SPI1_MISO	IO	UART1_RXD	I						
GPE7															I2C2_SCL	IO	SPI1_MOSI	IO	UART2_TXD	IO						
GPF0															I2C2_SDA	IO	SPI1_SS	IO	UART2_RXD	IO	ECAP0	I				
GPF1					EPWM_CH3	O									I2C2_SCL	IO			UART2_TXD	IO	ECAP1	I				
GPF2			ADC0_P8	A	EPWM_CH2	O									I2C2_SDA	IO			UART2_RXD	IO	ECAP2	I				
GPF3			ADC1_P3	A	EPWM_CH1	O																				
GPF4			ADC1_P4	A	EPWM_CH0	O																				

4.3.2 NM1240 Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

MFP only configures the ouput data or input data of PAD, the direction of PAD were configured by PMD.

The priority of MFP in the same multi-function was GPA > GPB > GPC > GPD > GPE > GPF.

The type A of multi-function needs to be configured to be input port.

4.3.2.1 NM1240 Series LQFP48/QFN48/QFN33 Pin Description

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
-	1	LDO_CAP/ NC(LQFP48)	A/	MFP0/	LDO output pin. Note: Recommend to connect a 1uF CAP to the pin.
-	2	PE.7	I/O	MFP0	General purpose digital I/O pin.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
-	3	PD.2	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P1	A	MFP2	ADC1 channel analog input.
		CCAP_P0	I	MFP7	Timer Continuous Capture input pin.
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
-	4	PF.0	I/O	MFP0	General purpose digital I/O pin.
		I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
		UART2_RXD	I/O	MFPB	Data receiver input pin for UART.
		ECAP0	I	MFPC	Enhanced Input Capture input pin.
2	5	PF.1	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH3	O	MFP3	EPWM channel3 output/capture input.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
3	6	PF.2	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P8	A	MFP2	ADC0 channel analog input.
		EPWM_CH2	O	MFP3	EPWM channel2 output/capture input.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
		UART2_RXD	I/O	MFPB	Data receiver input pin for UART.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.
4	7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
-	8	PF.3	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P3	A	MFP2	ADC1 channel analog input.
		EPWM_CH1	O	MFP3	EPWM channel1 output/capture input.
5	9	PF.4	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P4	A	MFP2	ADC1 channel analog input.
		EPWM_CH0	O	MFP3	EPWM channel0 output/capture input.
6	10	PB.0	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P0	A	MFP2	ADC0 channel analog input.
		ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
		ECAP0	I	MFP7	Enhanced Input Capture input pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
		ECAP0	I	MFPC	Enhanced Input Capture input pin.
7	11	PB.1	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P1	A	MFP2	ADC0 channel analog input.
		ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
		ECAP1	I	MFP7	Enhanced Input Capture input pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
8	12	PB.2	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P2	A	MFP2	ADC0 channel analog input.
		BPWM_CH1	O	MFP3	BPWM channel1 output/capture input.
		ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
		ECAP2	I	MFP7	Enhanced Input Capture input pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.
		T2	I/O	MFPE	Timer2 event counter input / toggle output.
9	13	PB.3	I/O	MFP0	General purpose digital I/O pin.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		ADC0_P9	A	MFP2	ADC0 channel analog input.
		T0	I/O	MFP7	Timer0 event counter input / toggle output.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.
10	14	PB.4	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P0	A	MFP2	ADC1 channel analog input.
		ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
		T1	I/O	MFP7	Timer1 event counter input / toggle output.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
11	15	PB.5	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P5	A	MFP2	ADC0 channel analog input.
		DAC0	A	MFP4	DAC0 analog output.
		CCAP_P0	I	MFP7	Timer Continuous Capture input pin.
		SPI1_CLK	I/O	MFPA	SPI1 serial clock pin.
		UART2_RXD	I/O	MFPB	Data receiver input pin for UART.
12	16	PB.6	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P6	A	MFP2	ADC0 channel analog input.
		PWM_BRK_P1	I	MFP3	Brake input pin of EPWM.
		CCAP_P0	I	MFP7	Timer Continuous Capture input pin.
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
		T1	I/O	MFPE	Timer1 event counter input / toggle output.
13	17	PB.7	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P7	A	MFP2	ADC0 channel analog input.
		PWM_BRK_P2	I	MFP3	Brake input pin of EPWM.
		CCAP_P0	I	MFP7	Timer Continuous Capture input pin.
		SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
		ECAP0	I	MFPC	Enhanced Input Capture input pin.
		EPWM_CH0	O	MFPE	EPWM channel0 output/capture input.
		EPWM_CH1	O	MFPF	EPWM channel1 output/capture input.
14	18	PC.5	I/O	MFP0	General purpose digital I/O pin.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		ADC1_P5	A	MFP2	ADC1 channel analog input.
		PWM_BRK_P0	I	MFP3	Brake input pin of EPWM.
		CCAP_P1	I	MFP7	Timer Continuous Capture input pin.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.
		EPWM_CH1	O	MFPE	EPWM channel1 output/capture input.
		EPWM_CH3	O	MFPF	EPWM channel3 output/capture input.
15	19	PC.6	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P6	A	MFP2	ADC1 channel analog input.
		EPWM_CH2	O	MFP3	EPWM channel2 output/capture input.
		DAC1	O	MFP5	DAC1 analog output.
		T2	I/O	MFP7	Timer2 event counter input / toggle output.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
		EPWM_CH5	O	MFPF	EPWM channel5 output/capture input.
-	20	PC.7	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P7	A	MFP2	ADC1 channel analog input.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
-	21	PC.0	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P3	A	MFP2	ADC0 channel analog input.
		BPWM_CH0	O	MFP3	BPWM channel0 output/capture input.
		I2C1_SCL	I/O	MFP8	I2C1 clock pin.
		SPI1_CLK	I/O	MFPA	SPI1 serial clock pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
-	22	PC.1	I/O	MFP0	General purpose digital I/O pin.
		ADC0_P4	A	MFP2	ADC0 channel analog input.
		STADC	I	MFP3	ADC external trigger input.
		ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.
		CCAP_P1	I	MFP7	Timer Continuous Capture input pin.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
16	23	PC.2	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P2	A	MFP2	ADC1 channel analog input.
		PWM_BRK_P0	I	MFP3	Brake input pin of EPWM.
		CCAP_P1	I	MFP7	Timer Continuous Capture input pin.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
		SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.
17	24	PC.3	I/O	MFP0	General purpose digital I/O pin.
		REF_CLK	I	MFP1	
		PWM_BRK_P1	I	MFP3	Brake input pin of EPWM.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
-	25	PC.4	I/O	MFP0	General purpose digital I/O pin.
		PWM_BRK_P2	I	MFP3	Brake input pin of EPWM.
		ECAP0	I	MFP7	Enhanced Input Capture input pin.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.
-	26	PA.0	I/O	MFP0	General purpose digital I/O pin.
		CLKO	O	MFP1	Clock Out.
		EPWM_CH0	O	MFP3	EPWM channel0 output/capture input.
		I2C1_SCL	I/O	MFP8	I2C1 clock pin.
		SPI1_CLK	I/O	MFPA	SPI1 serial clock pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
		EPWM_CH1	O	MFPF	EPWM channel1 output/capture input.
-	27	PA.1	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH1	O	MFP3	EPWM channel1 output/capture input.
		T2	I/O	MFP7	Timer2 event counter input / toggle output.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
		SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		SPI1_MISO	I/O	MFPE	SPI1 MISO (Master In, Slave Out) pin.
		EPWM_CH3	O	MFPF	EPWM channel3 output/capture input.
-	28	PA.2	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH2	O	MFP3	EPWM channel2 output/capture input.
		T0	I/O	MFP7	Timer0 event counter input / toggle output.
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
		SPI1_MOSI	I/O	MFPE	SPI1 MOSI (Master Out, Slave In) pin.
		EPWM_CH5	O	MFPF	EPWM channel5 output/capture input.
18	29	PA.3	I/O	MFP0	General purpose digital I/O pin.
		CLKO	O	MFP1	Clock Out.
		EPWM_CH3	O	MFP3	EPWM channel3 output/capture input.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
		EPWM_CH0	O	MFPF	EPWM channel0 output/capture input.
19	30	PA.4	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH4	O	MFP3	EPWM channel4 output/capture input.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
		EPWM_CH2	O	MFPF	EPWM channel2 output/capture input.
20	31	PA.5	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH5	O	MFP3	EPWM channel5 output/capture input.
		ACMP0_O	O	MFP4	Analog comparator0 output.
		I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
		UART2_RXD	I/O	MFPB	Data receiver input pin for UART.
		EPWM_CH4	O	MFPF	EPWM channel4 output/capture input.
21	32	PA.6	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH5	O	MFP3	EPWM channel5 output/capture input.
		I2C2_SCL	I/O	MFPE	I2C2 clock pin.
		BPWM_CH0	O	MFPF	BPWM channel0 output/capture input.
22	33	PA.7	I/O	MFP0	General purpose digital I/O pin.
		EPWM_CH4	O	MFP3	EPWM channel4 output/capture input.
		ACMP0_O	O	MFP4	Analog comparator0 output.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		I2C2_SDA	I/O	MFPE	I2C2 data input/output pin.
		BPWM_CH1	O	MFPF	BPWM channel1 output/capture input.
23	34	PD.1	I/O	MFP0	General purpose digital I/O pin.
		ICE_CLK	I	MFP1	Serial wired debugger clock pin.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
-	35	PD.3	I/O	MFP0	General purpose digital I/O pin.
		BPWM_CH1	O	MFP3	BPWM channel1 output/capture input.
		I2C1_SCL	I/O	MFP8	I2C1 clock pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
-	36	PD.4	I/O	MFP0	General purpose digital I/O pin.
		BPWM_CH0	O	MFP3	BPWM channel0 output/capture input.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.
		ECAP0	I	MFPC	Enhanced Input Capture input pin.
24	37	PD.5	I/O	MFP0	General purpose digital I/O pin.
		ICE_DAT	I/O	MFP1	Serial wired debugger data pin.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
		UART1_TXD	O	MFPE	Data transmitter output pin for UART.
		UART2_TXD	I/O	MFPF	Data transmitter output pin for UART.
25	38	PD.6	I/O	MFP0	General purpose digital I/O pin.
		I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
		SPI1_SS	I/O	MFPA	SPI1 slave select pin.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.
		UART1_RXD	I	MFPE	Data receiver input pin for UART.
		UART2_RXD	I/O	MFPF	Data receiver input pin for UART.
26	39	PD.7	I/O	MFP0	General purpose digital I/O pin.
		ECAP0	I	MFP7	Enhanced Input Capture input pin.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		SPI1_CLK	I/O	MFPA	SPI1 serial clock pin.
		UART2_TXD	I/O	MFPB	Data transmitter output pin for UART.
		ECAP2	I	MFPC	Enhanced Input Capture input pin.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
27	40	PE.0	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SCL	I/O	MFP8	I2C1 clock pin.
		SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
		UART2_RXD	I/O	MFPB	Data receiver input pin for UART.
		ECAP0	I	MFPC	Enhanced Input Capture input pin.
28	41	PE.1	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
		ECAP1	I	MFPC	Enhanced Input Capture input pin.
29	42	PE.2	I/O	MFP0	General purpose digital I/O pin.
		BPWM_CH1	O	MFP3	BPWM channel1 output/capture input.
		OP1_O	A	MFP6	Operational Amplifier output pin.
		I2C2_SCL	I/O	MFP8	I2C2 clock pin.
		UART2_TXD	O	MFPB	Data transmitter output pin for UART.
30	43	PE.3	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P8	A	MFP2	ADC1 channel analog input.
		OP1_N	A	MFP6	Operational Amplifier Negitive input pin.
		T1	I/O	MFP7	Timer1 event counter input / toggle output.
		I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
		UART2_RXD	I	MFPB	Data receiver input pin for UART.
31	44	PE.4	I/O	MFP0	General purpose digital I/O pin.
		ADC1_P9	A	MFP2	ADC1 channel analog input.
		OP1_P	A	MFP6	Operational Amplifier Positive input pin.
-	45	PE.5	I/O	MFP0	General purpose digital I/O pin.
		BPWM_CH0	O	MFP3	BPWM channel0 output/capture input.
		I2C1_SCL	I/O	MFP8	I2C1 clock pin.
		SPI1_CLK	I/O	MFPA	SPI1 serial clock pin.
		UART1_TXD	O	MFPB	Data transmitter output pin for UART.
-	46	PE.6	I/O	MFP0	General purpose digital I/O pin.
		T0	I/O	MFP7	Timer0 event counter input / toggle output.
		I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.

QFN33	QFN48/ LQFP48	Pin Name	Type	MFP*	Description
		SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
		UART1_RXD	I	MFPB	Data receiver input pin for UART.
32	47	VSS	PWR	MFP0	Ground pin for digital circuit.
1	48	VDD	PWR	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.

Table 4.3-1 LQFP48/QFN48/QFN33 Pin Description

Note:

1. Do not leave the pins ICE_CLK and ICE_DAT in floating when MCU is in operatoin. User may refer to one of the following methods
    a. Add external pull-up or pull-low resistors at pins.
    b. Set the 2 pins in Quasi-mode and output high to be equivelant to internal pull high.
    c. Enable intenal pull-up by setting PD_PHEN[1] = 1b、PD_PHEN[5] = 1b.
    d. Be wired to other deivce without floating at pins.

4.3.3 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_P0	PB.0	MFP4	A	Comparator0 positive input pin.
	ACMP0_P1	PB.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_P2	PB.2	MFP4	A	Comparator0 positive input pin.
	ACMP0_P3	PC.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_N	PB.4	MFP4	A	Comparator0 negative input pin.
	ACMP0_O	PA.7	MFP4	O	Comparator0 output pin.
		PA.5	MFP4	O	Comparator0 output pin.
STADC	STADC	PC.1	MFP3	I	External ADC trigger input pin.
ADC0	ADC0_P0	PB.0	MFP2	A	ADC0 analog input port 0.
	ADC0_P1	PB.1	MFP2	A	ADC0 analog input port 1.
	ADC0_P2	PB.2	MFP2	A	ADC0 analog input port 2.
	ADC0_P3	PC.0	MFP2	A	ADC0 analog input port 3.
	ADC0_P4	PC.1	MFP2	A	ADC0 analog input port 4.
	ADC0_P5	PB.5	MFP2	A	ADC0 analog input port 5.
	ADC0_P6	PB.6	MFP2	A	ADC0 analog input port 6.
	ADC0_P7	PB.7	MFP2	A	ADC0 analog input port 7.
	ADC0_P8	PF.2	MFP2	A	ADC0 analog input port 8.
	ADC0_P9	PB.3	MFP2	A	ADC0 analog input port 9.
ADC1	ADC1_P0	PB.4	MFP2	A	ADC1 analog input port 0.
	ADC1_P1	PD.2	MFP2	A	ADC1 analog input port 1.
	ADC1_P2	PC.2	MFP2	A	ADC1 analog input port 2.
	ADC1_P3	PF.3	MFP2	A	ADC1 analog input port 3.
	ADC1_P4	PF.4	MFP2	A	ADC1 analog input port 4.
	ADC1_P5	PC.5	MFP2	A	ADC1 analog input port 5.
	ADC1_P6	PC.6	MFP2	A	ADC1 analog input port 6.
	ADC1_P7	PC.7	MFP2	A	ADC1 analog input port 7.
	ADC1_P8	PE.3	MFP2	A	ADC1 analog input port 8.
	ADC1_P9	PE.4	MFP2	A	ADC1 analog input port 9.
CLKO	CLKO	PA.0	MFP1	O	Clock output pin.

Group	Pin Name	GPIO	MFP*	Type	Description
		PA.3	MFP1	O	Clock output pin.
BPWM	BPWM_CH0	PA.6	MFPF	O	Basic PWM channel 0 output
		PC.0	MFP3	O	Basic PWM channel 0 output
		PD.4	MFP3	O	Basic PWM channel 0 output
		PE.5	MFP3	O	Basic PWM channel 0 output
	BPWM_CH1	PA.7	MFPF	O	Basic PWM channel 1 output
		PB.2	MFP3	O	Basic PWM channel 1 output
		PD.3	MFP3	O	Basic PWM channel 1 output
		PE.2	MFP3	O	Basic PWM channel 1 output
CCAP	CCAP_P0	PB.5	MFP7	I	Continuous Capture Input
		PB.6	MFP7	I	Continuous Capture Input
		PB.7	MFP7	I	Continuous Capture Input
		PD.2	MFP7	I	Continuous Capture Input
	CCAP_P1	PC.1	MFP7	I	Continuous Capture Input
		PC.2	MFP7	I	Continuous Capture Input
		PC.5	MFP7	I	Continuous Capture Input
ECAP	ECAP_P0	PB.0	MFP7,MFPC	I	Input capture channel 0
		PB.7	MFPC	I	Input capture channel 0
		PC.4	MFP7	I	Input capture channel 0
		PD.4	MFPC	I	Input capture channel 0
		PD.7	MFP7	I	Input capture channel 0
		PE.0	MFPC	I	Input capture channel 0
		PF.0	MFPC	I	Input capture channel 0
	ECAP_P1	PB.1	MFP7,MFPC	I	Input capture channel 1
		PB.6	MFPC	I	Input capture channel 1
		PC.7	MFPC	I	Input capture channel 1
		PD.5	MFPC	I	Input capture channel 1
		PE.1	MFPC	I	Input capture channel 1
		PF.1	MFPC	I	Input capture channel 1
	ECAP_P2	PB.2	MFP7,MFPC	I	Input capture channel 2
		PC.4	MFPC	I	Input capture channel 2
		PC.5	MFPC	I	Input capture channel 2
		PD.6	MFPC	I	Input capture channel 2
		PD.7	MFPC	I	Input capture channel 2

Group	Pin Name	GPIO	MFP*	Type	Description
		PF.2	MFPC	I	Input capture channel 2
EPWM	PWM_BRK_P0	PC.2	MFP3	I	EPWM brake pin.
		PC.5	MFP3	I	EPWM brake pin.
	PWM_BRK_P1	PB.6	MFP3	I	EPWM brake pin.
		PC.3	MFP3	I	EPWM brake pin.
	PWM_BRK_P2	PB.7	MFP3	I	EPWM brake pin.
		PC.4	MFP3	I	EPWM brake pin.
	EPWM_CH5	PA.2	MFPF	O	Enhanced PWM output pin.
		PA.5	MFP3	O	Enhanced PWM output pin.
		PA.6	MFP3	O	Enhanced PWM output pin.
		PC.5	MFPF	O	Enhanced PWM output pin.
	EPWM_CH4	PA.4	MFP3	O	Enhanced PWM output pin.
		PA.5	MFPF	O	Enhanced PWM output pin.
		PA.7	MFP3	O	Enhanced PWM output pin.
	EPWM_CH3	PA.1	MFPF	O	Enhanced PWM output pin.
		PA.3	MFP3	O	Enhanced PWM output pin.
		PC.5	MFPF	O	Enhanced PWM output pin.
		PF.1	MFP3	O	Enhanced PWM output pin.
	EPWM_CH2	PA.2	MFP3	O	Enhanced PWM output pin.
		PA.4	MFPF	O	Enhanced PWM output pin.
		PC.6	MFP3	O	Enhanced PWM output pin.
		PF.2	MFP3	O	Enhanced PWM output pin.
	EPWM_CH1	PA.0	MFPF	O	Enhanced PWM output pin.
		PA.1	MFP3	O	Enhanced PWM output pin.
		PB.7	MFPF	O	Enhanced PWM output pin.
		PC.5	MFPE	O	Enhanced PWM output pin.
		PF.3	MFP3	O	Enhanced PWM output pin.
	EPWM_CH0	PA.0	MFP3	O	Enhanced PWM output pin.
		PA.3	MFPF	O	Enhanced PWM output pin.
		PB.7	MFPE	O	Enhanced PWM output pin.
		PF.4	MFP3	O	Enhanced PWM output pin.
nRESET	nRESET	--	--	I	External reset pin, internal pull-high.
I2C1	I2C1_SCL	PA.0	MFP8	I/O	I^2C1 clock pin.
		PC.0	MFP8	I/O	I^2C1 clock pin.

Group	Pin Name	GPIO	MFP*	Type	Description
		PD.3	MFP8	I/O	I²C1 clock pin.
		PE.0	MFP8	I/O	I²C1 clock pin.
		PE.5	MFP8	I/O	I²C1 clock pin.
	I2C1_SDA	PA.1	MFP8	I/O	I²C1 data pin.
		PC.1	MFP8	I/O	I²C1 data pin.
		PC.2	MFP8	I/O	I²C1 data pin.
		PD.4	MFP8	I/O	I²C1 data pin.
		PE.1	MFP8	I/O	I²C1 data pin.
		PE.6	MFP8	I/O	I²C1 data pin.
I2C2	I2C2_SCL	PA.4	MFP8	I/O	I²C2 clock pin.
		PA.6	MFPE	I/O	I²C2 clock pin.
		PC.4	MFP8	I/O	I²C2 clock pin.
		PC.6	MFP8	I/O	I²C2 clock pin.
		PD.7	MFP8	I/O	I²C2 clock pin.
		PE.2	MFP8	I/O	I²C2 clock pin.
		PE.7	MFP8	I/O	I²C2 clock pin.
		PF.1	MFP8	I/O	I²C2 clock pin.
	I2C2_SDA	PA.5	MFP8	I/O	I²C2 data pin.
		PA.7	MFPE	I/O	I²C2 data pin.
		PD.6	MFP8	I/O	I²C2 data pin.
		PE.3	MFP8	I/O	I²C2 data pin.
		PF.0	MFP8	I/O	I²C2 data pin.
		PF.2	MFP8	I/O	I²C2 data pin.
DAC	DAC0	PB.5	MFP4	A	DAC0 analog output pin.
	DAC1	PC.6	MFP5	A	DAC1 analog output pin.
OP	OP1_O	PE.2	MFP6	A	OP1 analog output pin.
	OP1_N	PE.3	MFP6	A	OP1 analog input pin.
	OP1_P	PE.4	MFP6	A	OP1 analog input pin.
SPI1	SPI1_MOSI	PA.1	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PA.2	MFPE	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PB.7	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PC.2	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PE.1	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PE.7	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.

Group	Pin Name	GPIO	MFP*	Type	Description
	SPI1_MISO	PA.1	MFPE	I/O	SPI1 MISO (Master In, Slave Out) pin
		PA.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
		PB.6	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
		PC.1	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
		PD.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
		PE.0	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
		PE.6	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_CLK	PA.0	MFPA	I/O	SPI1 clock pin.
		PB.5	MFPA	I/O	SPI1 clock pin.
		PC.0	MFPA	I/O	SPI1 clock pin.
		PD.7	MFPA	I/O	SPI1 clock pin.
		PE.5	MFPA	I/O	SPI1 clock pin.
	SPI1_SS	PA.3	MFPA	I/O	SPI1 Slave Select
		PB.4	MFPA	I/O	SPI1 Slave Select
		PC.3	MFPA	I/O	SPI1 Slave Select
		PC.4	MFPA	I/O	SPI1 Slave Select
		PD.1	MFPA	I/O	SPI1 Slave Select
		PD.6	MFPA	I/O	SPI1 Slave Select
		PF.0	MFPA	I/O	SPI1 Slave Select
TIMER0	T0	PA.2	MFP7	I	Timer0 event counter input / toggle output
		PB.3	MFP7	I	Timer0 event counter input / toggle output
		PE.6	MFP7	I	Timer0 event counter input / toggle output
TIMER1	T1	PB.4	MFP7	I	Timer1 event counter input / toggle output
		PB.6	MFPE	I	Timer1 event counter input / toggle output
		PE.3	MFP7	I	Timer1 event counter input / toggle output
TIMER2	T2	PA.1	MFP7	I	Timer2 event counter input / toggle output
		PB.2	MFPE	I	Timer2 event counter input / toggle output
		PC.6	MFP7	I	Timer2 event counter input / toggle output
EXT_OSC	EXT_CLK	PC.3	MFP1	A	External oscillator input pin.
UART1	UART1_TXD	PA.0	MFPB	O	UART1 data transmitter output pin.
		PB.0	MFPB	O	UART1 data transmitter output pin.
		PB.2	MFPB	O	UART1 data transmitter output pin.
		PC.0	MFPB	O	UART1 data transmitter output pin.
		PD.3	MFPB	O	UART1 data transmitter output pin.

Group	Pin Name	GPIO	MFP*	Type	Description
		PD.5	MFPE	O	UART1 data transmitter output pin.
		PE.5	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PA.1	MFPB	I	UART1 data receiver input pin.
		PB.1	MFPB	I	UART1 data receiver input pin.
		PB.3	MFPB	I	UART1 data receiver input pin.
		PC.1	MFPB	I	UART1 data receiver input pin.
		PC.2	MFPB	I	UART1 data receiver input pin.
		PD.4	MFPB	I	UART1 data receiver input pin.
		PD.6	MFPE	I	UART1 data receiver input pin.
		PE.6	MFPB	I	UART1 data receiver input pin.
UART2	UART2_TXD	PA.4	MFPB	O	UART2 data transmitter output pin.
		PB.4	MFPB	O	UART2 data transmitter output pin.
		PC.4	MFPB	O	UART2 data transmitter output pin.
		PC.6	MFPB	O	UART2 data transmitter output pin.
		PD.5	MFPF	O	UART2 data transmitter output pin.
		PD.7	MFPB	O	UART2 data transmitter output pin.
		PE.2	MFPB	O	UART2 data transmitter output pin.
		PE.7	MFPB	O	UART2 data transmitter output pin.
		PF.1	MFPB	O	UART2 data transmitter output pin.
	UART2_RXD	PA.5	MFPB	I	UART2 data receiver input pin.
		PB.5	MFPB	I	UART2 data receiver input pin.
		PD.6	MFPF	I	UART2 data receiver input pin.
		PE.0	MFPB	I	UART2 data receiver input pin.
		PE.3	MFPB	I	UART2 data receiver input pin.
		PF.0	MFPB	I	UART2 data receiver input pin.
		PF.2	MFPB	I	UART2 data receiver input pin.
ICE	ICE_DAT	PD.5	MFP1	I/O	Serial wired debugger data pin
	ICE_CLK	PD.1	MFP1	I	Serial wired debugger clock pin

Table 4.3-2 LQFP48/QFN48/QFN33 Multi-function Pin Summary

5 BLOCK DIAGRAM

5.1 NuMicro® NM1240 Block Diagram

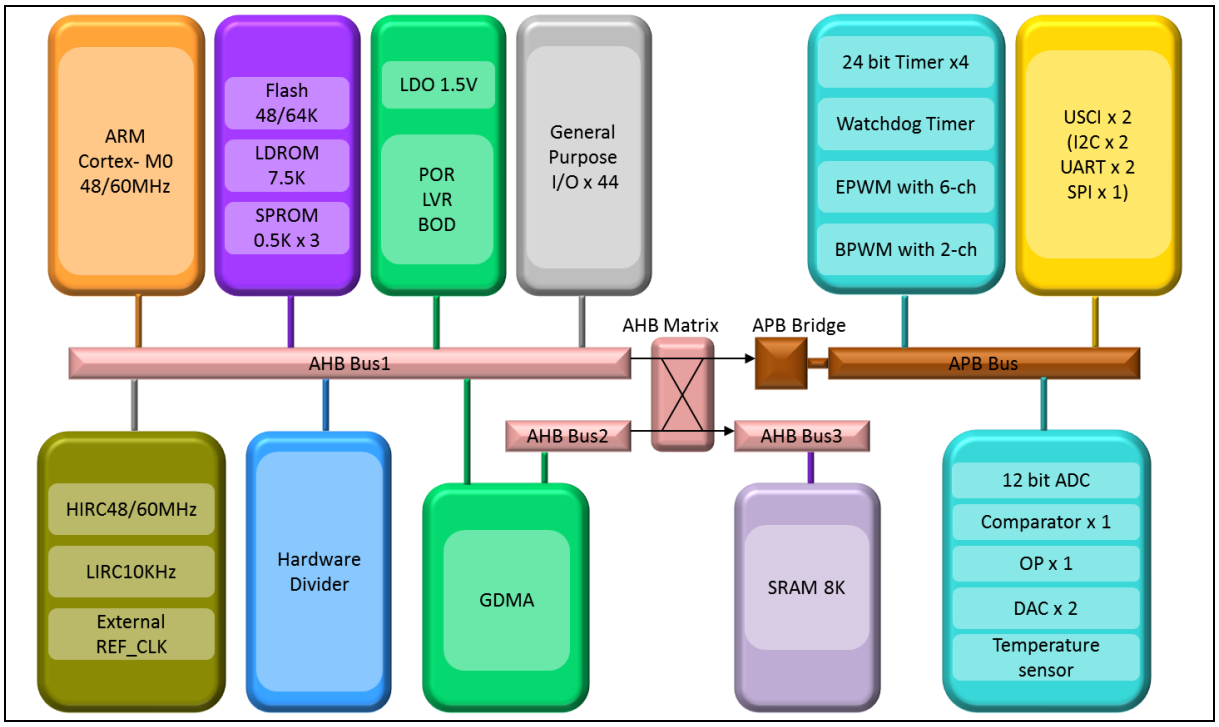


Figure 5.1-1 NuMicro® NM1240 Block Diagram

6 ELECTRICAL CHARACTERISTICS

For information on the NM1240 series electrical characteristics, please refer to NuMicro® NM1240 Series Datasheet.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	-	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	300	mA
	Maximum Current sourced by total I/O pins	-	300	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.2	-	5.5	V	V_{DD} = 2.2V ~ 5.5V up to 48 MHz V_{DD} = 3.0V ~ 5.5V up to 60 MHz			
V_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.21	1.23	1.25	V	V_{DD} = 2.2V ~ 5.5V, T_A = -40°C~105°C			
I_{DD}	Operating Current Normal Run Mode HCLK = 60 MHz while(1){} Executed from Flash	-	14.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	5.5V	X	60 MHz	X
I_{DD}		-	14.9	-	mA	3V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	3V	X	60 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	10.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	5.5V	X	48 MHz	X
I_{DD}		-	10.4	-	mA	3V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	3V	X	48 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	5.5V	24 MHz	X	X
I_{DD}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	3V	24 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD}		-	3.9	-	mA	3V	16 MHz	X	V

I_{DD}		-	3.0	-	mA	3V	16 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	3.1	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD}		-	2.5	-	mA	5.5V	12 MHz	X	X
I_{DD}		-	3.1	-	mA	3V	12 MHz	X	V
I_{DD}		-	2.4	-	mA	3V	12 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.5	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD}		-	1.3	-	mA	5.5V	4 MHz	X	X
I_{DD}		-	1.4	-	mA	3V	4 MHz	X	V
I_{DD}		-	1.2	-	mA	3V	4 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	184	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD}		-	182	-	µA	5.5V	32 KHz	V	X
I_{DD}		-	164	-	µA	3V	32 KHz	V	V[1]
I_{DD}		-	162	-	µA	3V	32 KHz	V	X
I_{DD}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	178	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD}		-	178	-	µA	5.5V	X	10 KHz	X
I_{DD}		-	158	-	µA	3V	X	10 KHz	V[2]
I_{DD}		-	158	-	µA	3V	X	10 KHz	X
I_{IDLE}	Operating Current Idle Mode HCLK= 60 MHz	-	8.3	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	3.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	8.3	-	mA	3V	X	V	V

I_{IDLE}		-	3.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK= 48 MHz	-	5.7	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	5.7	-	mA	3V	X	V	V
I_{IDLE}		-	2.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK = 24 MHz	-	2.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	5.5V	24 MHz	X	X
I_{IDLE}		-	2.9	-	mA	3V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	3V	24 MHz	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 16 MHz	-	2.2	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE}		-	2.1	-	mA	3V	V	X	V
I_{IDLE}		-	1.3	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 12 MHz	-	1.8	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.1	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.7	-	mA	3V	V	X	V
I_{IDLE}		-	1.1	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 4 MHz	-	1.0	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	0.8	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.0	-	mA	3V	V	X	V

I_{IDLE}		-	0.7	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 10 kHz	-	147	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{IDLE}		-	147	-	µA	5.5V	X	V	X
I_{IDLE}		-	127	-	µA	3V	X	V	V[2]
I_{IDLE}		-	126	-	µA	3V	X	V	X
I_{PWD}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD}		-	0.8	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			
V_{IL1}	Input Low Voltage (TTL Input)	0.8	1.42		V	V_{DD} = 5.5 V			
		0.8	1.08			V_{DD} = 3.3 V			
V_{IH1}	Input High Voltage (TTL Input)		1.42	2.0	V	V_{DD} = 5.5 V			
			1.08	2.0		V_{DD} = 3.3 V			
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-			
R_{UP}[3]	Internal Pull-up Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{LOW}[3]	Internal Pull-low Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.2 V ~ 5.5V			
V_{ILS}	Negative-going Threshold (Schmitt input)	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt input)	$0.7V_{DD}$	-	-	V	-			
I_{IL}	Logic 0 Input Current (Quasi-bidirectional Mode)	-	-63.65		µA	V_{DD} = 5.5 V, V_{IN} = 0V			
I_{TL}	Logic 1 to 0 Transition Current	-	-566.7	-	µA	V_{DD} = 5.5 V			
I_{SR}	Source Current (Quasi-bidirectional Mode)	-	-372	-	µA	V_{DD} = 4.5 V, V_{IN} = 2.4 V			
I_{SR}		-	-76.8	-	µA	V_{DD} = 2.7 V, V_{IN} = 2.2 V			
I_{SR}		-	-37.3	-	µA	V_{DD} = 2.2 V, V_{IN} = 1.8 V			

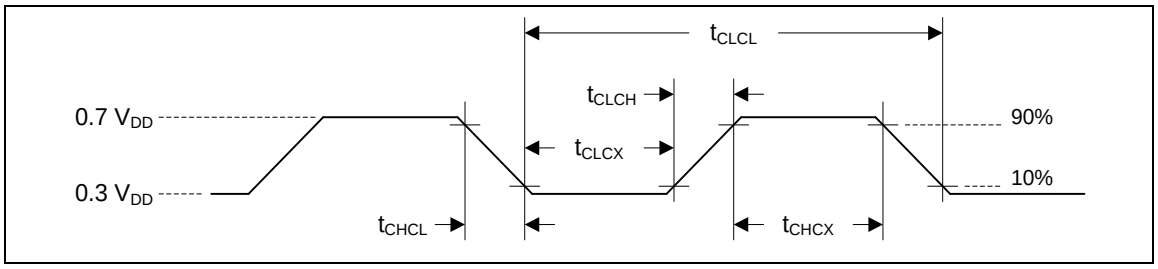
I_{SR}	Source Current (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-2	-	mA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SK}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.2 V, V_{IN} = 0.4 V

Notes:

1. Only enable modules, which support 32 kHz EXT_CLK source
2. Only enable modules, which support 10 kHz LIRC clock source.
3. Guaranteed by design, not test in production.

6.3 AC Electrical Characteristics

6.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

6.3.2 External Clock Input (EXT_CLK) (up to 24MHz)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{EXT_CLK}	Operation Voltage	2.2	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
F_{EXT_CLK}	Clock Frequency	-	-	24	MHz	-

6.3.3 48/60 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC60}	Center Frequency	-	60	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD}=4.5 V~ 5.5 V
		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=3.0 V~ 5.5 V
f_{HRC48}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD} = 5.5 V

		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=2.2 V~ 5.5 V

6.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-5[1]	-	+5[1]	%	V_{DD} = 2.2 V ~ 5.5 V T_A = -40℃ ~ +105℃

Note1: These parameters are characterized but not tested.

6.4 Analog Characteristics

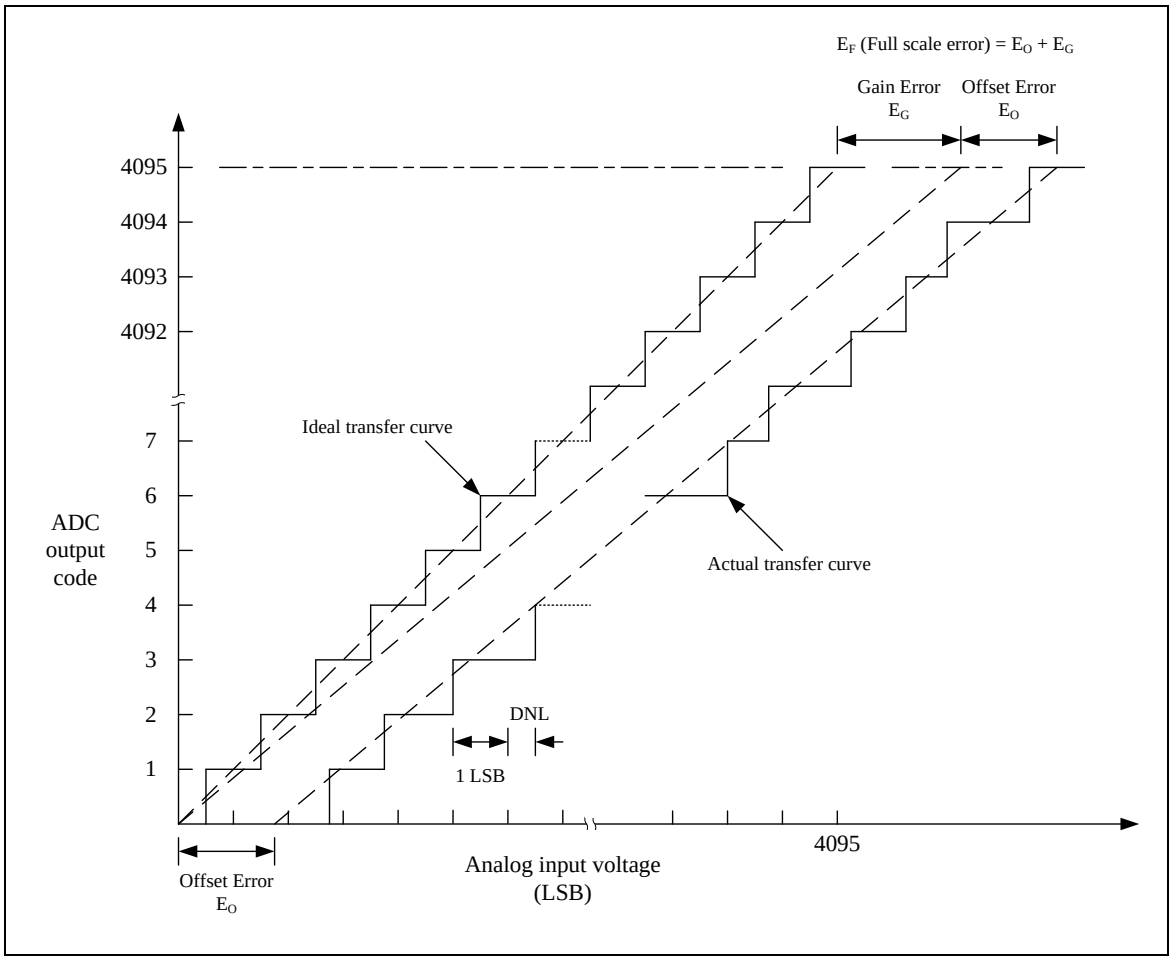
6.4.1 12-bit SAR ADC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		300			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]		800	1000	ns	V_{DD} = 3.0~5.5 V
I_{DDA}	Operation Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	V_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-

Note:

1. ADC voltage reference is same with V_{DD} .
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of C_{IN} is less than about 10% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 800ns at V_{DD} = 5V.


E_F (Full scale error) = E_O + E_G
Gain Error E_G
Offset Error E_O
4095
4094
4093
4092
7
6
5
4
3
2
1
ADC output code
Ideal transfer curve
Actual transfer curve
DNL
1 LSB
4095
Offset Error E_O
Analog input voltage (LSB)

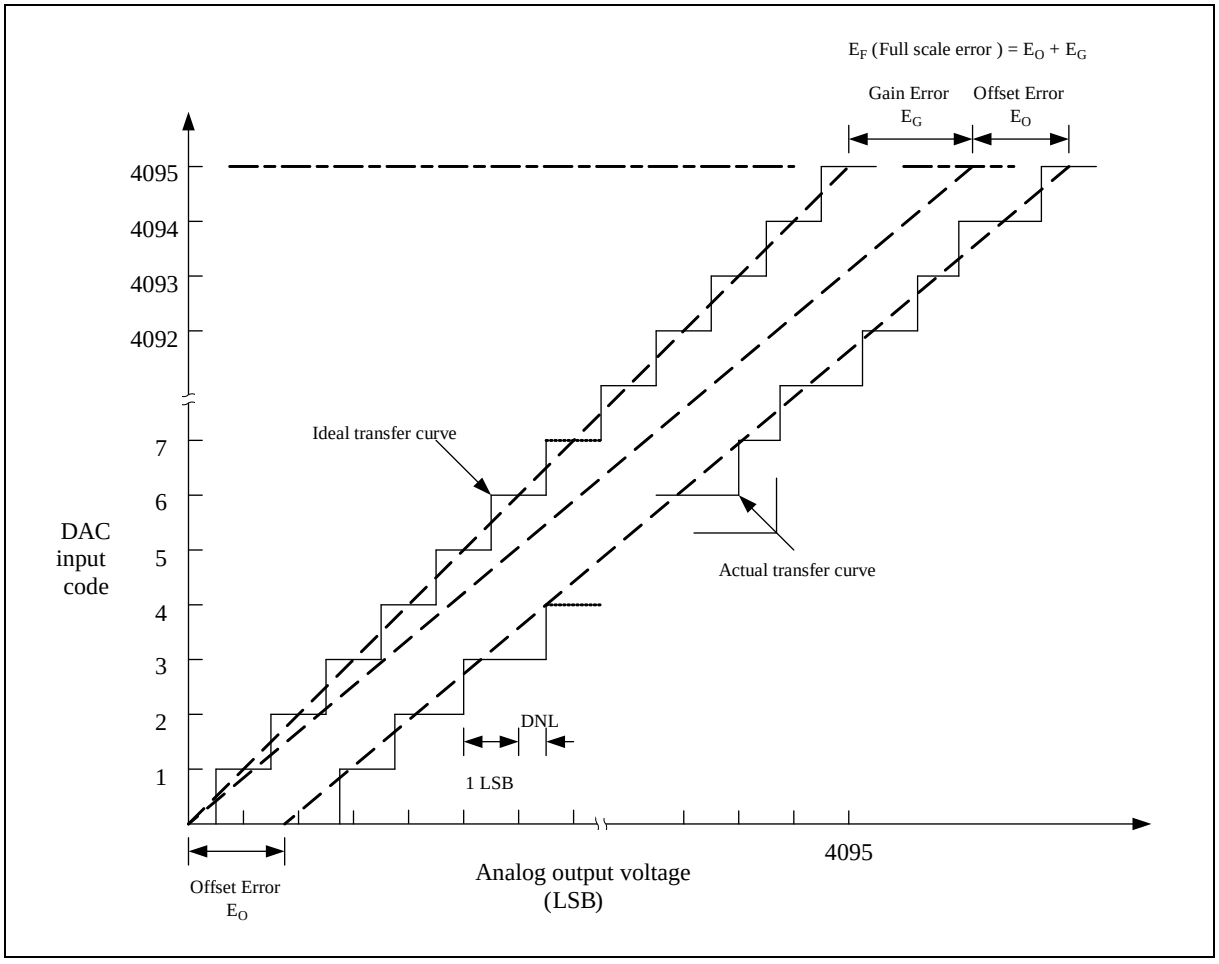
6.4.2 12-bit SAR DAC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±4	-	LSB	V_{DD} = 5V
INL	Integral Nonlinearity Error	-	±3	-	LSB	V_{DD} = 5V
E_O	Offset Error	-	3	-	LSB	V_{DD} = 5V
E_G	Gain Error (Transfer Gain)	-	3	-	LSB	V_{DD} = 5V
I_{DDA}	Operation Current (Avg.)	-	100	-	uA	V_{DD} = 5V
V_{out}	Analog output Voltage	0	-	V_{DD}	V	-

Note:

1. DAC voltage reference is the same with V_{DD}.



6.4.3 DAC Output buffer

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
Slew rate	3.0	-	-	V/us	V_{DD} = 5V, RLOAD = 33K, CLOAD = 50p
Output Current		3		mA	V_{DD} - 0.3 ~ V_{SS} + 0.3, V_{DD} = 3~5V
Power consumption		200		uA	V_{DD} = 5V

6.4.4 LDO & Power Management

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LDO}	Output Voltage	1.35	1.5	1.65	V	-

Notes:

It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

6.4.5 Brown-out Detector

(V_{DD} – V_{SS} = 0 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{BOD}	Brown-out Hysteresis	30	100	150	mV	
V_{BOD}	Brown-out Detector	4.15	4.3	4.45	V	BOV_VL [2:0] = 7
		3.85	4.0	4.15	V	BOV_VL [2:0] = 6
		3.55	3.7	3.85	V	BOV_VL [2:0] = 5
		2.85	3.0	3.15	V	BOV_VL [2:0] = 4
		2.55	2.7	2.85	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

6.4.6 Power-on Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{POR}	Threshold Voltage	1.60	1.75	1.90	V	-
V_{LVRLPM}	Threshold Voltage(Low Power)	1.3	1.6	2.1	V	-

6.4.7 LVR Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LVR}	Threshold Voltage(high→low)	1.7	1.9	2.1	V	-
V_{LVRHYS}	Hysteresis Voltage	-	-	100	mV	

6.4.8 Comparator

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	V_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	
V_{HYS}	Hysteresis	10	20	30	mV	ACMPHYSEN = 01
V_{HYS}	Hysteresis	60	90	120	mV	ACMPHYSEN = 10
V_{HYS}	Hysteresis	95	150	200	mV	ACMPHYSEN = 11
T_{STB}	Stable time	-	1.06	-	µs	

Notes:

Guaranteed by design, not test in production.

6.4.9 OP Amplifier

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
PSRR+	-	90	-	dB	VDD=5V
CMRR	-	90	-	dB	VDD=5V
Slew rate	6.0	-	-	V/us	VDD=5V, RLOAD=33K, CLOAD=50p
Wake up time	-	-	1	us	
Maximum output voltage swing from rail		20		mV	V_{DD} =5.5, RL=10K
		100		mV	V_{DD} =5.5, RL=2K
Open-loop output implement		200		ohm	V_{DD} =5, f=10MHz
Close-loop output implement		95		ohm	V_{DD} =5, f=10MHz

6.4.10 Temperature Sensor

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1],	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	715	-	mV	TA = 0 ℃

Note:

1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

6.4.11 ESD Characteristics

Symbol	Ratings	Condition	Package	Maximum Value	Unit
V_{ESD}	Electrostatic discharge (Human body mode)	TA = + 25 ℃	LQFP 48	6000	V
	Electrostatic discharge (Charged Device mode)			500	V

6.4.12 EFT Characteristics

Symbol	Condition	Package	Pass Level	Unit
	Fsys			
	HIRC	LQFP 48	+/- 4000	V

6.5 Flash DC Electrical Characteristics

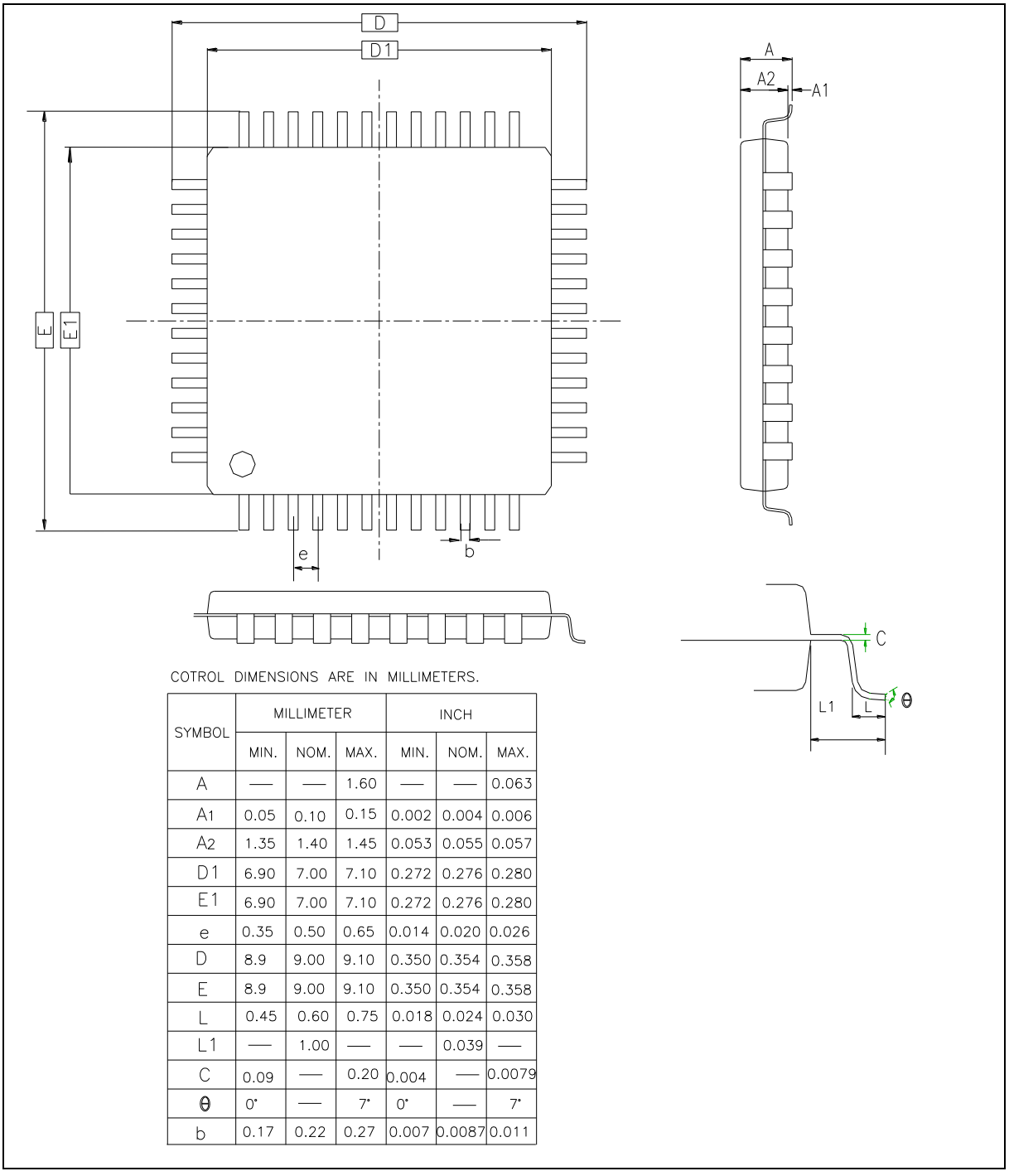
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	5	6.5	us	Per Byte
I_{DD1}	Read Current	-	4	5.5	mA	@50MHz
I_{DD2}	Program Current	-	-	3.5	mA	
I_{DD3}	Erase Current	-	-	2	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
   Guaranteed by design, not test in production.

7 PACKAGE DIMENSIONS

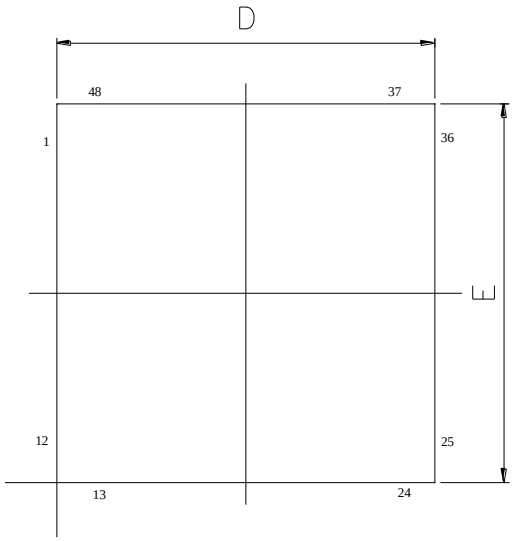
7.1 48-Pin LQFP (7mm x 7mm)

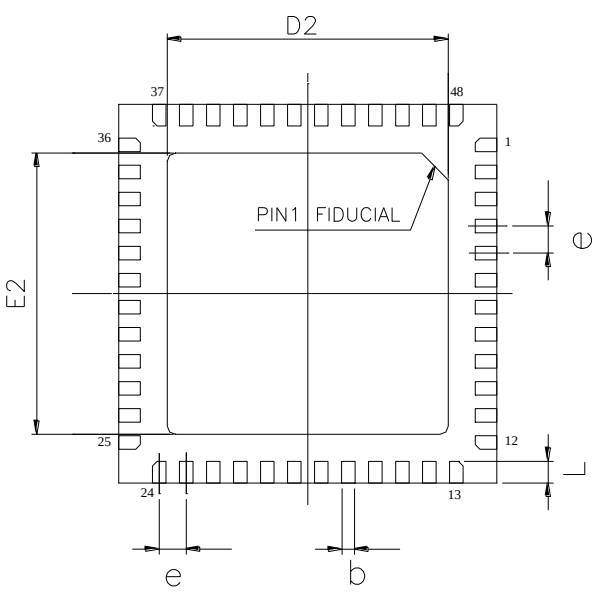


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

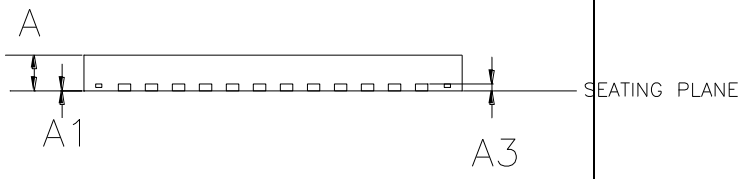
7.2 48-Pin QFN (7mm x 7mm)





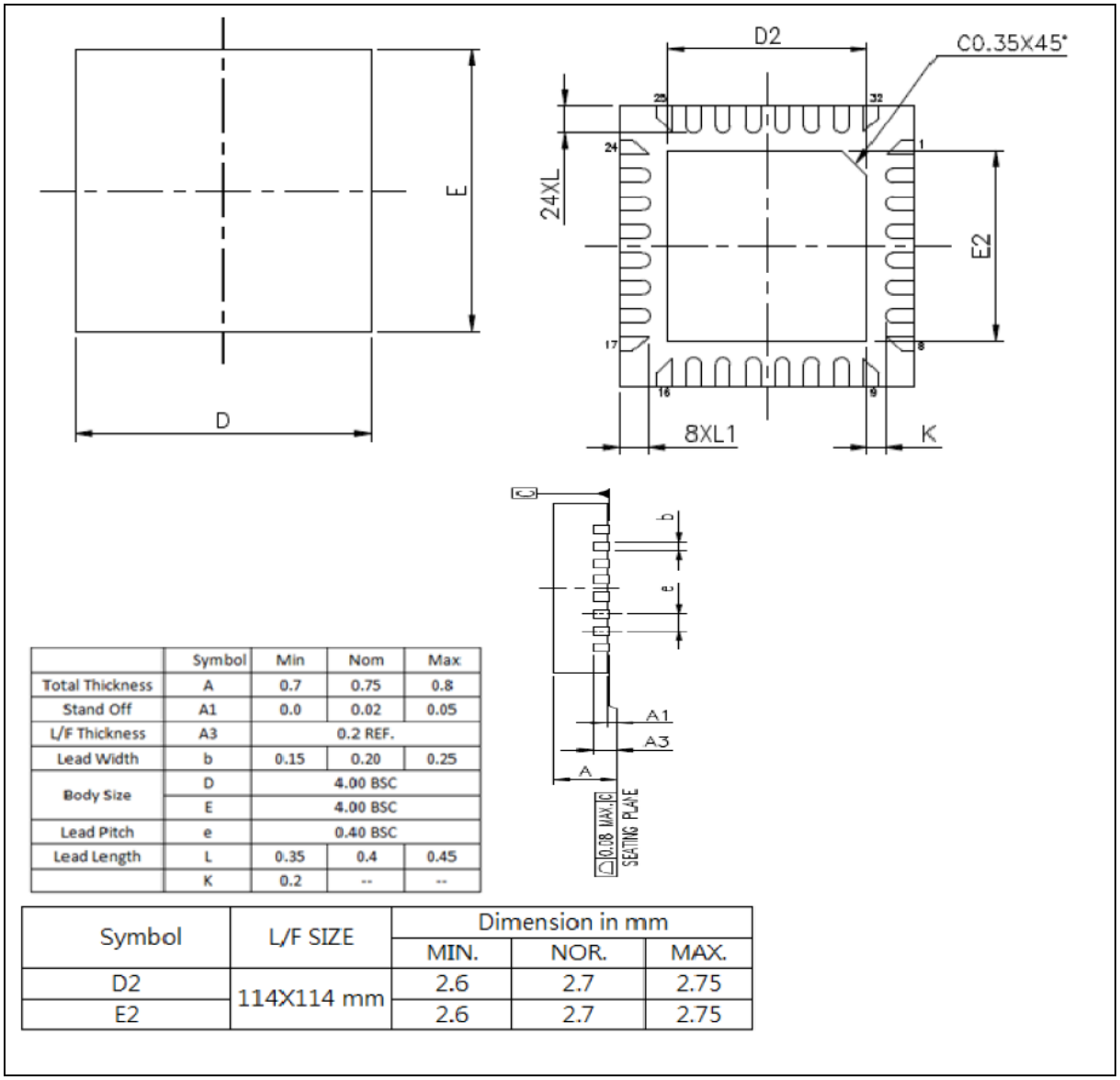
Controlling Dimension :Millimeters

SYMBOL	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.61	0.66	0.70	0.024	0.026	0.028
A1	0	0.02	0.05	0	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	7.00 BSC			0.276 BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00 BSC			0.276 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.08			0.003		



*D2,*E2 :By die size difference

7.3 33-pin QFN33 (4 mm x 4 mm)



	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

8 REVISION HISTORY

Date	Revision	Description
2020.07.22	0.1	Preliminary version
2020.09.03	0.1	1. Modify GDMA in Features 2. Modify the Selection Guide 3. Modify the Electrical Characteristics
2020.09.28	0.1	1. Correct the 1000ns to 800ns in the note of section 6.4.1 12-bit SAR ADC
2020.12.08	0.1	1. Remove the parts of NM1243 series
2021.03.10	0.1	1. Modify the ADC Block Diagram
2021.10.01	0.1	1. Update the ESD and EFT characteristics