ARM Cortex®-M0

32-BIT MICROCONTROLLER

NM18407 Series Product Brief

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1 GENERAL DESCRIPTION

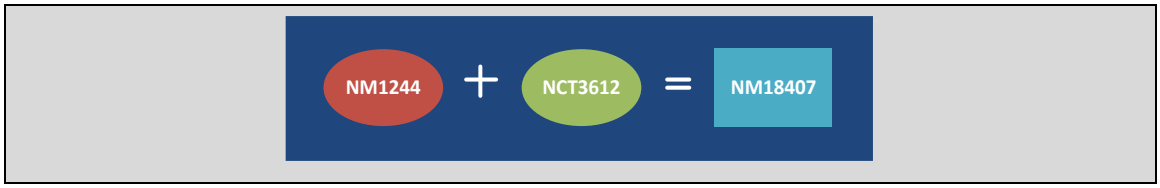
The NM18407 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and monolithic half-bridge gate driver for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NM1244 series can run up to 48(60) MHz and operate at 2.2V(3.3V) ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NM1244 offers 64 Kbytes embedded program Flash, size configurable Data Flash (shared with program flash), 7.5 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 8Kbytes SRAM. Plentiful system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, DAC, OP, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM18407 to reduce component count, board space and system cost.

The power supply input of NM18407 is up to 35V. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component.

Additionally, the NM18407 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM18407 is the combination of MCU NM1244 and Gate Driver NCT3612. User may refer to the TRM of NM1244 and the datasheet of NCT3612 for the detailed specification. The NM1244 BSP is also for NM18407 software developing.



2 FEATURES

- Recommended operation Supply Voltage VIN Range from 8 to 35V
- Gate Driver
  - 8 ~ 35V Operate Supply Voltage Range from VIN
  - 7 ~ 12V voltage range from GD_VDD(Gate driver power input)
  - 250mA Source & 500mA Sink Gate Drive Current Capability @VIN > 20V
  - Integrated 1 LDO
    - 5V, 35mA, LDO Output for MCU power supply(Note1)
  - Integrated bootstrap diode
  - Protection:
    - UVLO (Under Voltage Lockout)
    - Thermal Shutdown Protection (typically @165℃)
- MCU Core
  - ARM® Cortex™-M0 core running up to 48/60 MHz by internal RC oscillator
  - One 24-bit system tick timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Memory
  - 64 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 7.5 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM0, 1, 2)
  - 8 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - 48(60) MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 28 general-purpose I/O (GPIO) pins
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence

- Optional TTL/Schmitt trigger input
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink I/O mode
- GPIO built-in Pull-up/Pull-low resistor for selection

- Timer
  - Provides four channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides four operation modes: One-shot, Periodic, Toggle and Continuous
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
- Continuous Capture
  - Timer0, Timer1, Timer2 and Systick provided with continuous capture function to capture at most 4 edges continuously on one signal
- ECAP (Enhanced Input Capture)
  - One units of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP ports(ECAP0, ECAP1 and ECAP2)
    - ACMP Trigger
- GDMA (General Direct Memory Access)
  - Two channels
  - Memory to/from memory or APB device
  - Memory to/from USCI TX/RX buffer which supports the hardware trigger
  - Supports “4-data burst” mode to boost performance
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Support a built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/synchronous/independent/ complementary modes

- Supports One-shot PWM function
- Supports Edge-aligned and Center-aligned PWM type
- Support Asymmetric mode
- Programmable dead-zone insertion between complementary channels
- Each output has independent polarity setting control
- Hardware fault brake and software brake protections
- Supports rising, falling, central, period, and fault break interrupts
- Supports duty/period trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function
- Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

- BPWM (Basic PWM Generator)
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
  - Synchronous mode for BPWM and EPWM
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - USCI1 Supports to be configured as UART, SPI or I²C individually
  - USCI2 Supports to be configured as UART and I²C individually
  - Supports programmable baud-rate generator
  - Supports GDMA trasfer
- 12-bit ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 800ns conversion time
  - Supports 2 S/H (sample/hold)
  - Up to 17-ch single-end input from I/O and one internal input from band-gap.
  - Each input channel has own data register

- Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
- Supports temperature sensor for measurement chip temperature
- Supports independent and simultaneous conversion modes

- OP Amplifier
  - Rail-to-rail OPA x 1
- DAC
  - Built-in two of 12-bit DAC,
  - Be the reference voltage for ACMP, ADC or output to pins.
- Analog Comparator
  - One analog comparators with 4 reference voltage source
    - Built-in 12-bit DAC0 and DAC1 for comparator reference voltage
    - Band-gap voltage
    - External voltage from port pin
  - Supports Hysteresis function 0/20/90/150mV at V_{DD} = 5V
  - Interrupt when compared result changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
  - Support 3 group of independent dividend, divisor, quotient and remainder registers for three times of calculation capacity
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: ESD HBM pass 2 kV; ESD 2 kV
- Packages:
  - Green package (RoHS)

- 48-pin QFN, 7mm x 7mm

Note:

1. Higher LDO output current causes the higher IC temperature. Refer to section 5.9 NCT3612 DC Electrical Characteristics

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NM18407 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48/60 MHZ	BOD	PWM	Analog Comp.	OPA	DAC (12-Bit)	ADC (12-Bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI												
							UART*	I^2C	SPI										
NM18407Y	64	8	7.5	√	29	3	2	2	1	1	1	6	2	1	2	17x 12bit	1	√	QFN 48 (7x7mm)

Table 3.1-1 NM18407 Base Series Selection Guide

3.2 Pin Configuration

3.2.1 NM18407Y QFN48 Pin Diagram

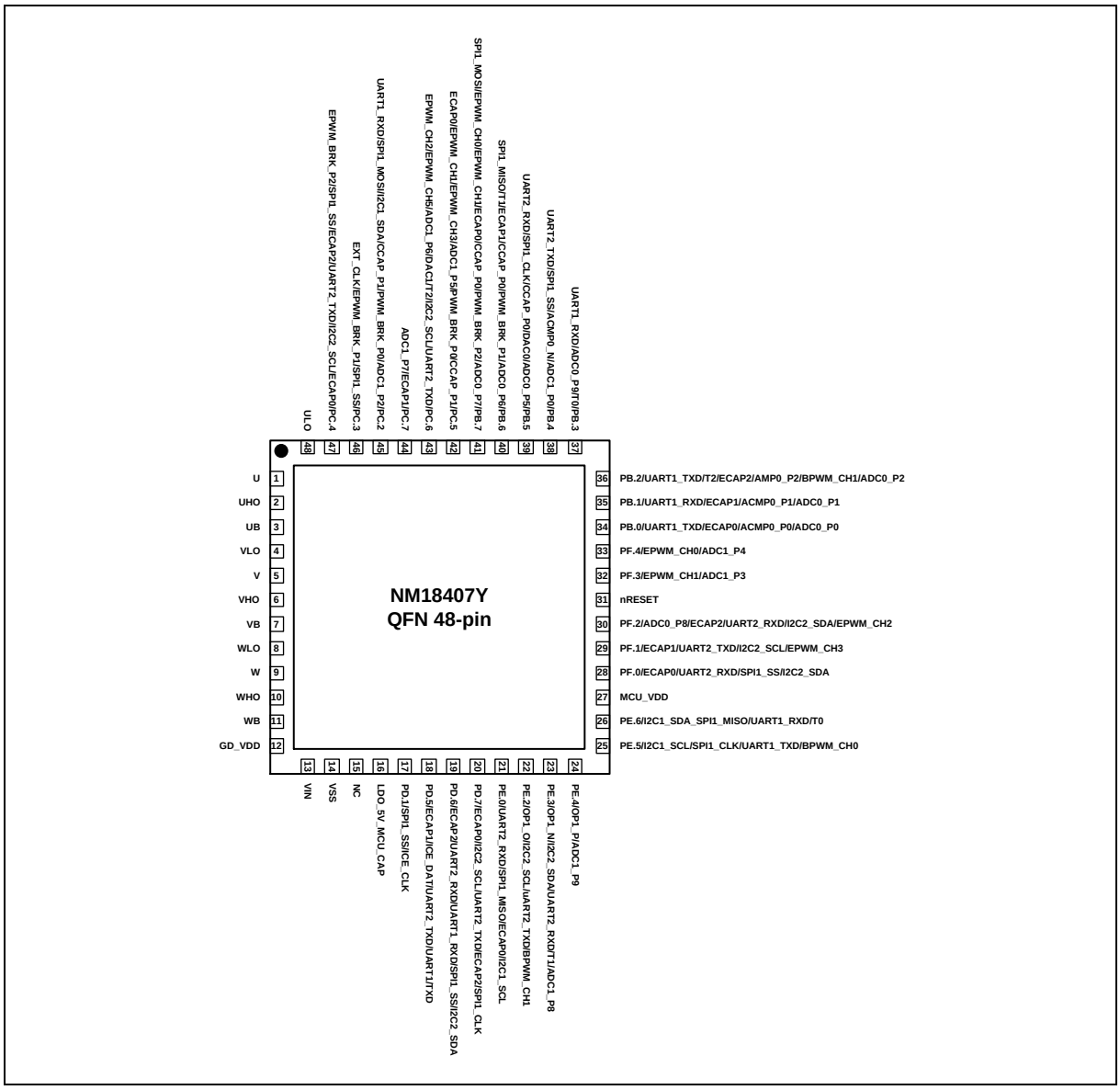


Figure 3.2-1 NM18407Y QFN48 pin Diagram

3.3 Pin Description

3.3.1 NM18407Y Series QFN48 Pin Description

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
-	21	1	U	HI	U-Phase input. It should be connected to U-phase high-side MOSFET source and low-side FET drain.
-	22	2	UHO	HO	Output for U-phase high-side MOSFET. Connect to U-phase high-side MOSFET gate.
-	23	3	UB	HP	U-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and U.
-	24	4	VLO	HO	Output for V-phase low-side MOSFET. Connect to V-phase low-side MOSFET gate.
-	25	5	V	HI	V-Phase input. It should be connected to V-phase high-side MOSFET source and low-side FET drain
-	26	6	VHO	HO	Output for V-phase high-side MOSFET. Connect to V-phase high-side MOSFET gate.
-	27	7	VB	HP	V-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and V.
-	28	8	WLO	HO	Output for W-phase low-side MOSFET. Connect to W-phase low-side MOSFET gate.
-	1	9	W	HI	W-Phase input. It should be connected to high-side MOSFET source and low-side FET drain.
-	2	10	WHO	HO	Output for W-phase high-side MOSFET. Connect to W-phase high-side MOSFET gate.
-	3	11	WB	HP	W-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and W.
-	-	12	GD_VDD	P	Gate driver power input. Recommended voltage range is 7V~12V.
-	5	13	VIN	HP	Power supply for internal control circuit. Recommend connect a capacitor to GND to stabilize the input power.
-	6	14	VSS	P	Ground pin for gate driver
-	-	15	NC		No connection

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
-	7	16	LDO_5V_MCU_CAP	P	5V LDO OUT for MCU(5VOUT). Recommend connect a 1uF capacitor to GND.
34	-	17	PD.1	I/O	General purpose digital I/O pin.
			ICE_CLK	I	Serial wired debugger clock pin.
			SPI1_SS	I/O	SPI1 slave select pin.
37	-	18	PD.5	I/O	General purpose digital I/O pin.
			ICE_DAT	I/O	Serial wired debugger data pin.
			ECAP1	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			UART2_TXD	I/O	Data transmitter output pin for UART.
38	-	19	PD.6	I/O	General purpose digital I/O pin.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			ECAP2	I	Enhanced Input Capture input pin.
			UART1_RXD	I	Data receiver input pin for UART.
			UART2_RXD	I/O	Data receiver input pin for UART.
39	-	20	PD.7	I/O	General purpose digital I/O pin.
			ECAP0	I	Enhanced Input Capture input pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
40	-	21	PE.0	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.
42	-	22	PE.2	I/O	General purpose digital I/O pin.
			BPWM_CH1	O	BPWM channel1 output/capture input.

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
			OP1_O	A	Operational Amplifier output pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	O	Data transmitter output pin for UART.
43	-	23	PE.3	I/O	General purpose digital I/O pin.
			ADC1_P8	A	ADC1 channel analog input.
			OP1_N	A	Operational Amplifier Negitive input pin.
			T1	I/O	Timer1 event counter input / toggle output.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			UART2_RXD	I	Data receiver input pin for UART.
44	-	24	PE.4	I/O	General purpose digital I/O pin.
			ADC1_P9	A	ADC1 channel analog input.
			OP1_P	A	Operational Amplifier Positive input pin.
45	-	25	PE.5	I/O	General purpose digital I/O pin.
			BPWM_CH0	O	BPWM channel0 output/capture input.
			I2C1_SCL	I/O	I2C1 clock pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART1_TXD	O	Data transmitter output pin for UART.
46	-	26	PE.6	I/O	General purpose digital I/O pin.
			T0	I/O	Timer0 event counter input / toggle output.
			I2C1_SDA	I/O	I2C1 data input/output pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
			UART1_RXD	I	Data receiver input pin for UART.
48	-	27	MCU_VDD	P	
4	-	28	PF.0	I/O	General purpose digital I/O pin.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
5	-	29	PF.1	I/O	General purpose digital I/O pin.
			EPWM_CH3	O	EPWM channel3 output/capture input.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP1	I	Enhanced Input Capture input pin.
6	-	30	PF.2	I/O	General purpose digital I/O pin.
			ADC0_P8	A	ADC0 channel analog input.
			EPWM_CH2	O	EPWM channel2 output/capture input.
			I2C2_SDA	I/O	I2C2 data input/output pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
7	-	31	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
8	-	32	PF.3	I/O	General purpose digital I/O pin.
			ADC1_P3	A	ADC1 channel analog input.
			EPWM_CH1	O	EPWM channel1 output/capture input.
9	-	33	PF.4	I/O	General purpose digital I/O pin.
			ADC1_P4	A	ADC1 channel analog input.
			EPWM_CH0	O	EPWM channel0 output/capture input.
10	-	34	PB.0	I/O	General purpose digital I/O pin.
			ADC0_P0	A	ADC0 channel analog input.
			ACMP0_P0	A	Analog comparator0 positive input pin.
			ECAP0	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			ECAP0	I	Enhanced Input Capture input pin.
11	-	35	PB.1	I/O	General purpose digital I/O pin.
			ADC0_P1	A	ADC0 channel analog input.
			ACMP0_P1	A	Analog comparator0 positive input pin.
			ECAP1	I	Enhanced Input Capture input pin.

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
			UART1_RXD	I	Data receiver input pin for UART.
			ECAP1	I	Enhanced Input Capture input pin.
12	-	36	PB.2	I/O	General purpose digital I/O pin.
			ADC0_P2	A	ADC0 channel analog input.
			BPWM_CH1	O	BPWM channel1 output/capture input.
			ACMP0_P2	A	Analog comparator0 positive input pin.
			ECAP2	I	Enhanced Input Capture input pin.
			UART1_TXD	O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
			T2	I/O	Timer2 event counter input / toggle output.
13	-	37	PB.3	I/O	General purpose digital I/O pin.
			ADC0_P9	A	ADC0 channel analog input.
			T0	I/O	Timer0 event counter input / toggle output.
			UART1_RXD	I	Data receiver input pin for UART.
14	-	38	PB.4	I/O	General purpose digital I/O pin.
			ADC1_P0	A	ADC1 channel analog input.
			ACMP0_N	A	Analog comparator0 negative input pin.
			T1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
15	-	39	PB.5	I/O	General purpose digital I/O pin.
			ADC0_P5	A	ADC0 channel analog input.
			DAC0	A	DAC0 analog output.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
			UART2_RXD	I/O	Data receiver input pin for UART.
16	-	40	PB.6	I/O	General purpose digital I/O pin.
			ADC0_P6	A	ADC0 channel analog input.

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
			PWM_BRK_P1	I	Brake input pin of EPWM.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
			ECAP1	I	Enhanced Input Capture input pin.
			T1	I/O	Timer1 event counter input / toggle output.
17	-	41	PB.7	I/O	General purpose digital I/O pin.
			ADC0_P7	A	ADC0 channel analog input.
			PWM_BRK_P2	I	Brake input pin of EPWM.
			CCAP_P0	I	Timer Continuous Capture input pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			ECAP0	I	Enhanced Input Capture input pin.
			EPWM_CH0	O	EPWM channel0 output/capture input.
			EPWM_CH1	O	EPWM channel1 output/capture input.
18	-	42	PC.5	I/O	General purpose digital I/O pin.
			ADC1_P5	A	ADC1 channel analog input.
			PWM_BRK_P0	I	Brake input pin of EPWM.
			CCAP_P1	I	Timer Continuous Capture input pin.
			ECAP2	I	Enhanced Input Capture input pin.
			EPWM_CH1	O	EPWM channel1 output/capture input.
			EPWM_CH3	O	EPWM channel3 output/capture input.
19	-	43	PC.6	I/O	General purpose digital I/O pin.
			ADC1_P6	A	ADC1 channel analog input.
			EPWM_CH2	O	EPWM channel2 output/capture input.
			DAC1	O	DAC1 analog output.
			T2	I/O	Timer2 event counter input / toggle output.
			I2C2_SCL	I/O	I2C2 clock pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			EPWM_CH5	O	EPWM channel5 output/capture input.

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
20	-	44	PC.7	I/O	General purpose digital I/O pin.
			ADC1_P7	A	ADC1 channel analog input.
			ECAP1	I	Enhanced Input Capture input pin.
23	-	45	PC.2	I/O	General purpose digital I/O pin.
			ADC1_P2	A	ADC1 channel analog input.
			PWM_BRK_P0	I	Brake input pin of EPWM.
			CCAP_P1	I	Timer Continuous Capture input pin.
			I2C1_SDA	I/O	I2C1 data input/output pin.
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
			UART1_RXD	I	Data receiver input pin for UART.
24		46	PC.3	I/O	
			REF_CLK	I	
			PWM_BRK_P1	I	
			SPI1_SS	I/O	
25		47	PC.4	I/O	General purpose digital I/O pin.
			PWM_BRK_P2	I	Brake input pin of EPWM.
			ECAP0	I	Enhanced Input Capture input pin.
			I2C2_SCL	I/O	I2C2 clock pin.
			SPI1_SS	I/O	SPI1 slave select pin.
			UART2_TXD	I/O	Data transmitter output pin for UART.
			ECAP2	I	Enhanced Input Capture input pin.
-	20	48	ULO	HO	Output for U-phase low-side MOSFET. Connect to U-phase low-side MOSFET gate.
31[3]	11	-	-		PWM0 (PA.5) connect to HIN_U
29[3]	12	-	-		PWM1 (PA.4) connect to LIN_U
28[3]	13	-	-		PWM2 (PA.3) connect to HIN_V
27[3]	14	-	-		PWM3 (PA.2) connect to LIN_V
26[3]	15	-	-		PWM4 (PA.1) connect to HIN_W
25[3]	16	-	-		PWM5 (PA.0) connect to LIN_W
-	8	-	-		LV_O of gate drive is no bonding
-	9	-	-		LV_I of gate drive is no bonding
-	10				RSTB of gate driver is no bonding

NM1244Y48 QFN48 7x7	NCT3612 QFN28 4x4	NM18407Y QFN48 7x7	Pin Name	Pin Type	Description
-	17	-	-		DIR of gate driver is no bonding
	18	-	-		HV_I/O of gate drive is no bonding
-	19	-	-		no connect

Table 3.3-1 NM18407Y QFN48 Pin Description

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

[3] GPA0 ~ GPA5 are set as EPWM5 ~ EPWM0 in NM18407Y

4 BLOCK DIAGRAM

4.1 NM18407 Block Diagram

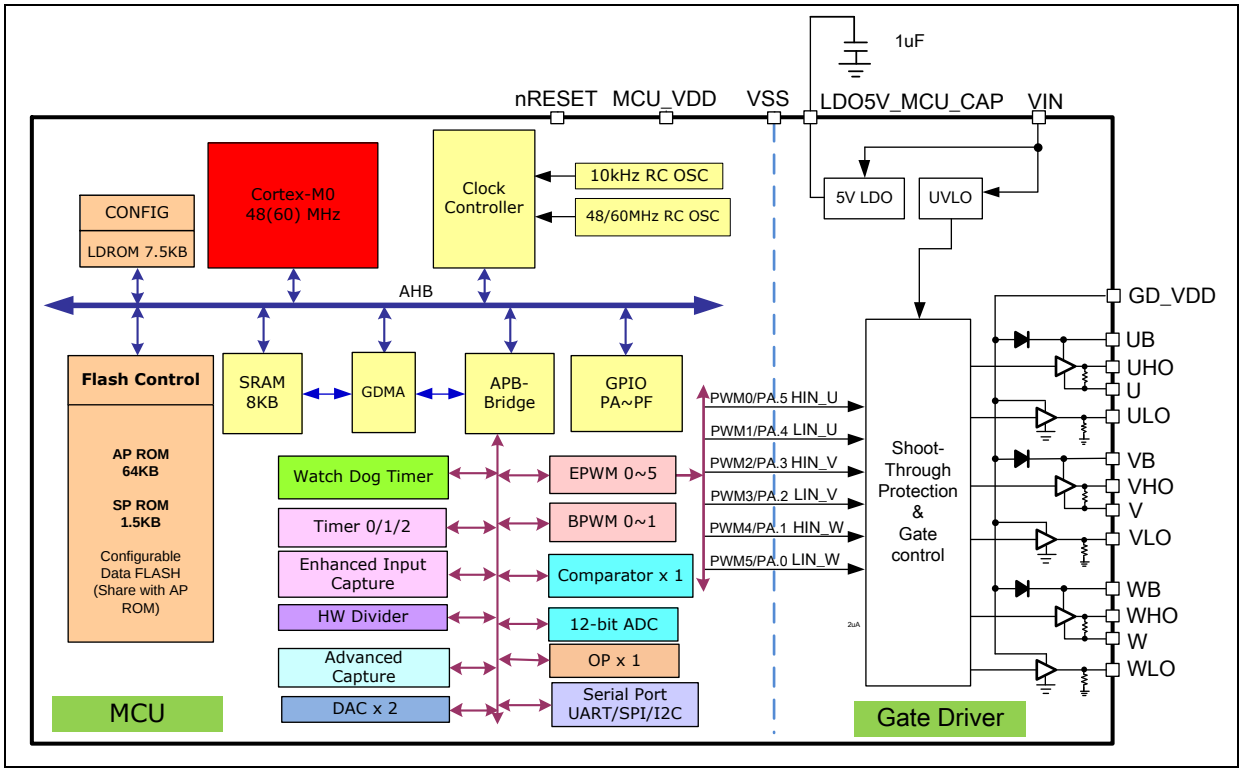
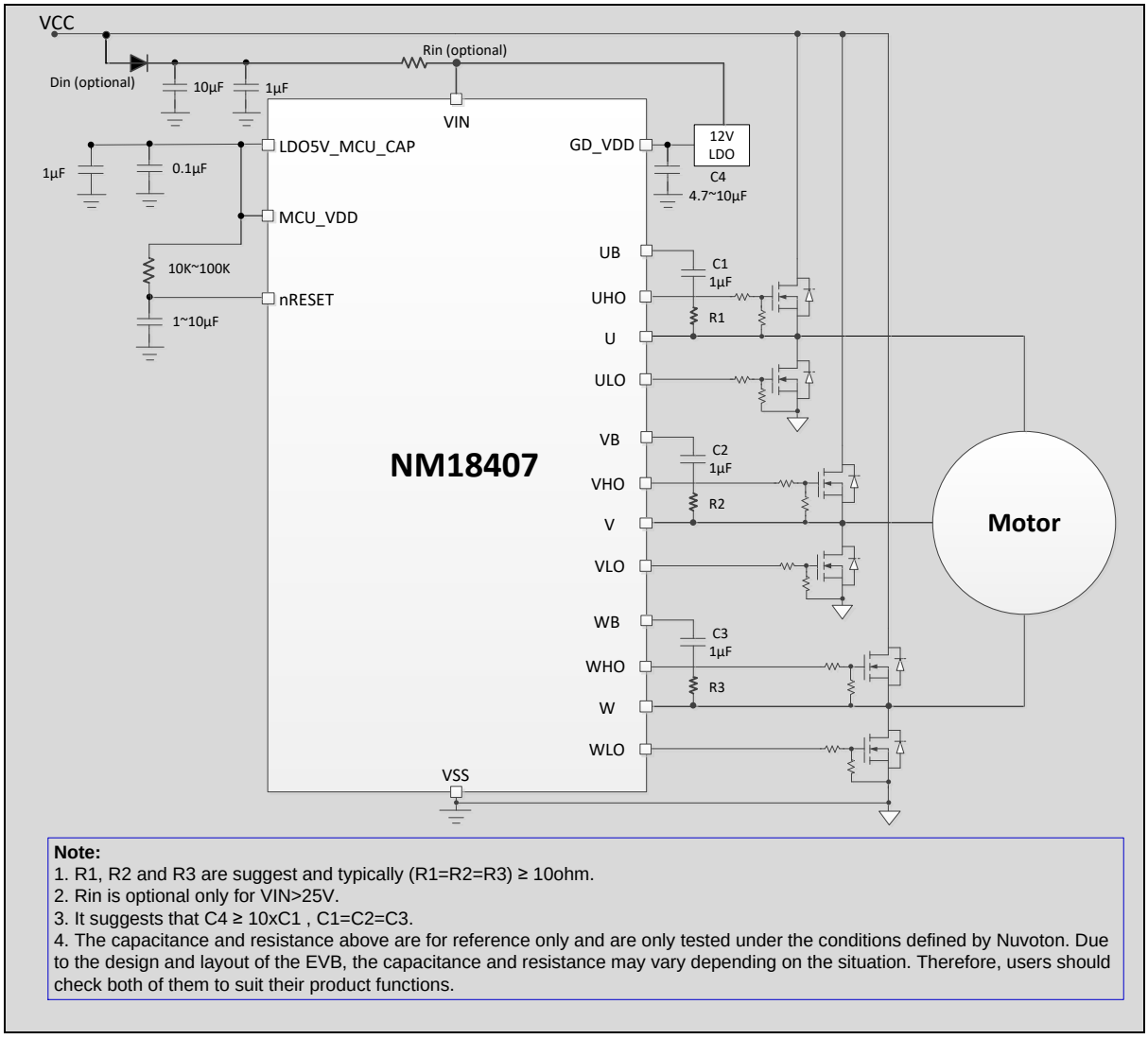


Figure 4.1-1 NM18407 Series Block Diagram

4.2 NM18407 Application Circuit



Note:
1. R1, R2 and R3 are suggest and typically (R1=R2=R3) ≥ 10ohm.
2. Rin is optional only for VIN>25V.
3. It suggests that C4 ≥ 10xC1 , C1=C2=C3.
4. The capacitance and resistance above are for reference only and are only tested under the conditions defined by Nuvoton. Due to the design and layout of the EVB, the capacitance and resistance may vary depending on the situation. Therefore, users should check both of them to suit their product functions.

Figure 4.2-1 NM18407 Application Circuit

5 NM18407 ELECTRICAL CHARACTERISTICS

The data is for reference only. Please refer to the TRM of NM1244 and the datasheet of NCT3612 for the detailed electrical characteristics.

5.1 NM1244 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	-	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	300	mA
	Maximum Current sourced by total I/O pins	-	300	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

5.2 NM1244 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.2	-	5.5	V	V_{DD} = 2.2V ~ 5.5V up to 48 MHz V_{DD} = 3.0V ~ 5.5V up to 60 MHz			
V_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.21	1.23	1.25	V	V_{DD} = 2.2V ~ 5.5V, T_A = -40°C~105°C			
I_{DD}	Operating Current Normal Run Mode HCLK = 60 MHz while(1){} Executed from Flash	-	14.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	5.5V	X	60 MHz	X
I_{DD}		-	14.9	-	mA	3V	X	60 MHz	V
I_{DD}		-	10.3	-	mA	3V	X	60 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	10.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	5.5V	X	48 MHz	X
I_{DD}		-	10.4	-	mA	3V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	3V	X	48 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	5.5V	24 MHz	X	X
I_{DD}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	3V	24 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	5.5V	16 MHz	X	X

I_{DD}		-	3.9	-	mA	3V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	3V	16 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	3.1	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD}		-	2.5	-	mA	5.5V	12 MHz	X	X
I_{DD}		-	3.1	-	mA	3V	12 MHz	X	V
I_{DD}		-	2.4	-	mA	3V	12 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.5	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD}		-	1.3	-	mA	5.5V	4 MHz	X	X
I_{DD}		-	1.4	-	mA	3V	4 MHz	X	V
I_{DD}		-	1.2	-	mA	3V	4 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	184	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD}		-	182	-	µA	5.5V	32 KHz	V	X
I_{DD}		-	164	-	µA	3V	32 KHz	V	V[1]
I_{DD}		-	162	-	µA	3V	32 KHz	V	X
I_{DD}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	178	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD}		-	178	-	µA	5.5V	X	10 KHz	X
I_{DD}		-	158	-	µA	3V	X	10 KHz	V[2]
I_{DD}		-	158	-	µA	3V	X	10 KHz	X
I_{IDLE}	Operating Current Idle Mode HCLK= 60 MHz	-	8.3	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	3.6	-	mA	5.5V	X	V	X

I_{IDLE}		-	8.3	-	mA	3V	X	V	V
I_{IDLE}		-	3.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK= 48 MHz	-	5.7	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	5.7	-	mA	3V	X	V	V
I_{IDLE}		-	2.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK = 24 MHz	-	2.9	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	5.5V	24 MHz	X	X
I_{IDLE}		-	2.9	-	mA	3V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	3V	24 MHz	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 16 MHz	-	2.2	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE}		-	2.1	-	mA	3V	V	X	V
I_{IDLE}		-	1.3	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 12 MHz	-	1.8	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.1	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.7	-	mA	3V	V	X	V
I_{IDLE}		-	1.1	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 4 MHz	-	1.0	-	mA	V_{DD}	EXT_CLK	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	0.8	-	mA	5.5V	V	X	X

I_{IDLE}		-	1.0	-	mA	3V	V	X	V
I_{IDLE}		-	0.7	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 10 kHz	-	147	-	µA	V_{DD}	EXT_CLK	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{IDLE}		-	147	-	µA	5.5V	X	V	X
I_{IDLE}		-	127	-	µA	3V	X	V	V[2]
I_{IDLE}		-	126	-	µA	3V	X	V	X
I_{PWD}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD}		-	0.8	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			
V_{IL1}	Input Low Voltage (TTL Input)	0.8	1.42		V	V_{DD} = 5.5 V			
		0.8	1.08			V_{DD} = 3.3 V			
V_{IH1}	Input High Voltage (TTL Input)		1.42	2.0	V	V_{DD} = 5.5 V			
			1.08	2.0		V_{DD} = 3.3 V			
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-			
R_{UP}[3]	Internal Pull-up Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{LOW}[3]	Internal Pull-low Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.2 V ~ 5.5V			
V_{ILS}	Negative-going Threshold (Schmitt input)	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt input)	$0.7V_{DD}$	-	-	V	-			
I_{IL}	Logic 0 Input Current (Quasi-bidirectional Mode)	-	-63.65		µA	V_{DD} = 5.5 V, V_{IN} = 0V			
I_{TL}	Logic 1 to 0 Transition Current	-	-566.7	-	µA	V_{DD} = 5.5 V			
I_{SR}	Source Current (Quasi-	-	-372	-	µA	V_{DD} = 4.5 V, V_{IN} = 2.4 V			

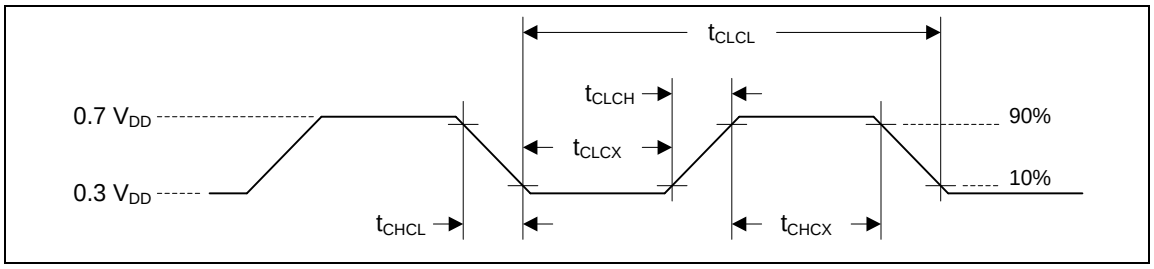
I_{SR}	bidirectional Mode)	-	-76.8	-	µA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-37.3	-	µA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SR}	Source Current (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-2	-	mA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SK}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.2 V, V_{IN} = 0.4 V

Notes:

1. Only enable modules, which support 32 kHz EXT_CLK source
2. Only enable modules, which support 10 kHz LIRC clock source.
3. Guaranteed by design, not test in production.

5.3 NM1244 AC Electrical Characteristics

5.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

5.3.2 External Clock Input (EXT_CLK) (up to 24MHz)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{EXT_CLK}	Operation Voltage	2.2	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
F_{EXT_CLK}	Clock Frequency	-	-	24	MHz	-

5.3.3 48/60 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC60}	Center Frequency	-	60	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD}=4.5 V~ 5.5 V
		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=3.0 V~ 5.5 V
f_{HRC48}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.0	-	+1.0	%	T_A = 25 ℃ V_{DD} = 5.5 V
		-2.5	-	2.5	%	T_A = -40℃~105℃ V_{DD}=2.2 V~ 5.5 V

5.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-5[1]	-	+5[1]	%	V_{DD} = 2.2 V ~ 5.5 V T_A = -40℃ ~ +105℃

Note1: These parameters are characterized but not tested.

5.4 NM1244 Analog Characteristics

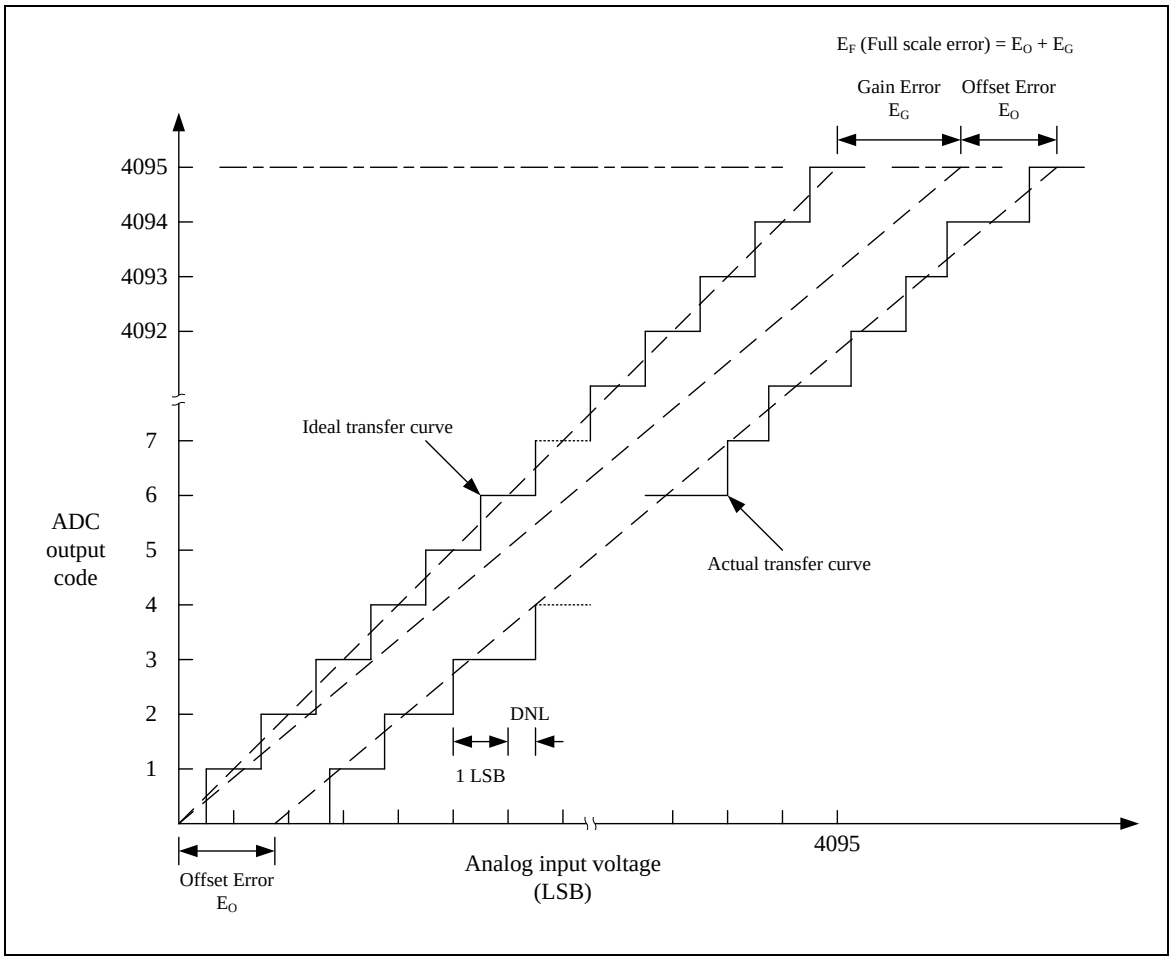
5.4.1 12-bit SAR ADC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		300			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]		800	1000	ns	V_{DD} = 3.0~5.5 V
I_{DDA}	Operation Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	V_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-

Note:

1. ADC voltage reference is same with V_{DD} .
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of C_{IN} is less than about 10% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 800ns at V_{DD} = 5V.


E_F (Full scale error) = E_O + E_G
Gain Error E_G
Offset Error E_O
4095
4094
4093
4092
7
6
5
4
3
2
1
ADC output code
Ideal transfer curve
Actual transfer curve
DNL
1 LSB
4095
Offset Error E_O
Analog input voltage (LSB)

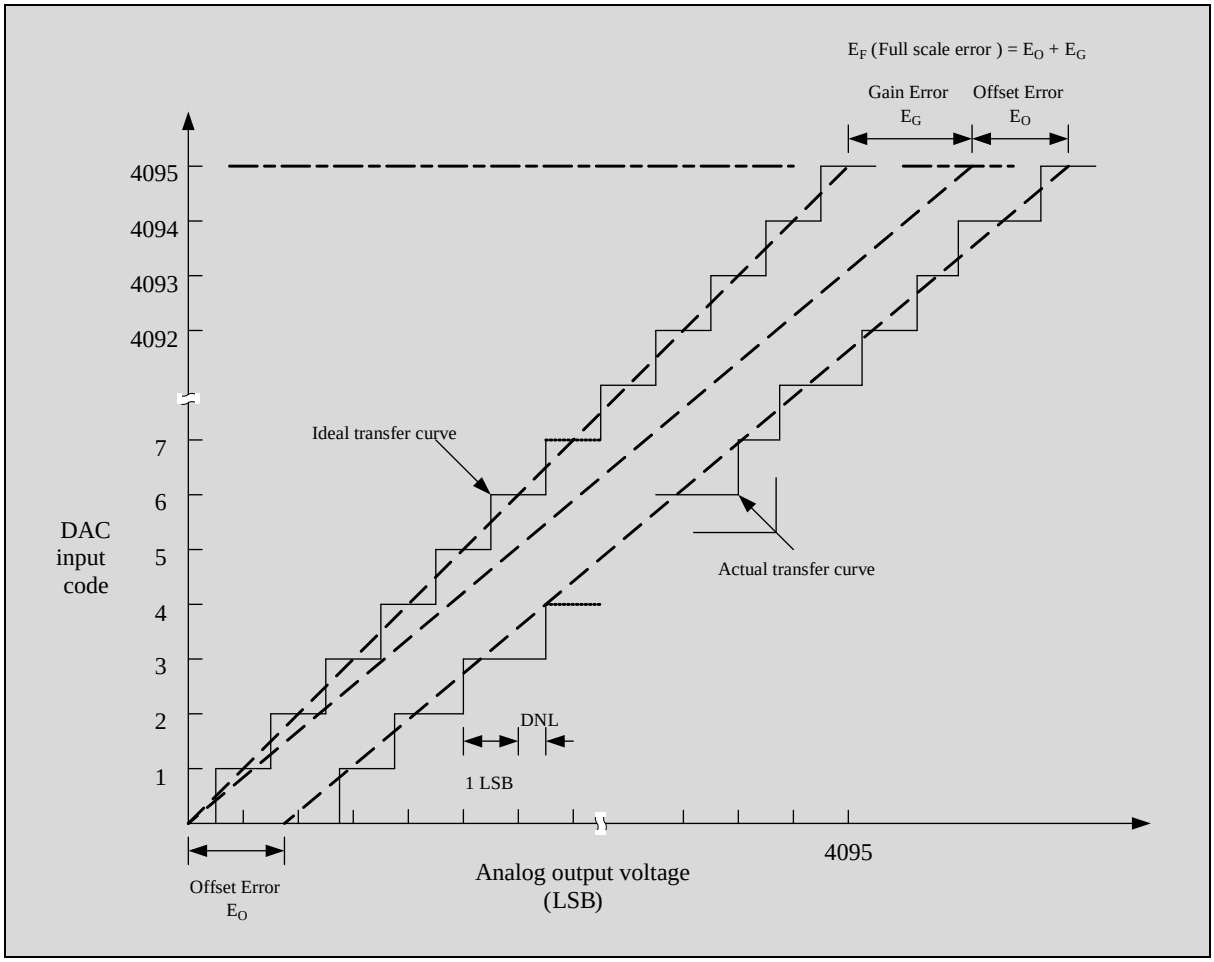
5.4.2 12-bit SAR DAC

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±4	-	LSB	V_{DD} = 5V
INL	Integral Nonlinearity Error	-	±3	-	LSB	V_{DD} = 5V
E_O	Offset Error	-	3	-	LSB	V_{DD} = 5V
E_G	Gain Error (Transfer Gain)	-	3	-	LSB	V_{DD} = 5V
I_{DDA}	Operation Current (Avg.)	-	100	-	uA	V_{DD} = 5V
V_{out}	Analog output Voltage	0	-	V_{DD}	V	-

Note:

1. DAC voltage reference is the same with V_{DD}.



5.4.3 DAC Output buffer

(V_{DD} – V_{SS} = 2.5 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
Slew rate	3.0	-	-	V/us	V_{DD} = 5V, RLOAD = 33K, CLOAD = 50p
Output Current		3		mA	V_{DD} - 0.3 ~ V_{SS} + 0.3, V_{DD} = 3~5V
Power consumption		200		uA	V_{DD} = 5V

5.4.4 LDO & Power Management

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LDO}	Output Voltage	1.35	1.5	1.65	V	-

Notes:

It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

5.4.5 Brown-out Detector

(V_{DD} – V_{SS} = 0 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{BOD}	Brown-out Hysteresis	30	100	150	mV	
V_{BOD}	Brown-out Detector	4.15	4.3	4.45	V	BOV_VL [2:0] = 7
		3.85	4.0	4.15	V	BOV_VL [2:0] = 6
		3.55	3.7	3.85	V	BOV_VL [2:0] = 5
		2.85	3.0	3.15	V	BOV_VL [2:0] = 4
		2.55	2.7	2.85	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

5.4.6 Power-on Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{POR}	Threshold Voltage	1.60	1.75	1.90	V	-
V_{LVRLPM}	Threshold Voltage(Low Power)	1.3	1.6	2.1	V	-

5.4.7 LVR Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LVR}	Threshold Voltage(high→low)	1.7	1.9	2.1	V	-

V_{LVRHYS}	Hysteresis Voltage	-	-	100	mV	

5.4.8 Comparator

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	V_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	
V_{HYS}	Hysteresis	10	20	30	mV	ACMPHYSEN = 01
V_{HYS}	Hysteresis	60	90	120	mV	ACMPHYSEN = 10
V_{HYS}	Hysteresis	95	150	200	mV	ACMPHYSEN = 11
T_{STB}	Stable time	-	1.06	-	μs	

Notes:

Guaranteed by design, not test in production.

5.4.9 OP Amplifier

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
PSRR+	-	90	-	dB	VDD=5V
CMRR	-	90	-	dB	VDD=5V
Slew rate	6.0	-	-	V/us	VDD=5V, RLOAD=33K, CLOAD=50p
Wake up time	-	-	1	us	
Maximum output voltage swing from rail		20		mV	V_{DD} =5.5, RL=10K
		100		mV	V_{DD} =5.5, RL=2K
Open-loop output implement		200		ohm	V_{DD} =5, f=10MHz
Close-loop output implement		95		ohm	V_{DD} =5, f=10MHz

5.4.10 Temperature Sensor

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1],	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	715	-	mV	TA = 0 ℃

Note:

1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

5.4.11 ESD Characteristics

Symbol	Ratings	Condition	Package	Maximum Value	Unit
V_{ESD}	Electrostatic discharge (Human body mode)	TA = + 25 ℃	LQFP 48	TBD	V
	Electrostatic discharge (Machine mode)			TBD	V
	Electrostatic discharge (Charged Device mode)			TBD	V

5.4.12 EFT Characteristics

Symbol	Condition	Package	Pass Level	Unit
	Fsys			
	HIRC	LQFP 48	TBD	V

5.5 NM1244 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	5	6.5	us	Per Byte
I_{DD1}	Read Current	-	4	5.5	mA	@50MHz
I_{DD2}	Program Current	-	-	3.5	mA	
I_{DD3}	Erase Current	-	-	2	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
   Guaranteed by design, not test in production.

5.6 NCT3612 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VCC	Input supply voltage.	-0.3 to 40	V
VB	High-side floating supply absolute voltage.	-0.3 to VS+VR12V	V
VS	High-side floating supply offset voltage.	-2 to VCC+2	V
HO	High-side floating output voltage.	VS-0.3 to VB+0.3	V
LO	Low-side output voltage.	-0.3 to VR12V+0.3	V
Other pins	5VOUT (LDO5V_MCU_CAP), RSTB, HIN, LIN.	-0.3 to 6	V
θ_{JA}	Thermal Resistance,	40	℃/W
θ_{JC}	Thermal Resistance,	10	℃/W
θ_{STG}	Storage Temperature	-50 to 150	℃
θ_{J}	Junction Temperature	150	℃
ESD Rating	Human Body Mode(all pins)	±2	KV
	Charge Device Mode	±500	V
	Latch-up	±100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.7 NCT3612 Recommended Operating Conditions

PARAMETER	RATING	UNIT
Low side and logic fixed supply voltage	8 to 25	V
LDO5V Supply Output Current	20	mA
Operating Temperature	-40 to 105	℃
Junction Temperature	-40 to 125	℃

Note: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

5.8 NCT3612 DC Electrical Characteristics

(VCC= 35V, TA = TJ = 25° C, unless otherwise specified)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Input supply voltage	VCC		8	---	35	V
VCC UVLO turn-on threshold	UVLO+		---	4	---	V
VCC UVLO turn-off threshold	UVLO-		---	3.6	---	V
VCC UVLO threshold hysteresis			---	0.4	---	V
VCC operation current		PWM=20KHz, Duty=50%	---	20	---	mA
VCC sleep mode current		RSTB=Low	---	100		uA
Gate Driver Output						
Souring peak current	I_{O+}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.25	---	A
Sinking peak current	I_{O-}	C_L=0.22uF, PWM=1KHz, Duty=50%	---	0.5	---	A
Turn-on propagation delay	t_{on}	VCC=35，C_L=1nF	---	50	---	nS
Turn-off propagation delay	t_{off}	VCC=35，C_L=1nF	---	50	---	nS
Turn-on rise time	t_r	C_L=1nF	---	50	---	nS
Turn-off fall time	t_f	C_L=1nF	---	30	---	nS
PWM delay matching	MT		---	50	---	nS
Pull low resistance	R_o		---	100	---	KΩ
Logic Input						
Voltage high Level	VIH		2.4	---	---	V
Voltage low Level	VIL		---	---	0.8	V
HIN/LIN pull low Resistance			---	100	---	KΩ
Internal 5V/12V regulator						
5V output voltage	$5V_{OUT}$		4.75	5	5.25	V
5V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
12V output voltage	V_{R12V}		---	12	---	V
12V output current Limit		VCC=35，TA = 25° C	---	---	30	mA
Bootstrapped Power Supply Section						
VS_U/V/W leakage current		VB_U/V/W=VS_U/V/W=40V	---	---	50	uA

Bootstrap diode ON resistance	R_{BD}		---	150	---	Ω
Thermal Protection						
Thermal shutdown temperature	TSD		---	165	---	℃
Thermal shutdown hysteresis	TSDHYS		---	50	---	℃

5.9 NCT3612 DC Electrical Characteristics

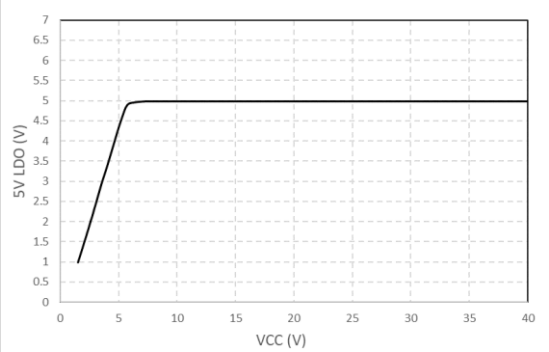


Figure 5.9-1 VCC vs. 5V LDO Voltage

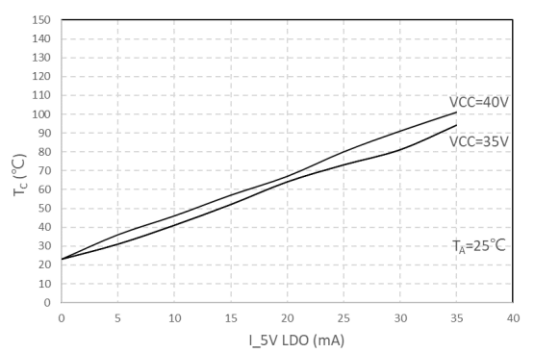


Figure 5.9-2 5V LDO Current vs. IC temperature

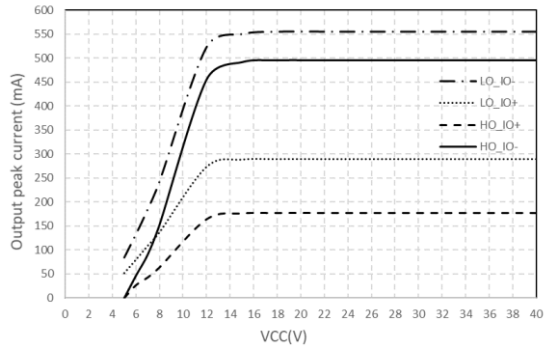


Figure 5.9-3 VCC vs. Output peak current

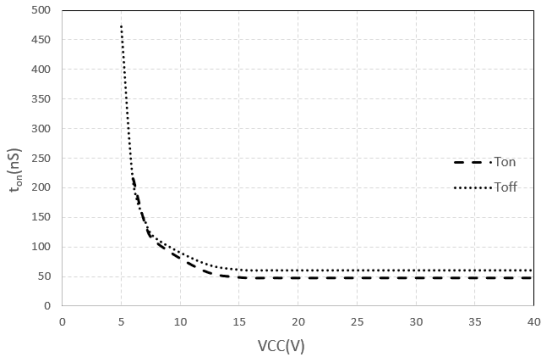


Figure 5.9-4 VCC vs. Ton/Toff propagation delay

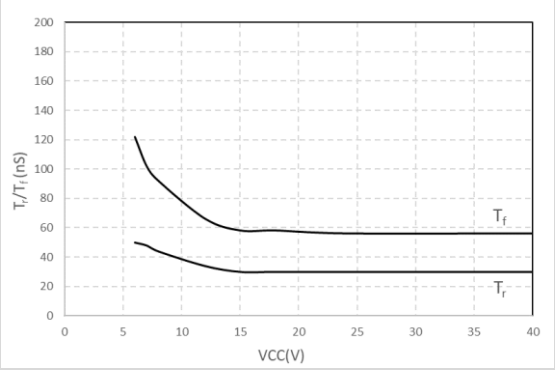
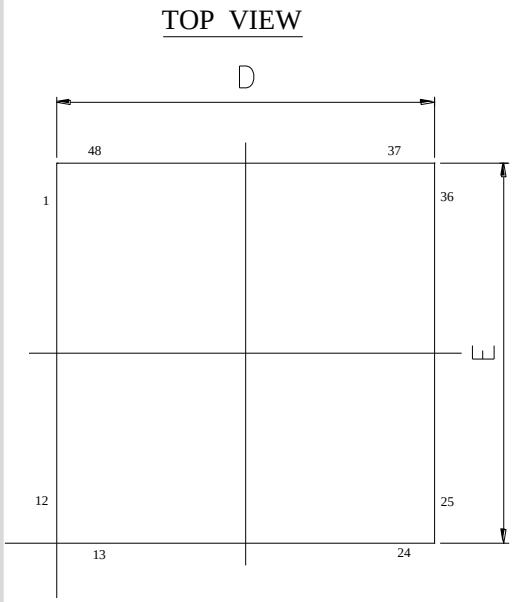
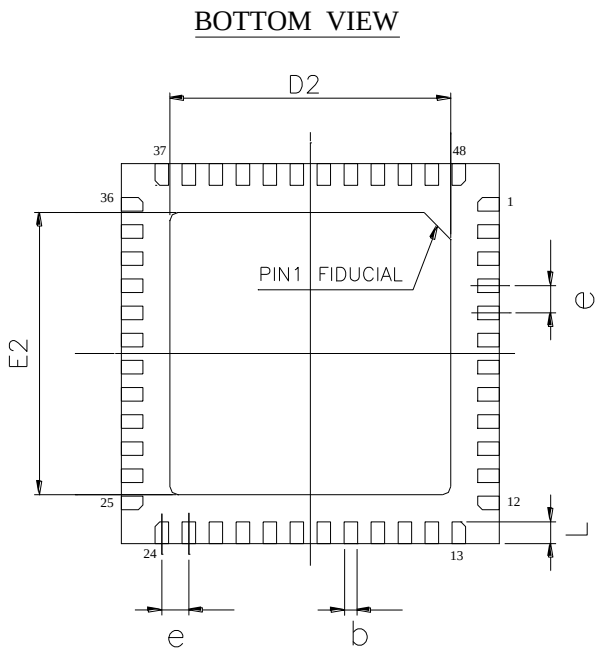


Figure 5.9-5 VCC vs. Turn-on/off rise time

6 PACKAGE DIMENSIONS

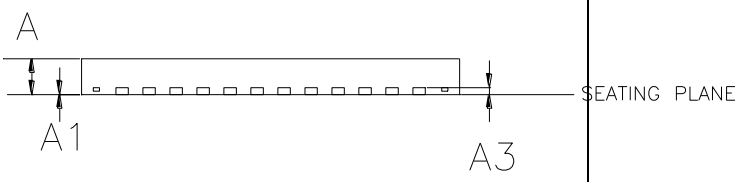
6.1 48-pin QFN (7mm x 7mm)





Controlling Dimension :Millimeters

SYMBOL	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.61	0.66	0.70	0.024	0.026	0.028
A1	0	0.02	0.05	0	0.001	0.002
A3		0.127 REF			0.005 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		7.00 BSC			0.276 BSC	
D2	2.25	4.70	5.25	0.089	0.185	0.207
E		7.00 BSC			0.276 BSC	
E2	2.25	4.70	5.25	0.089	0.185	0.207
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
y		0.08			0.003	



*D2,*E2 :By die size difference

7 ORDERING INFORMATION

Part Number	Supplied As	Package Type	Operating Temperature
NM18407Y	4000 units/ T&R	QFN48, Green Package	Commercial, -40℃~105℃

8 REVISION HISTORY

Revision	Date	Description
0.01	March 23, 2021	1. Preliminary version 0.01

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