ISD ChipCorder®
ISD15D00 Series
Design Guide

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The ISD15D00 is a digital ChipCorder® featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The ISD15D00 utilizes serial flash memory to provide non-volatile audio playback for a two-chip solution. The ISD15D00 provides an I²S digital audio interface, faster digital programming, higher sampling frequency, and a signal path with SNR 80dB.

The ISD15D00 can take digital audio data via I²S or SPI interface. When I²S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD15D00 supported sample rates.

The ISD15D00 has inbuilt analog audio inputs, analog audio line driver, and speaker driver output.

The analog audio input, Aux-in, has a fixed gain configured by SPI command. Aux-in can directly feed-through to the analog outputs; it can also mix with the DAC output and then feed-through to the analog outputs.

The ISD15D00 can deliver three kinds output: 1) Aux-out, an analog single-ended voltage output; 2) Class-AB BTL (bridge-tied-load) analog differential voltage output; 3) Class-D PWM. Both Class-AB BTL and Class-D PWM output can directly drive a speaker.

2 FEATURES

- External Memory:
  - The ISD15D00 supports the following flash:

Manufacturer	Winbond		Numonyx			MXIC
Family	25X	25Q	25P	25PX	25PE	25L / 25V
JEDEC ID	EF 30 1X	EF 40 1X	20 20 1X	20 71 1X	20 80 1X	C2 20 1X

  - The addressing ability of ISD15D00 is up to 128Mbit, which is 64-minute playback time based on 8kHz/4bit ADPCM.
  - Inbuilt 3V voltage regulator to provide power source to the external flash memory
- Fast Digital Programming
  - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Memory Management
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index-based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences.
- Sample Rate
  - Seven sampling frequencies are available for a given master sample rate. For example, the sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate.
  - For I²S operation, 32, 44.1 and 48kHz master sample rates are available with playback sampling frequencies scaling accordingly.
- Compression Algorithm
  - For Pre-Recorded Voice Prompts
    - µ-Law: 6, 7 or 8 bits per sample
    - Differential µ-Law: 6, 7 or 8 bits per sample
    - PCM: 8, 10 or 12 bits per sample
    - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
    - Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
  - Internal oscillator with internal reference: 2.048 MHz with ±1% deviation

  - Internal oscillator with external resistor: 2.048 MHz with ±2% deviation[1]
  - I^2S bit clock input
- Input
  - Aux-in: Analog input with 2-bit gain control configured by SPI command
- Output
  - Aux-out: an analog single-ended voltage output
  - Class-D PWM speaker driver, capable of delivering typical power:
    - 4Ω load: 1W @5.5V; 335mW @3.3V.
    - 8Ω load: 930mW @5.5V; 320mW @ 3.3V.
  - Class-AB BTL analog differential output, capable of delivering typical power:
    - 4Ω load: 950mW @5.5V; 330mW @3.3V.
    - 8Ω load: 930mW @5.5V; 320mW @ 3.3V.
- I/O
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - I^2S interface: I^2S_CLK, I^2S_WS, I^2S_SDI, I^2S_SDO for digital audio data
  - 8 GPIO pins:
    - 4 GPIO pins share with I^2S
    - 4 GPIO pins share with SPI Interface
    - GPIO pins can trigger Voice Macro for a pushbutton application
- 8-bit Volume Control set by SPI command for flexible mixing
- Talarm temperature threshold: 125°C typical
- Operating Voltage: 2.7 ~ 5.5V
- Standby Current: 1uA typical
- Package:
  - Green 32L-QFN
- Temperature Options:
  - Industrial: -40°C to 85°C

[1] With ±1% precision 80kohm external resistor.

3 BLOCK DIAGRAM

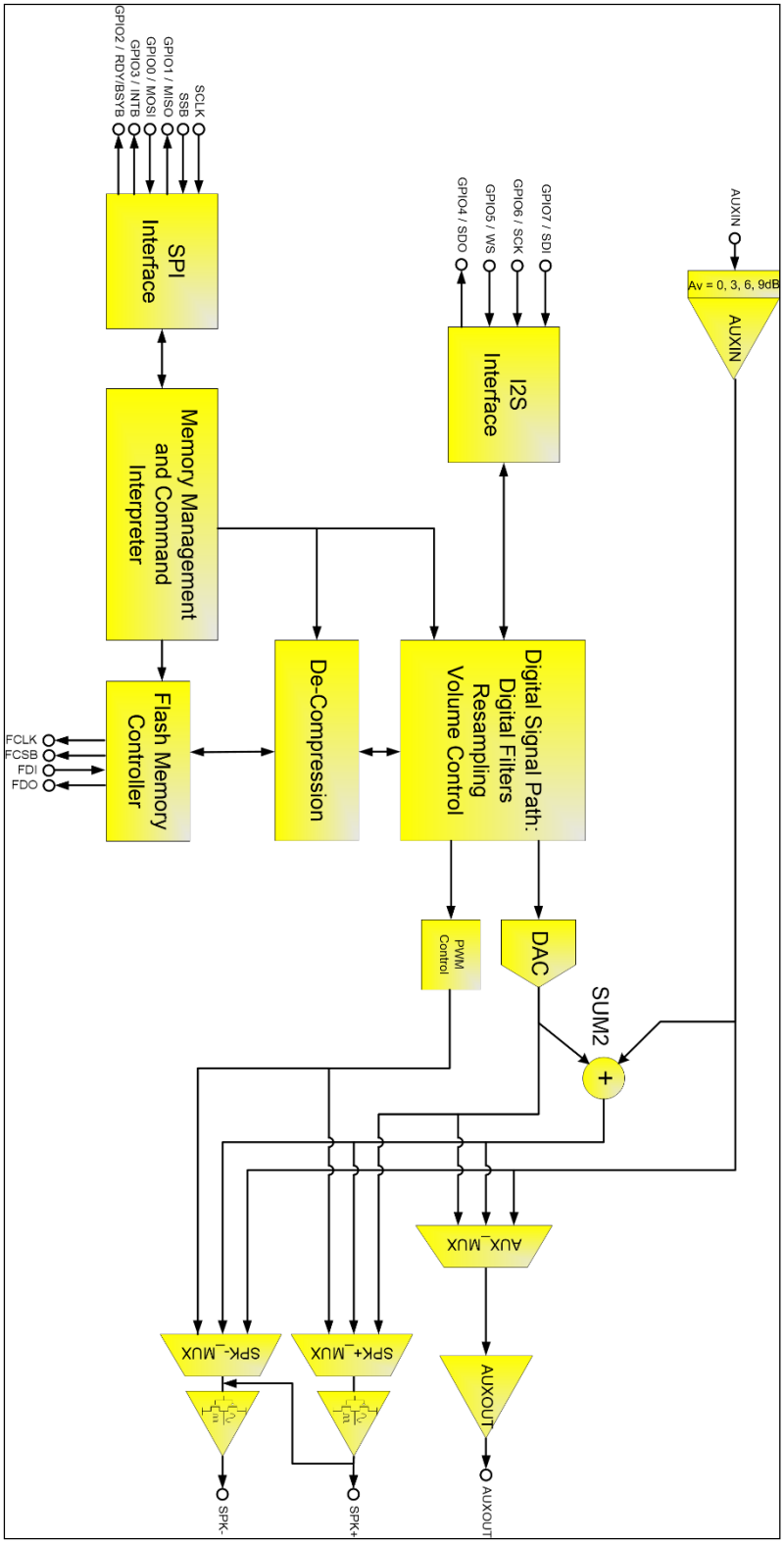


Figure 3-1 ISD15D00 Block Diagram

4 PINOUT CONFIGURATION

4.1 32L-QFN

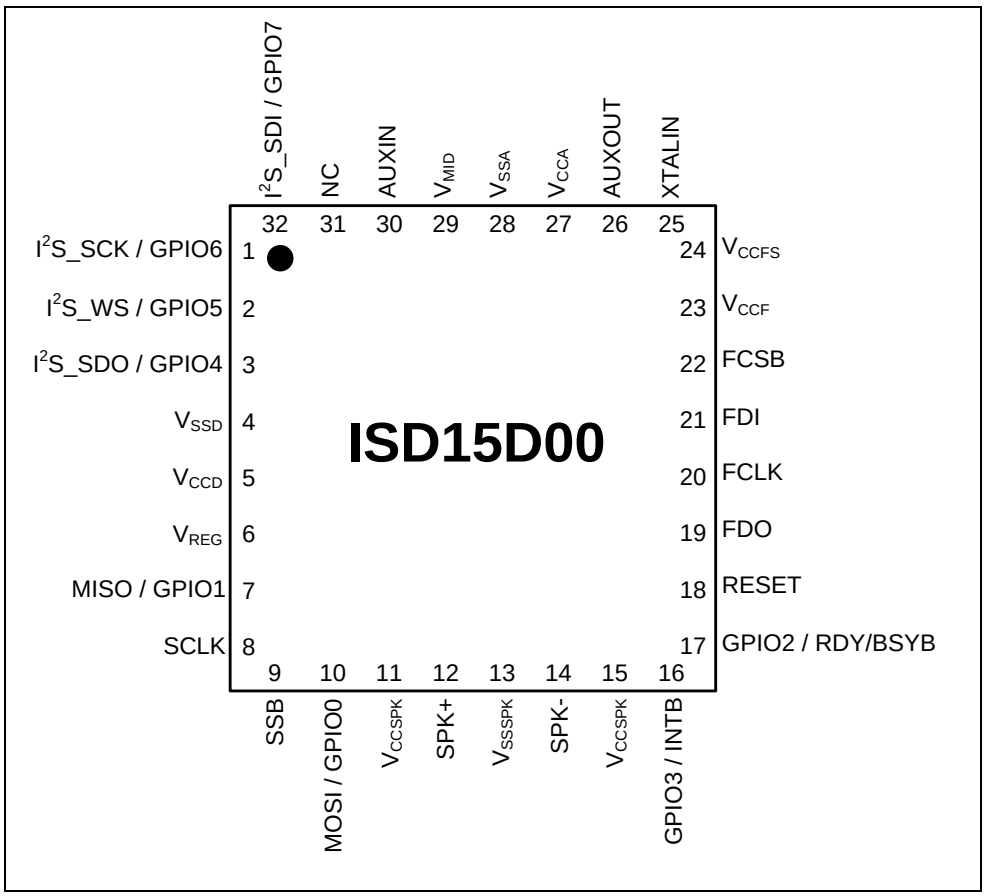


Figure 4-1 ISD15D00 32-Lead QFN Pin Configuration

5 PIN DESCRIPTION

Pin Name	I/O		Function
QFN-32			
1	GPIO6 / I^2S_SCK	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I^2S is not used.
2	GPIO5 / I^2S_WS	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Word Select (WS) input in slave mode or WS output in master mode.
3	GPIO4 / I^2S_SDO	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Output of the I^2S Interface.
4	V_{SSD}	I	Digital Ground.
5	V_{CCD}	I	Digital power supply.
6	V_{REG}	O	A 1.8V regulator to supply the internal logic. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability.
7	GPIO1 / MISO	O	Master-In-Slave-Out. Serial output from the ISD15D00 to the host. This pin is in tri-state when SSB=1. Can be configured as GPIO1.
8	SCLK	I	Serial Clock input to the ISD15D00 from the host.
9	SSB	I	Slave Select input to the ISD15D00 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
10	GPIO0 / MOSI	I	Master-Out-Slave-In. Serial input to the ISD15D00 from the host. Can be configured as GPIO0.
11	V_{CCSPK}	I	Power supply for speaker driver.
12	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive a speaker. During power down this pin is in tri-state. Or, can be configured as Class-AB BTL which, together with SPK- pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
13	V_{SSSPK}	I	In PWM mode: Digital Ground for the PWM Driver. Or, In Class-AB mode: Analog Ground for the Class-AB output.
14	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive a speaker. During power down this pin is tri-state. Or, can be configured as Class-AB BTL which, together with SPK+ pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
15	V_{CCSPK}	I	Power supply for speaker driver.

Pin Name	I/O		Function
QFN-32			
16	GPIO3 / INTB	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as GPIO3.
17	GPIO2 / RDY/ BSYB	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD15D00 is ready to accept new SPI commands or data. Can be configured as GPIO2.
18	RESET	I	Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)
19	FDO	O	Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash.
20	FCLK	O	Serial data CLK of the external serial flash interface.
21	FDI	I	Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory.
22	FCSB	O	Chip Select Bar of the external serial flash interface.
23	V_{CCF}	O	Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
24	V_{CCFS}	I	Digital power supply for the inbuilt voltage regulator for the external flash memory. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
	XTALOUT	O	Crystal interface output pin.
25	XTALIN	I	The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected.
26	AUXOUT	O	Aux Output. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected.
27	V_{CCA}	I	Analog power supply pin.
28	V_{SSA}	I	Analog ground pin.
29	V_{MID}	O	Middle voltage reference for the swing of analog/digital audio outputs. A 4.7uF capacitor should be connected to this pin for supply decoupling and stability.
30	AUXIN	I	Auxiliary input with the gain set by SPI command If Aux-in is not used, this pin should be left unconnected.
31	NC		This pin should be left unconnected.
32	GPIO7 / I^2S_SDI	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Input of the I^2S interface.

*note: for QFN-32 package center pad underneath should be connected to VSSA. Please avoid placing exposed via under this pad.

6 SPI INTERFACE

This is a standard four-wire interface used for communication between ISD15D00 and the host. It consists of an active low slave-select (SSB), a serial clock (SCLK), a data input (Master Out Slave In - MOSI), and a data output (Master In Slave Out - MISO). In addition, for some transactions requiring data flow control, a RDY/BSYB signal (pin) is available.

The ISD15D00 supports SPI mode 3: (1) SCLK must be high when SPI bus is inactive, and (2) data is sampled at SCLK rising edge. A SPI transaction begins on the falling edge of SSB and its waveform is illustrated below:

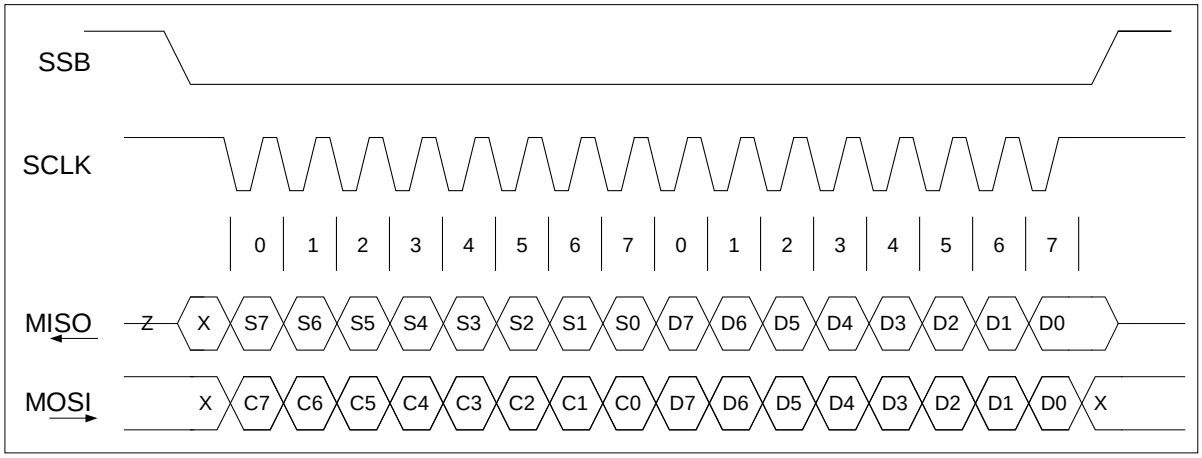


Figure 6-1 SPI Data Transaction.

A transaction begins with sending a command byte (C7-C0) with the most significant bit (MSB – C7) sent in first. During the byte transmission, the status (S7-S0) of the device is sent out via the MISO pin. After the byte transmission, depending upon the command sent, one or more bytes of data will be sent via the MISO pin.

RDY/BSYB pin is used to handshake data into or out of the device. Upon completion of a byte transmission, RDY/BSYB pin could change its state after the rising edge of the SCLK if the built-in 32-byte data buffer is either full or empty. At this point, SCLK must remain high until RDY/BSYB pin returns to high, indicating that the ISD15D00 is ready for the next data transmission. See below for timing diagram.

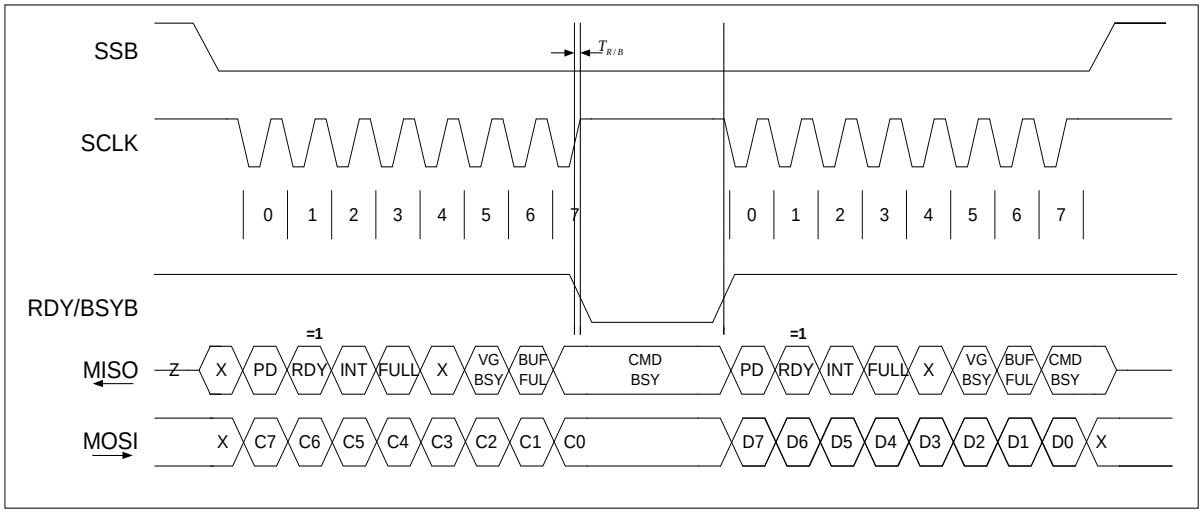


Figure 6-2 RDY/BSYB Timing for SPI Writing Transactions.

If the SCLK does not remain high, RDY bit of the status register will be set to zero and be reported via the MISO pin so the host can take the necessary actions (i.e., terminate SPI transmission and re-transmit the data when the RDY/BSYB pin returns to high).

For commands (i.e., DIG_READ, SPI_PCM_READ) that read data from ISD15D00, MISO is used to read the data; therefore, the host must monitor the status via the RDY/BSYB pin and take the necessary actions.

The INT pin will go low to indicate (1) data overrun/overflow when sending data to the ISD15D00; or (2) invalid data from ISD15D00. See Figure 6-3 for the timing diagram.

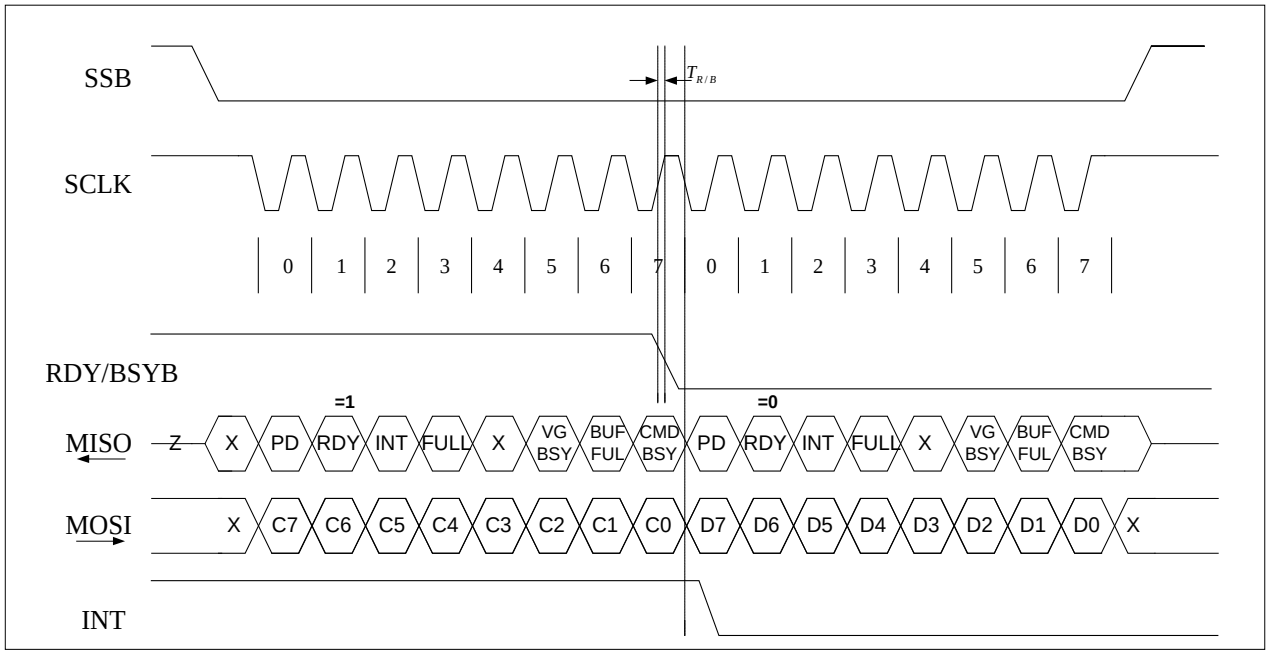


Figure 6-3 SPI Transaction Ignoring RDY/BSYB

7 ANALOG AND DIGITAL SIGNAL PATH

7.1 Analog Signal Path

Analog signal path provides a configurable Aux-in analog input and two analog outputs along with multiplexing and summation blocks to route signals between analog blocks and the digital signal path.

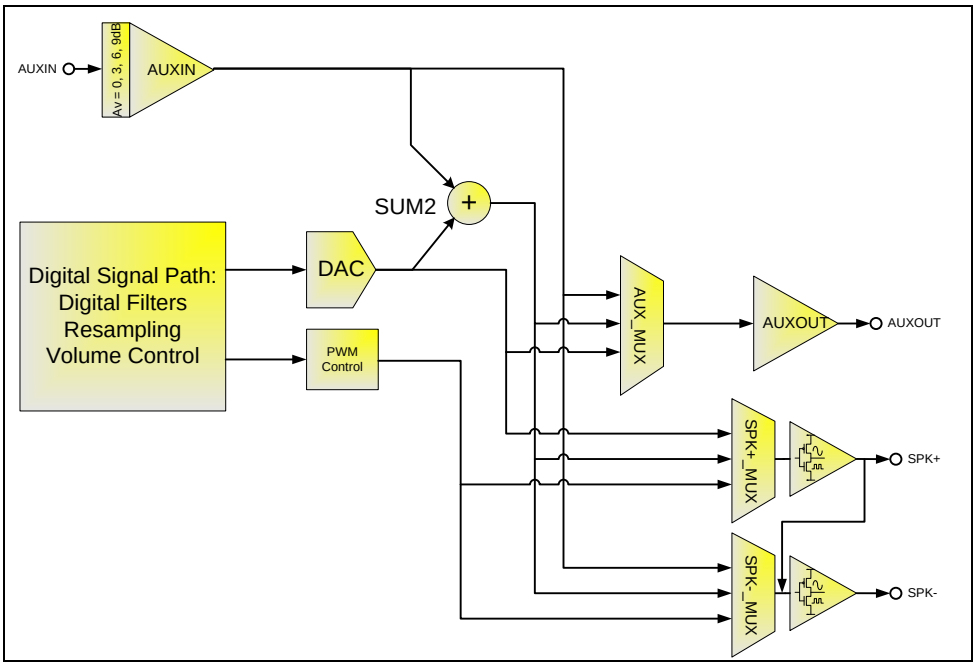


Figure 7-1 Analog Signal Path

Analog outputs consist of:

- AUXOUT is a single-ended voltage output.
- Class-AB BTL (bridge-tied-load) is a differential voltage output, which shares the same two pins of PWM (SPK+/SPK-). Signal source of Class-AB BTL could be either from DAC or SUM2.
    - Besides Class-AB BTL, SPK+ and/or SPK- can also be individually configured as a single-ended Class-AB output.

The analog path consists of the following blocks: AUXIN, SUM2, AUX_MUX, SPK+_MUX, and SPK-_MUX. The summation block SUM2 is able to mix two signals together. SUM2 mixes the analog input AUXIN with the digital signal path output. AUX_MUX provides input selection into the AUXOUT block. SPK+_MUX and SPK-_MUX provide input selection into the SPK+ and SPK- blocks. The configuration registers, CFG5-CFG9 & CFG18, control the active path features, allow individual power control of each block and enable the muting of certain path inputs. The details of the path configuration registers are described in Section 12.3.

7.2 AUX ANALOG INPUT

The AUX Analog Input amplifies input signals with a fixed gain of 0dB, 3dB, 6dB, or 9dB, selectable via SPI command. Similar to ANAIN, the gain setting should be configured so that the output signal has a 1Vpp swing.

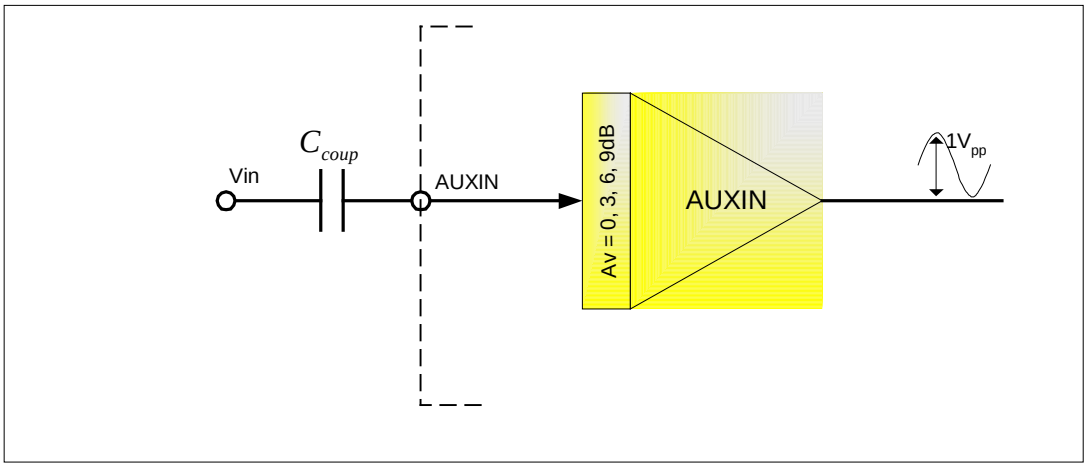


Figure 7-2 AUXIN Input Amplifier

The coupling capacitor, C_{coup}, like in the case of ANAIN, should be set according to the value of R_{in} to allow signals above a certain frequency to pass through. The relationship repeated here is:

$$f_{pass} = \frac{1}{2\pi R_{in} C_{coup}}$$

R_{in} is the input impedance of the AUXIN amplifier and is dependent upon the gain setting as shown in Table 7-1 below.

Table 7-1 Gain Setting Vs. Rin

Setting	Gain dB	Gain	Rin (kOhms)
00	0	1.00	40.0
01	3	1.41	33.2
10	6	2.00	26.7
11	9	2.82	21.0

The minimum value of R_{in} is approximately 20kOhms, so a C_{coup} of 1µF will allow audio signals to pass through under all possible gain settings.

7.2.1 AUX & Class-AB BTL Analog Output

AUXOUT is a single-ended voltage output. It needs an external amplifier to drive the speaker. AUXOUT together with the external amplifier is usually used when loud volume is needed.

Class-AB BTL (bridge-tied-load) is a differential voltage output, which shares the same two pins of PWM (SPK+ and SPK-). As a differential output, Class-AB BTL is naturally better than AUXOUT in terms of noise rejection.

Class-AB BTL can directly drive a speaker or drive a speaker via an external amplifier. Below is a table comparing the Class-AB BTL and AUXOUT:

	Class-AB BTL	AUXOUT	PWM
Driving Method	Direct drive. Or, drive with an external amplifier.	Need an external amplifier.	Direct drive.
Driving Ability	1 W at V_{CCSPK} = 5V.	High: depends on the external amplifier.	1 W at V_{CCSPK} = 5V.
Quality	Typical 80dB with good noise rejection.	Typical 80dB.	Typical 60dB
Cost	No extra cost.	Extra cost of the external amplifier.	No extra cost.

Table 7-2 Comparison of Class-AB BTL, AUXOUT, and PWM

Signal source of Class-AB BTL could be either from DAC or SUM2. Figure 7-3 (the red line) shows an example of Class-AB BTL setting from the DAC.

Besides Class-AB BTL, SPK+ and/or SPK- can also be individually configured as a single-ended Class-AB output. For detailed settings, please refer to 12.3 Device Configuration Registers, CFG18.

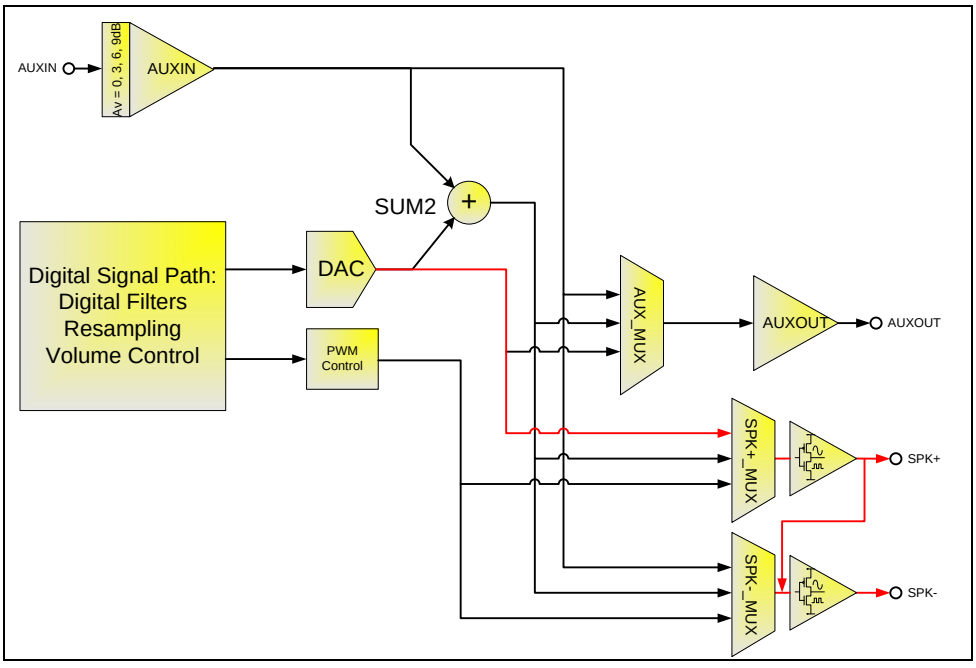


Figure 7-3 DAC to Class-AB BTL

7.3 DIGITAL SIGNAL PATH

The digital signal path performs filtering, sample rate conversion, mixing, volume control and decompression. A block diagram of the digital signal path is shown in Figure 7-4.

The digital signal path operates at a master sample rate Fs (nominally 32kHz) set by the master clock source (see Section 10). It has the ability to up-sample or down-sample to a lower sample-rate, Fsub for playback and audio transfer to/from the SPI interface. Audio input at Fs into the signal path comes from the I²S digital audio interface. Audio at Fsub is up-sampled and can be mixed with the input and level adjusted via VOLA, VOLB and VOLC before going out on the DAC, I²S or PWM driver paths. The FIFO synchronizes audio sources at the sub-sampled bandwidth. One input and one output can be active at a time. The possible combinations are:

DECOMPRESSOR → SPI_OUT (SPI Playback)
DECOMPRESSOR → UPSAMPLE (Playback)

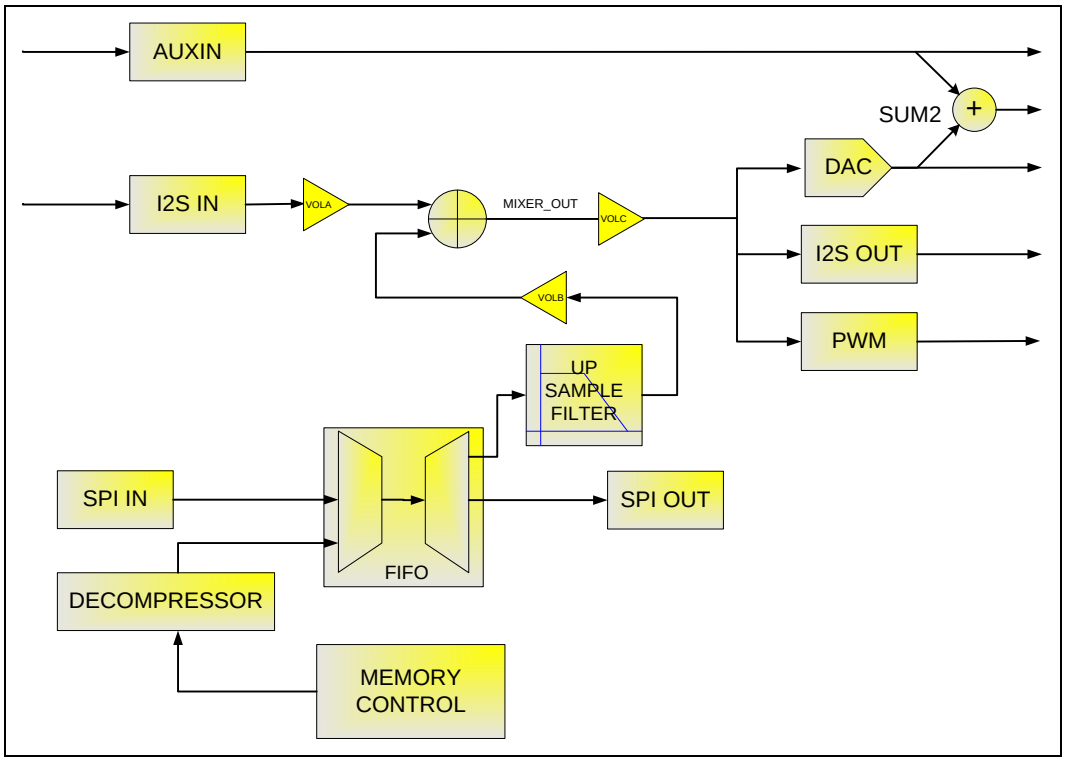


Figure 7-4 Digital Signal Path

8 ISD15D00 MEMORY MANAGEMENT

The ISD15D00 employs several memory management techniques to make audio playback transparent to the host controller. The address space of the ISD15D00 starts at address zero of the external serial flash memory. The external memory size can go up to 128Mbit with an erasable sector size of 4kBytes. The following sections will describe the ISD15D00 memory management architecture and the message management functions.

8.1 MESSAGE MANAGEMENT

The message management schemes implemented on the ISD15D00 are:

1. Voice Prompts: A collection of pre-recorded audio that can be played back using the PLAY_VP SPI command or Voice Macros.
2. Voice Macros: A powerful voice script allowing users to create custom macros to play Voice Prompts, insert silence and configure the device. Voice Macros are executed with a single SPI command.
3. User Data: Memory sectors defined and allocated by the users for use in other applications

8.1.1 Voice Prompts

Voice prompts are pre-recorded audio of any length, from short words, phrases or sound effects to long passages of music. These Voice Prompts can be played back in any order as determined by the users and applications. A Voice Prompt consists of two components:

1. An index pointing to the pre-recorded audio
2. Pre-recorded audio

To play a Voice Prompt, the ISD15D00 use the index of the Voice Prompt to locate and play the pre-recorded audio. This approach allows users to easily manage the pre-recorded audio without the need to update the code on the host controller. In addition, the users can store a multitude of pre-recorded audio without the overhead of maintaining a complicated lookup table. To assist customers in creating the Voice Prompts, a software tool, the ISD15D00 Voice Prompt Editor and writer are available for development purposes.

8.1.2 Voice Macros

Voice Macros are a powerful voice script that allows users to customize their own play patterns such as play Voice Prompts, insert silence, change the master sample clock, power-down the device and configure the signal path, including gain and volume control. Voice Macros are executed using a single SPI command and are accessed using the same index structure as Voice Prompts. This means that a Voice Macro (or Voice Prompt) can be updated on the ISD15D00 without the need to update code on the host micro-controller since absolute addresses are not needed.

The following locations have been reserved for three special Voice Macros:

- Index 0: Power-On Initialization (POI)
- Index 1: Power-Up (PU)
- Index 2: GPIO-Wakeup (WAKEUP)

These Voice Macros allow the users to customize the ISD15D00 power-on and power-up procedures and are executed automatically when utilized. The built-in voice macros will be used when they are not utilized. Please see Section 11 for details.

Here is an example to illustrate the usage of the PU Voice Macro.

- SET_CLK_CFG(0x34)

- WR_CFG_REG(0x02,0x48)
- WR_CFG_REG(0x05,0x80)
- WR_CFG_REG(0x18,0xAB)
- FINISH

The above PU Voice Macro will perform the following:

- Choose internal reference as the clock source
- Set up a playback path from Memory to Class-AB BTL

The following is the complete list of the commands for Voice Macro:

- SET_CLK_CFG(n) – Set clock configuration register to n.
- WR_CFG_REG(reg,n) – Set configuration register reg to value n.
- PWR_DN – Power down the ISD15D00.
- PLAY_VP(i) – Play Voice Prompt index i.
- PLAY_VP@Rn – Indirect Play Voice Prompt.
- PLAY_VP_LP(i) – Loop Play Voice Prompt index i.
- PLAY_VP_LP@Rn – Indirect Loop Play Voice Prompt.
- EXE_VM(i) – Execute Voice Macro index i.
- EXE_VM@Rn – Indirect Execute Voice Macro.
- PLAY_SIL(n) – Play silence for n units. A unit is 32ms at master sampling rate of 32 kHz.
- WAIT_INT – Wait until current play command finishes before executing next macro instruction.
- FINISH – Finish the voice macro and exit.

8.1.3 User Data

User Data consist of 4kByte chunks of erasable sectors defined and allocated by the users for use in other applications. The users have the freedom not to allocate or reserve any memory sectors. A software tool, the ISD15D00 Voice Prompt Editor is available to assist customers in allocating such memory.

8.2 MEMORY HEADER

The Memory headers are located at the initial bytes of the 4kByte memory sector used to determine the format or function of the memory. The Memory Header stores users' configurable information including the memory protection scheme, the PMP pointer and the index table including POI, PU and other Voice Macros defined by the users.

Table 8-1Memory Header

Initial Bytes of the Memory Header						
Byte0	**Byte1-2**	**Byte3-4**	**Bytes5-10**	**Bytes11-16**	**Byte17-22**	**Byte23-28**
0xCX	-	PMP[15:0]	POI_VM	PU_VM	VM/VP[2]	VM/VP[3]

The Memory Header contains at least seventeen bytes located at the beginning of the memory space. Byte0 determines the memory protection scheme. Byte3-4 stores the PMP pointer. After the PMP, it is the start of the Voice Prompt/Voice Macro index table defined by the users. This table consists of six byte entries that are the start and end address of Voice Prompt or Voice Macro. Byte5-10 & Byte11-15 are reserved for the POI and PU Voice Macro which are the first two entries in this table (index 0 and index 1) to be executed on power-on initialization and power-up, respectively. If this function is not desired, these entries should be left erased (0xFFFFFF,0xFFFFFF). When a PLAY_VP(i) or EXE_VM(i) command is sent to the ISD15D00, it reads the index table entry at address 6i+5 and executes the VP or VM at the address present in the table.

The PMP points to the boundary of protected memory and is used in conjunction with the RP, WP and CEP bits to set memory protection indicated below (also see Section 8.5 for details).

Table 8-2 The first byte of the Memory Header

Memory Header Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	0	1	RP	WP	CEP

8.3 DIGITAL ACCESS OF MEMORY

ISD15D00 memory can be accessed as conventional digital memory using the DIG_READ and DIG_WRTIE SPI commands. This allows the user to:

- Reserve areas of memory for use as digital non-volatile memory as User Data
- Update Voice Prompts and macros (pre-recorded audio) in system.
- Read and verify Voice Prompt memory.
- Read sector headers of memory to determine memory usage.

The digital read and write commands can be issued even while an audio playback is in progress. The RDY/BSYB pin governs the flow control for all digital operations.

8.4 DEVICE ERASE COMMANDS

ISD15D00 provides several ways to erase the flash memory. The flash memory has a minimum erasable sector size of 4kBytes. The sector erase command is sent with a start and stop sector address. The ISD15D00 also has commands to mass erase the memory.

8.5 MEMORY CONTENTS PROTECTION

Under certain circumstances, it is desirable for the users to protect portions of the internal memory from write/erase or interrogation (read). The ISD15D00 provides a method to achieve this by setting a protection memory pointer (PMP) that allows the users to protect internal memory for an address range from the beginning of memory to this sector where PMP is pointed. The type of protection is set by three bits in the memory header byte.

- The **CEP** (Chip Erase Protect) bit set to zero enables chip erase protection. This prevents a mass erase function, allowing the device to be configured as a write-once part. With the **CEP** bit set to one, even with write protection enabled, the part can be mass erased. After mass erasure, the initial sector byte defaults to no protection so the device can be re-programmed.
- The **WP** (Write Protect) bit set to zero enables write protection of the internal memory below the sector pointed to by the PMP. Write protection means that digital write or erase commands will not function in this memory area. This can be used to ensure that audio or data is not inadvertently erased or overwritten.
- The **RP** (Read Protect) bit set to zero enables read protection of the internal memory below the sector pointed to by the PMP. Read protection means that digital read or audio playback commands through SPI or I^2S will not function in this memory area. This can be used to ensure that internal memory contents cannot be digitally copied or read.

Memory protection is activated on power-up of the chip. Therefore, each time the user changes the setting of memory protection, the new setting will not be effective until the chip is reset.

9 I2S INTERFACE

The I²S interface is a digital audio interface that allows the transfer of the audio data between other digital audio devices such as multimedia processors, audio amplifiers or DSPs. The ISD15D00 acts as either a master or a slave device on an I²S bus. As a slave the ISD15D00 accepts SCK and WS clock and frame signals from a bus master. In master mode the ISD15D00 generates SCK and WS. It is capable of both data input and output depending upon configuration. The ISD15D00 is configurable to accept data from either the left or right audio channel or a mono mix of both. It can output data to either the left, right or both channels. It is also capable of feeding through a stereo signal and mixing a playback operation into the signal. In slave mode, to synchronize data transfer, the ISD15D00 must derive its master clock from the I²S SCK or be operating from a synchronous external clock source.

I²S is for high bandwidth audio input/output. High bandwidth audio input comes either from the ADC path or the I²S. High bandwidth audio output goes out on the DAC, I²S or PWM driver paths. It all depends on how you configure the path. However, commanding the ISD15D00 is through SPI commands. For instance, the user could configure the path, through the SPI commands, as: "I²S input -> ADPCM-4bit Compression -> Memory Control", then the user can feed the audio data from I²S.

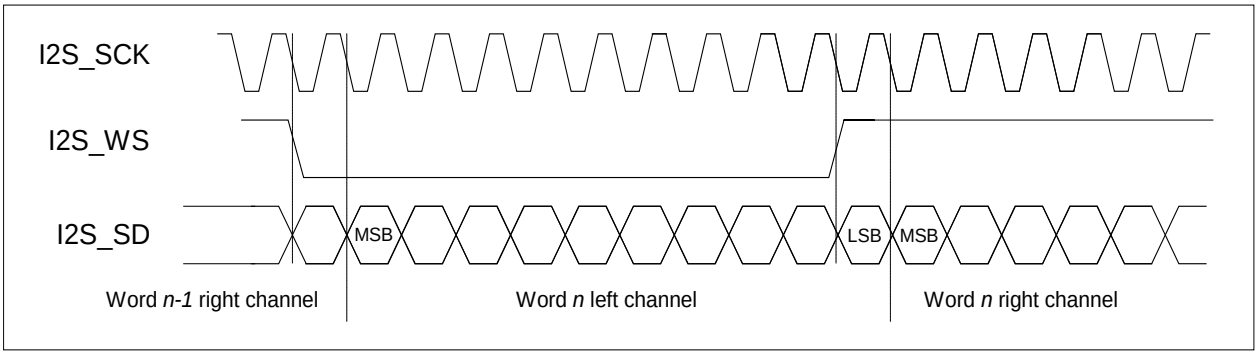


Figure 9-1 I²S Protocol

10 CLOCK GENERATION

The ISD15D00 can derive its master clock from five sources:

1. An internal oscillator controlled by an external resistor (attached to pin XTALIN and GND).
2. An internal oscillator with internal reference.
3. The SCK clock of the I²S interface.

Regardless of source, the selected clock is fed to a phase-locked loop (PLL) to generate the internal master clock (MCLK) of the ISD15D00.

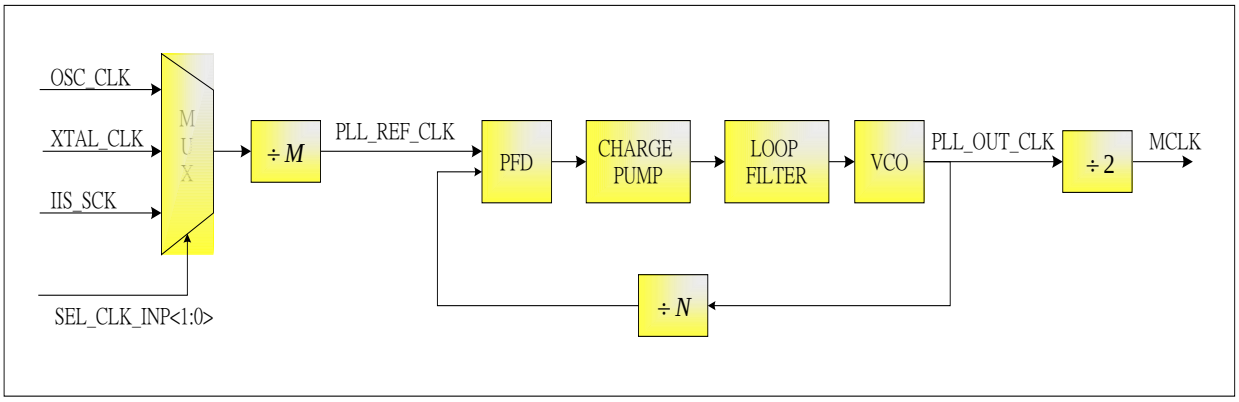


Figure 10-1 PLL Clock Generation on ISD15D00

The goal of clock generation is to generate a master clock rate (MCLK) at 512x the master sample rate (Fs). A table of supported master clock and sample rates is shown below. The master sample frequency can be expressed by the formula:

$$F_{MCLK} = F_{OSC}\frac{N}{2M} \text{ where } M = \{1,2,3\} \text{ and } N = \{8,16,32\}$$

$$F_s = F_{MCLK}\frac{1}{512}$$

Table 10-1 Master Clock and Sample Rates

MCLK (MHz)	Fs (kHz)
16.384	32
24.576	48
22.5792	44.1

For the above master sample rates Fs, playback is available at fixed ratios of the master sample rate.

Table 10-2 Sub-Sample Rates available.

Sub-Sampled ratio	Master Sample Rate Fs (kHz)			Available Sample Rates (kHz)
	32	44.1	48	
8	4	5.5125	6	
6	5.333	7.35	8	
5	6.4	8.82	9.6	
4	8	11.025	12	

2.5	12.8	17.64	19.2
2	16	22.05	24
1	32	44.1	48

10.1 I²S Clock Usage

The SCK clock of the I²S interface must be used to synchronize the ISD15D00 if an I²S interface is used. The ISD15D00 accepts I²S_SCK clock rates of 32xFs or 64xFs.

Table 10-3 Supported I²S Clock Rates with PLL Settings

I²S_SCK (MHz)	M	N	Fs (kHz)
1.024	1	32	32
2.048	2	32	32
1.4112	1	32	44.1
2.8224	2	32	44.1
1.536	1	32	48
3.072	2	32	48

10.2 INTERNAL OSCILLATOR

The ISD15D00 also provides an internal oscillator that requires only an external resistor to operate. If the device is configured to use the internal oscillator, then a resistor is connected to the XTALIN pin and GND. The internal oscillator with external resistor has an accuracy of ±5% and gives a master sample rate of:

$$F_s = \frac{32 \times 80 \times 10^3}{R_{OSC}} \text{ (kHz) for } M = 2,\ N = 32$$

So if the user connects an 80kohm resistor to the XTALIN and GND, a 32 kHz sample frequency is fed-through the analog path.

11 INITIALIZATION & PLAY FLOWCHART

Whenever the ISD15D00 detect as power-on reset condition or a high on the RESET pin of the device it begins a power-on initialization (POI) sequence. Whenever the ISD15D00 receives a power up command (PU) when it is in a power down state, it begins a power-up initialization (PU) sequence. Voice Macros VM(0) and VM(1) are reserved for POI and PU initialization routines. If no reserved memory exists or if the vectors VM(0) or VM(1) are not set, then a default routine is executed. The default sequence for POI is to power-down the ISD15D00. The default PU sequence is to select a clock configuration of internal oscillator with PLL active for Fs=32kHz.

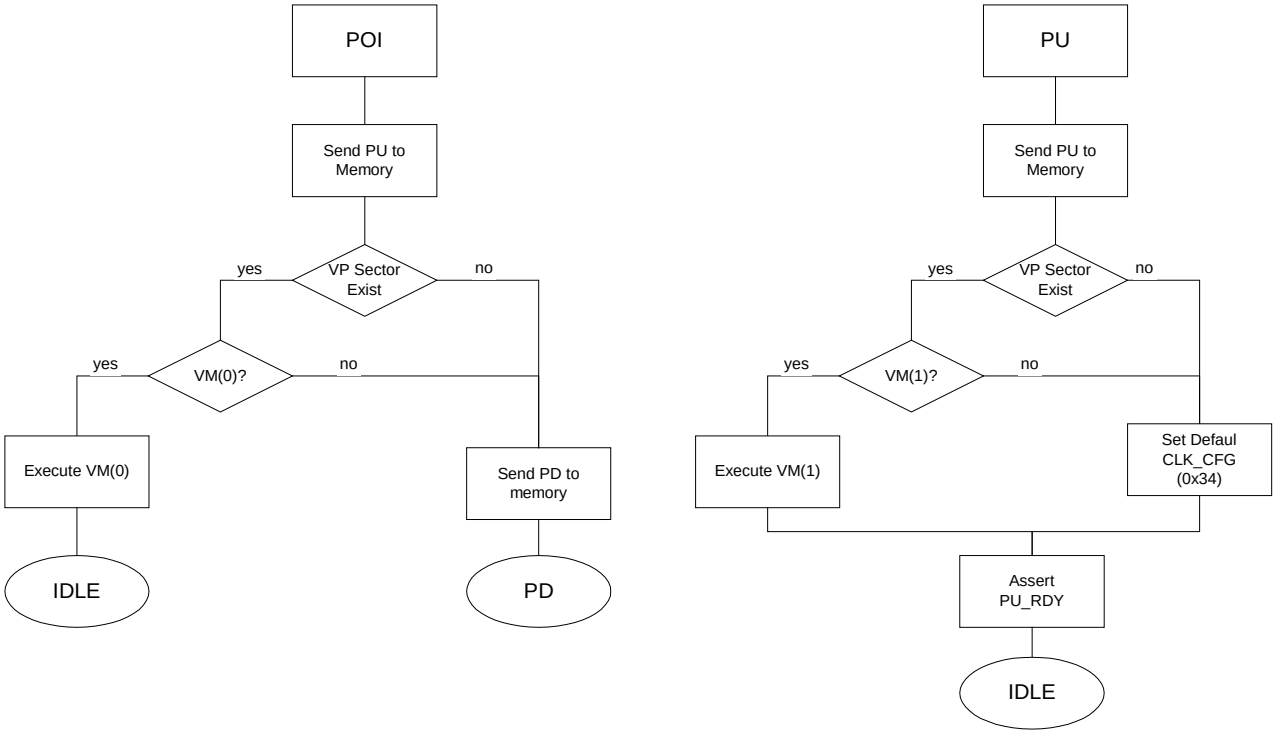


Figure 11-1 POI and PU Initialization Flowcharts

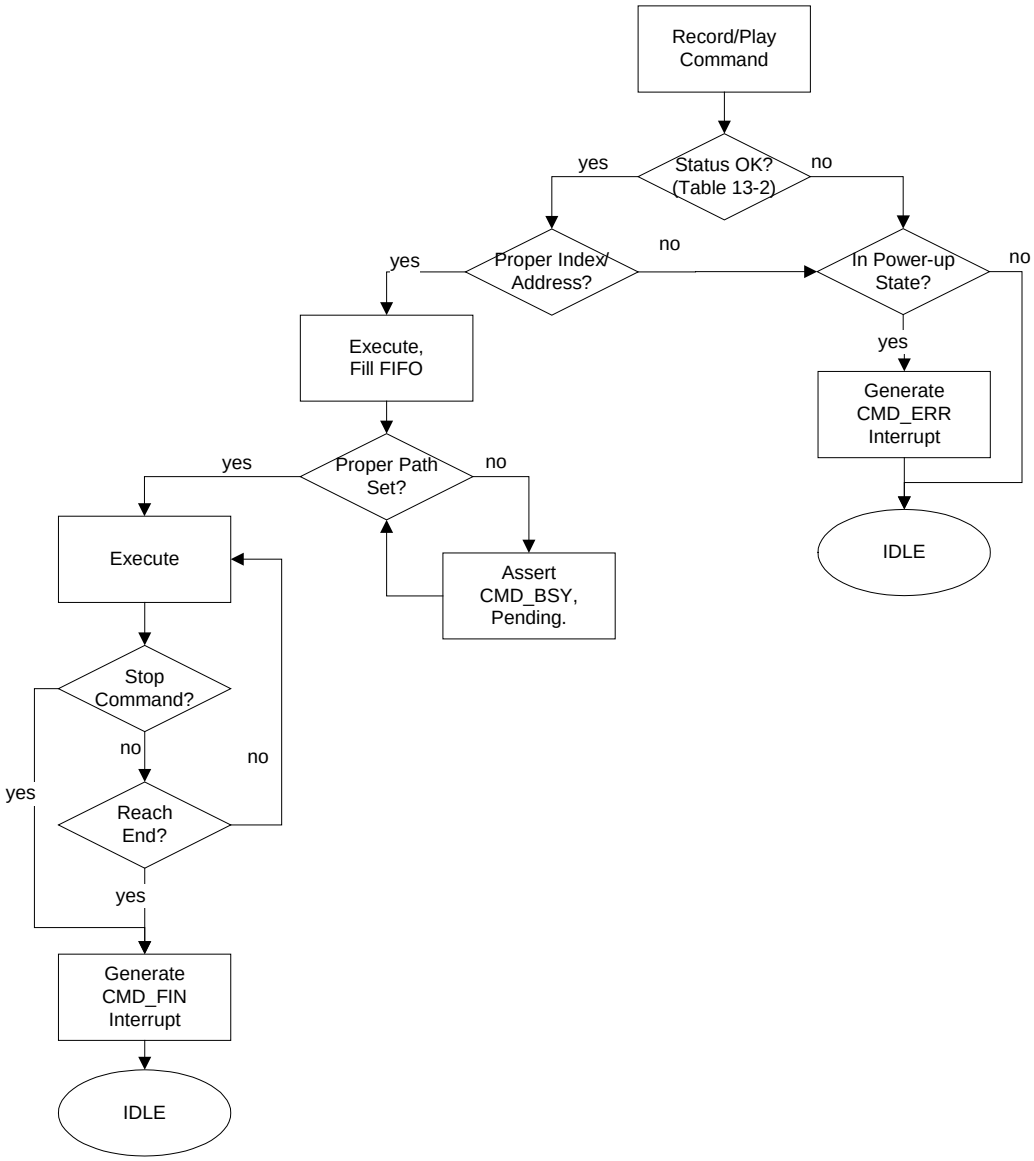


Figure 11-2 Playback Flowchart

12 DEVICE CONFIGURATION AND STATUS

12.1 CLOCK CONFIGURATION

The clock configuration register is accessed via the SET_CLK_CFG command. It configures the clock source of the ISD15D00. The default state of the clock configuration register is0x34, that is internal clock with internal reference, PLL active for 32kHz sample rate and no external clock output. When PLL_BYPASS is set, the PLL is powered down and PLL_REF_CLK is fed directly to MCLK. The CLK_OUT control bits configure the I²S clock pin, SCK, as a clock output to allow the ISD15D00 to provide an oscillator output to another device such as the host microcontroller.

Table 12-1 Clock Configuration Register Description

CLK_CFG							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CLK_OUT[1:0]		CLK_N_DIV[1:0]		CLK_M_DIV[1:0]		CLK_INP_SEL[1:0]	
00		11		01		00	

Default 0x34:

- Internal clock with internal reference
- PLL active for F_s=32khz sample rate
- No external clock output

Table 12-2 Clock Configuration Source

CLK_INP_SEL	
CLK_INP_SEL[1:0]	**Clock Source**
00	Internal Oscillator with Internal Reference
01	I²S SCK Clock
10	Internal Oscillator with Rext
11	XTAL Interface

Table 12-3 Clock PLL M & N Divisor

CLK_M_DIV	
CLK_M_DIV[1:0]	**M**
00	1
01	2
10	3
11	N/A

CLK_N_DIV	
CLK_N_DIV[1:0]	**N**
00	PLL_BYPASS
01	8
10	16
11	32

Table 12-4 External Clock Output

EXT Clock	
CLK_OUT[1:0]	
00	NONE – OFF
01	Fosc
10	PLL_REF_CLK
11	MCLK

12.2 DEVICE STATUS REGISTER

Whenever the ISD15D00 receives an SPI command it also returns its current status via MISO. The details of the status byte are shown below. For commands that are not reading digital data from the device this status byte is sent via MISO for every byte of data sent to the ISD15D00.

Table 12-5 Status Register Description

Status Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PD	DBUF_RDY	INT	-	TALARM	VM_BSY	CBUF_FUL	CMD_BSY

The individual bits of the status register refer to the following conditions:

- **PD** – If this bit is high then the device is powered down. The DBUF_RDY bit will be low, but all device output pins will be high impedance. When PD is high only the READ_STATUS, READ_INT and PWR_UP commands are accepted. If any other command is sent, it is ignored and no interrupt for an error is generated.
- **DBUF_RDY** – in PD this bit is low indicating the device can only accept a PWR_UP (power up) command. When PD is low this bit reflects the state of the RDY/BSY pin.
- **INT** – an interrupt has been generated. The interrupt is cleared by the READ_INT command. Interrupt type can be determined by the bits of the Interrupt Status Byte.
- **TALARM** – Temperature-Alarm indicates that the chip is heated up and the temperature is higher than the specified temperature threshold. Please refer to register 0x30 for details of setting temperature alarm.
- **VM_BSY** – indicates the device is processing a voice macro. The device will not respond to a new audio command until this bit returns low.
- **CBUF_FUL** – indicates that the command buffer is full. No more commands can be queued for execution until this bit returns low.
- **CMD_BSY** – indicates the device is processing a command. Device will not respond to a new command until this bit returns low. If CMD_BSY=1 and CBUF_FUL=0 and VM_BSY=0, a new command will go into the command buffer and execute when the current command finishes. If CMD_BSY=1 and CBUF_FUL=1 or VM_BSY=1 any new audio command will be ignored and generate a command error. For erasing commands like ERASE_MEM and CHIP_ERASE, the user has to poll this bit to see if the erasing is done.

Whenever the ISD15D00 generates an interrupt the Interrupt Status register holds flags that indicate what type of interrupt was generated. These flags will remain set until a READ_INT command clears them and the interrupt pin.

Table 12-6 Interrupt Status Register Description

Interrupt Status Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TALARM	MPT_ERR	WR_FIN	CMD_ERR	OVF_ERR	CMD_FIN	-	-

The individual bits of the status register refer to the following conditions:

INT – an interrupt has been generated. The interrupt is cleared by the READ_INT command.

- **TALARM** – Temperature-Alarm indicates that the chip is heated up and the temperature is higher than the specified temperature threshold. Please refer to register 0x30 for details of setting temperature alarm.

- **MPT_ERR** – Indicates a memory protection error. Digital access attempted for protected memory.
- **WR_FIN** – indicates a digital write command has finished writing to the flash memory.
- **CMD_ERR** – an invalid command was sent to the device. Command was ignored because the command buffer was full, a voice macro was active or the device was not ready to respond to an erase command.
- **OVF_ERR** – This error is generated if host illegally tries to read or write data while RDY/BSYB pin is low. It is also generated if a digital read or write attempts to read or write past the end of memory.
- **CMD_FIN** – This bit indicates an interrupt was generated because a command finished executing. A CMD_FIN interrupt will be generated each time an audio play or voice macro finishes.

12.3 DEVICE CONFIGURATION REGISTERS

The configuration of the ISD15D00 is achieved by configuration registers as described below.

Table 12-7 CFG0 Register

CFG0 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SR[2:0]			CMP[4:0]				
011			00100				

Default 0x64:

- 4-bit ADPCM
- Ratio to Fs = 4

Configuration register CFG0 controls the sample rate and compression algorithm. It can also override sample rate setting for playback by setting bit 0 of CFG1 high. SR[2:0] = CFG0[7:5] controls the sample rate, and CMP[4:0]=CFG0[4:0] controls the compression. An explanation of these follows below.

Table 12-8 CFG0 Register Compression Type.

Compression Type	Bit rate (bits/sample)	CMP[4:0]	
		(Dec)	(Hex)
ADPCM	2	2	0x02
ADPCM	3	3	0x03
ADPCM	4	4	0x04
ADPCM	5	5	0x05
µ-Law	6	16	0x10
µ-Law	7	17	0x11
µ-Law	8	18	0x12
Dµ-Law	6	20	0x14
Dµ-Law	7	21	0x15
Dµ-Law	8	22	0x16
PCM	8	24	0x18
PCM	10	25	0x19
PCM	12	27	0x1B

Table 12-9 CFG0 Sample Rate Control

Ratio to Fs	Sample Rate (kHz) (for Fs=32kHz)	Code SR[2:0]	CFG0[7:0] (Dec)	CFG0[7:0] (Hex)
8	4	0	0	0x00
6	5.333	1	32	0x20
5	6.4	2	64	0x40
4	8	3	96	0x60
2.5	12.8	4	128	0x80
2	16	5	160	0xA0
1	32	6	192	0xC0

The current operational mode of the ISD15D00 can also be queried by setting CFG1[4] and reading CFG0. Under this condition, rather than reading back the configuration register, the result will be current audio path sample rate and compression scheme.

Table 12-10 CFG1 Register

CFG1 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	LRMP	CFG0_READ	-	NRMP	SRSIL	SRCFG

Default 0x00:

- Sample rate is set by the audio header.
- Whenever a change in sample rate is detected between two consecutive messages, a period of silence is automatically inserted.
- If an audio playback finishes at a non-zero level the input to the signal path will be ramped to zero.
- A read of CFG0 will read the setting of the CFG0 register rather than the current operating mode of compression and sample rate.

Configuration register CFG1 controls how compressed audio is treated by the compression block:

- **SRCFG** – Forces the sample rate to be set by the CFG0 register by setting this bit to one, overriding any sample rate contained in the audio header.
- **SRSIL** – Under normal circumstances, whenever a change in sample rate is detected between two consecutive messages a period of silence is automatically inserted. This is to prevent any transients in the signal path occurring as filter coefficients are changed. To turn off this silence insertion set this bit to one.
- **NRMP** – Under normal conditions, if an audio playback finishes at a non-zero level, the input to the signal path will be ramped to zero. This prevents a DC offset appearing on the output. To turn this feature off, set this bit to one and the input to the signal path will not be ramped. Please note that **NRMP** and **LRMP** should not be set at the same time.
- **CFG0_READ** – When this bit is set, a read of CFG0 will result in the current operation mode of compression and sample rate rather than the setting of the CFG register. A write to CFG0 will still result in setting the register, but the contents of the register cannot be read back until CFG0_READ is set to zero.
- **LRMP** – Under normal conditions, if an audio playback finishes at a non-zero level, the input to the signal path will be ramped to zero. This prevents a DC offset appearing on the output. To

turn this feature off, set this bit to one and the input to the signal path will not be ramped during the loop-play, but will be ramped to zero when the playback finishes or being stopped by a STOP or STOP_LP command. Please note that **NRMP** and **LRMP** should not be set at the same time.

Table 12-11 CFG2 Register

CFG2 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I^2S_IN	DECODE	SPI_IN	I^2S_OUT	DAC_OUT	PWM_OUT	-	SPI_OUT

Default 0x00:

- All digital paths are disabled.

Configuration register CFG2 controls how digital audio signal path is configured:

The ISD15D00 Voice Prompt Editor provides a graphic view of the path configuration to help users get a better understanding of the audio signal path and largely ease the path setting.

- **SPI_OUT** – Output signal data to SPI. If DECODE is selected, the signal path is bypassed and ISD15D00 is ready for SPI_Playback operation. Use the SPI_PCM_READ command to read the audio data out the SPI interface.
- **PWM_OUT** – Output signal to PWM.
- **DAC_OUT** – Output signal to AUXOUT.
- **I^2S_OUT** – Output signal data to I^2S interface
- **SPI_IN** – Input data from SPI. SPI_IN and DECODE cannot be both on at the same time.
- **DECODE** – Used in conjunction with a play operation. When selected the signal path picks up data from the de-compressor and plays it to the corresponding outputs selected.
- **I^2S_IN** – Input data from I^2S.

Table 12-12 CFG3 Register

CFG3 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLC[7:0]							

Default 0x00:

- 0 dB attenuation to the output signal volume

Configuration register CFG3 sets the output signal volume. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-13 CFG5 Register

CFG5 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PU_DAC	-	PU_OP_SUM	-	PU_AUXIN	AUXIN_GAIN[1:0]		-

Default 0x00:

- All blocks in the analog signal path are powered off.

Configuration register CFG5 controls the power up state of blocks in the analog signal path along with the gain of the AUXIN input:

- **AUXIN_GAIN**- Sets the gain of the AUXIN input buffer.
- **PU_AUXIN** – Powers up the AUXIN input buffer.
- **PU_OP_SUM** – Powers up the output summation amplifier (SUM2).
- **PU_DAC** – Powers up the digital-to-analog converter (DAC).

Table 12-14 AUXIN Gain Configuration

AUXIN_GAIN	
AUXIN_GAIN[1:0]	**Gain (dB)**
00	0
01	3
10	6
11	9

Table 12-15 CFG6 Register

CFG6 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AUX_SEL[1:0]		-		-	-	-	PU_AUXOUT

Default 0x00:

Configuration register CFG6 controls the analog signal path functions:

- **PU_AUXOUT** – Powers up the AUXOUT output buffer.
- **AUX_SEL** – Selects the input source to the AUXOUT buffer.

Table 12-16 AUXOUT Source Selection

AUX_SEL	
AUX_SEL[1:0]	**Source**
00	-
01	AUXIN
10	SUM2
11	DAC

Table 12-17 CFG8 Register

CFG8 Configuration Register				
Bit 7 - 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	MUTE_SUM2	MUTE_AUXOUT	-

Default 0x00:

- NOT mute on analog signal path.

Configuration register CFG8 controls the analog signal path functions:

- **MUTE_AUXOUT** – Mutes AUXOUT output.
- **MUTE_SUM2** – Mutes the SUM2_MUX input to the SUM2 summation block.

Bits 4-7 are unused and have no effect on the signal path.

Table 12-18 CFG9 Register

CFG9 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PWMF[3:0]				I²S_L_IN	I²S_R_IN	I²S_L_OUT	I²S_R_OUT

Default 0x00:

- Disable I²S function.
- PWM nominal frequency is 256 kHz when master sample rate is 32 kHz.

Configuration register CFG9 controls the functionality of the I²S audio interface:

- **I²S_L_IN** – Enables I²S input from the left (WS=0) channel to the signal path.
- **I²S_R_IN** – Enables I²S input from the right (WS=1) channel to the signal path.
- **I²S_L_OUT** – Enables signal path output to the left (WS=0) I²S channel.
- **I²S_R_OUT** – Enables signal path output to the right (WS=1) I²S channel.
- In addition to this basic functionality these bits are decoded to determine the whether mixing or feed-through occurs in the I²S path. See I²S section for details.
- **PWMF[3:0]** – Adjusts the nominal frequency of the PWM driver. This frequency is 1MHz/PWMF for all settings except 0, where frequency = 256kHz. Numbers are relative to a 32kHz master sample rate.

Table 12-19 I²S Selection

I²S Channel Selection	
CFG9[3:0]	**Description**
0000	No I²S input or output selected
1111	Stereo Feed-through.
10XX	Left channel in; can output to both/either
01XX	Right channel in can output to both/either.
1100, 1101, 1110	Left+Right mixed for either channel output.

Table 12-20 CFG14 Register

CFG14 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLB[7:0]							

Default 0x00:

- 0 dB attenuation to the volume control coming from the decompression block.

Configuration register CFG14 controls the volume level coming from the decompression block. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-21 CFG15 Register

CFG15 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLA[7:0]							

Default 0x00:

- 0 dB attenuation to the volume control coming from the I^2S.

Configuration register CFG15 controls the volume level coming from the I^2S input. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-22 CFG17 Register

CFG17 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PLL_LOCK	-	I^2S_MM	I^2S_ATT	DECODE	COMP_ACTIVE	-	-

Default 0x01:

- Disable the 3dB attenuation when left and right channel are mixed.
- I^2S slave mode: ISD15D00 accepts SCK and WS from a bus master.

Configuration register CFG17 controls how the configuration registers are applied:

- **COMP_ACTIVE –** Indicates that compression or decompression is active. (Read only).
- **DECODE** – Indicates that compressor is in decode mode. (Read Only)
- **I^2S_MM** – Enables I^2S master mode. With this bit set to one, the device generates I^2S SCK and WS at 32fs.
- **I^2S_ATT** – Enables 3dB of attenuation when left and right channels are mixed.
- **PLL_LOCK** – Indicates that the PLL is locked. If this bit is zero it indicates the PLL is attempting to lock on the input clock. (Read Only)

Table 12-23 CFG18 Register

CFG18 Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANA_EN	MUTE_SPK-	BTL_MODE	SPK-_IN_SEL	PU_SPK-	MUTE_SPK+	SPK+_IN_SEL	PU_SPK+

Default 0x00:

- PWM is selected by default.

CFG18 controls the configuration of the two pins SPK+ and SPK-:

- **PU_SPK+** – Powers up SPK+.
- **SPK+_IN_SEL** –
  - When ANA_EN = 1 and BTL_MODE = 1:
    - SPK+_IN_SEL selects the source of the Class-AB BTL output:
      - SPK+_IN_SEL = 1: the source is DAC.
      - SPK+_IN_SEL = 0: the source is SUM2.
  - When ANA_EN = 1 and BTL_MODE = 0 (separate outputs):
    - SPK+_IN_SEL selects the source of the SPK+ output:
      - SPK+_IN_SEL = 1: the source is DAC.
      - SPK+_IN_SEL = 0: the source is SUM2.
- **MUTE_SPK+ –** Mutes SPK+ output.
- **PU_SPK-** – Powers up SPK-.
- **SPK-_IN_SEL** –
  - When ANA_EN = 1 and BTL_MODE = 1: SPK-_IN_SEL is not functional.
  - When ANA_EN = 1 and BTL_MODE = 0: SPK-_IN_SEL selects the signal source of the SPK- pin.
    - When SPK-_IN_SEL =1: the source is SUM2.
    - When SPK-_IN_SEL =0: the source is AUXIN.
- **BTL_MODE –**
  - When ANA_EN = 1 and BTL_MODE = 1: the speaker driver operates in Class-AB BTL mode for driving a speaker.
  - When ANA_EN = 1 and BTL_MODE = 0: each speaker driver pin operates independently.
- **MUTE_SPK- –** Mutes SPK- output.
- **ANA_EN** –
  - When ANA_EN = 1: the speaker driver operates in the analog mode.
  - When ANA_EN = 0: the speaker driver operates in the PWM mode. When operating in PWM mode, all remaining bits in CFG18 are not functional.

The figure below shows an example of Class-AB BTL setting from the DAC.

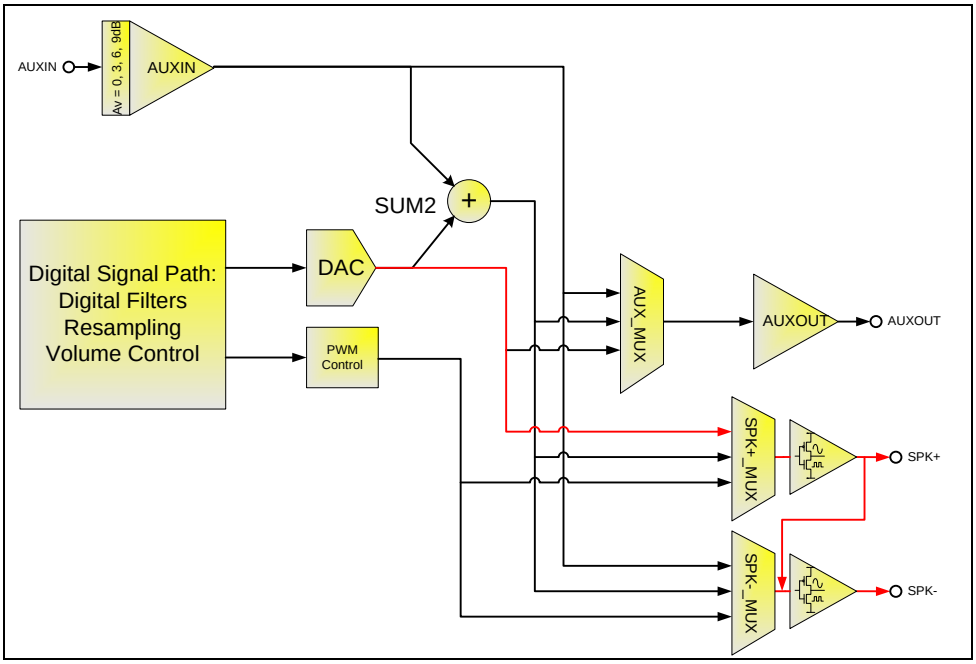


Figure 12-1 DAC to Class-AB BTL (the red line)

Table 12-24 CFG19 Register

CFG19 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 DOUT	GPIO6 DOUT	GPIO5 DOUT	GPIO4 DOUT	GPIO3 DOUT	GPIO2 DOUT	GPIO1 DOUT	GPIO0 DOUT

Default 0x00:

This register sets the value to output to GPIO when OE is 1.

Table 12-25 CFG1A Register

CFG1A Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 OE	GPIO6 OE	GPIO5 OE	GPIO4 OE	GPIO3 OE	GPIO2 OE	GPIO1 OE	GPIO0 OE

Default 0x00:

- Set to input (output disabled).

This register sets Output-Enable to GPIO

- 1: output enabled.
- 0: output disabled.

Table 12-26 CFG1B Register

CFG1B Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 PE	GPIO6 PE	GPIO5 PE	GPIO4 PE	GPIO3 PE	GPIO2 PE	GPIO1 PE	GPIO0 PE

Default 0xFF:

- pull up/down enabled.

This register sets Pull-up/down-Enable to GPIO

- 1: pull up/down enabled.
- 0: pull up/down disabled.

Table 12-27 CFG1C Register (Read Only)

CFG1C Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 DIN	GPIO6 DIN	GPIO5 DIN	GPIO4 DIN	GPIO3 DIN	GPIO2 DIN	GPIO1 DIN	GPIO0 DIN

This register monitors the GPIO input value.

Table 12-28 CFG1D Register

CFG1D Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 PS	GPIO6 PS	GPIO5 PS	GPIO4 PS	GPIO3 PS	GPIO2 PS	GPIO1 PS	GPIO0 PS

Default 0xFF:

- Set to pull-up.

This register selects Pull-up or pull-down when PE is 1.

- 1: pull up
- 0: pull down

Table 12-29 CFG1E & CFG1F Register

CFG1E & CFG1F Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG1E AF1 (GPIO Alternative Function 1)							
CFG1F AF0 (GPIO Alternative Function 0)							

CFG1E Default 0x00:

CFG1F Default 0x0F:

- GPIO 7 ~ 4: GPIO pins.
- GPIO 3 ~ 0: SPI interface.

ISD15D00 has eight GPIO pins in total. Each GPIO pin is configurable: GPIO pins 7 ~ 4 could be either I²S interface or general I/O pins. GPIO pins 3 ~ 0 could be either SPI interface or general I/O pins. Regardless how the GPIO pins 0 and 1 are configured, these two pins turn into the SPI interface whenever the SSB pin goes low and resume back to their configurations when the SSB pin goes back to high. On the contrary, GPIO pins 2 and 3 don't automatically change their configurations when SSB pin goes low. Users shall especially pay attention to the GPIO2 (RDY/BSYB) as RDY/BSYB pin is required when doing the digital-read or digital-write, but GPIO2 does not automatically change to RDY/BSYB pin as mentioned above.

AF1 together with AF0 configure the eight GPIO pins to one of the four possible configurations as shown in the table below.

Table 12-30

	AF0 = 0	AF0 = 1
AF1 = 0	General I/O	SPI or I2S depending on which GPIO pin it is.

AF1 = 1	Falling edge triggers the Voice Macro	Falling and rising edges both trigger the Voice Macro.

R0 ~ R7 in the following tables serve two purposes:

- R0 ~ R7 store the VP/VM indexes for the indirect playback commands. Indirect Playback commands include:
  - PLAY_VP@Rn
  - PLAY_VP_LP@Rn
  - EXE_VM@Rn
- When a GPIO pin is configured as a trigger to wake up the ISD15D00 and runs a specified VM, the VM index is stored in Rn, n = 0 ~ 7 (corresponding to GPIO pins 0 ~ 7).

Table 12-31 CFG20 & CFG21 Register

CFG20 & CFG21 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG20 R0[7:0]							
CFG21 R0[15:8]							

Table 12-32 CFG22 & CFG23 Register

CFG22 & CFG23 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG22 R1[7:0]							
CFG23 R1[15:8]							

Table 12-33 CFG24 & CFG25 Register

CFG24 & CFG25 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG24 R2[7:0]							
CFG25 R2[15:8]							

Table 12-34 CFG26 & CFG27 Register

CFG26 & CFG27 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG26 R3[7:0]							
CFG27 R3[15:8]							

Table 12-35 CFG28 & CFG29 Register

CFG28 & CFG29 Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFG28 R4[7:0]							
CFG29 R4[15:8]							

Table 12-36 CFG2A & CFG2B Register

CFG2A & CFG2B Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG2A R5[7:0]							
CFG2B R5[15:8]							

Table 12-37 CFG2C & CFG2D Register

CFG2C & CFG2D Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG2C R6[7:0]							
CFG2D R6[15:8]							

Table 12-38 CFG2E & CFG2F Register

CFG2E & CFG2F Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG2E R7[7:0]							
CFG2F R7[15:8]							

Table 12-39 CFG30 Register

CFG30 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TALARM	TSENSE	0	1	DISCH_ REG	-	RESET_ CHECKSUM	SIL_ 32_8

Default 0xD1 (users should not change bits 4 ~ 7):

- Silence is played in 32ms increments.
- The 3V flash regulator output is not discharged on power down.

This register controls the following:

- **SIL_32_8** – when set to 1, silence is played in 32ms increments. When set to 0, silence is played in 8ms increments.
- **RESET_CHECKSUM** – write a 1 followed a 0 to this bit to reset the CHECKSUM CFG31 ~ CFG34.
- **DISCH_REG –** when this bit is set, a 500-ohm pull-down will be enabled on the 3V flash regulator output on power down to discharge the regulator.
- **TSENSE** – when this bit is set, device will issue interrupt on INTB pin when device temperature exceeds the threshold.
- **TALARM –** when this bit is set, device will shutdown itself when device temperature exceeds the threshold.

Table 12-40 CFG31 ~ CFG34 Register

CFG31 ~ CFG34 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CFG31 CHECKSUM[7:0]							
CFG32 CHECKSUM[15:8]							
CFG33 CHECKSUM[23:16]							
CFG34 CHECKSUM[31:24]							

CFG31 ~ CFG34 are read-only registers.

The SPI command CHECKSUM initiates a 4-byte checksum calculation from the very beginning to the specified end address. The calculated checksum is stored in registers CFG31 ~ CFG34. To re-calculate the checksum with a different end address, users have to set register CFG30 bit-1 to clear the registers CFG31 ~ CFG0x34.

Table 12-41 CFG35 Register

CFG35 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SOFT_MUTE_EN	SOFT_MUTE	-	-	-	-	-	-

Default 0x00:

- Soft-mute block is disabled.

This register soft-mutes the SPK +/-. Different from the normal-mute (CFG18 bit-2 & bit-6), soft-mute ramps the input to the signal path to zero before it mutes the output.

- **SOFT_MUTE_EN –** Enables the soft-mute block.
- **SOFT_MUTE** – soft-mute the SPK +/-.

Table 12-42 CFG36 Register

CFG36 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	-	-	-	VMID_CTRL		

Default 0x00:

- AUTO: during power-down, V_{MID} is tied to V_{SSA}. Once the ISD15D00 is powered up, V_{MID} automatically begins to ramp to V_{CCA} /2.

This register controls pin 45 V_{MID}, the middle voltage reference of V_{CCA}. V_{MID} is the analog ground reference. It is the middle of swings of analog input (Aux-in) and analog outputs (Aux-out and Class-AB).

- **000 –** AUTO: during power-down, V_{MID} is tied to V_{SSA}. Once the ISD15D00 is powered up, V_{MID} automatically begins to ramp to V_{CCA} /2.
- **001** – 5K: V_{MID} ramps to V_{CCA} /2 through a 5k-ohm resistor.
- **010** – 600K: V_{MID} ramps to V_{CCA} /2 through a 600k-ohm resistor.
- **011** – 600K to V_{SSA}: V_{MID} ramps to V_{SSA} through a 600k-ohm pull-down resistor.
- **100** – Reserved.
- **101** – 5K to V_{SSA}: V_{MID} ramps to V_{SSA} through a 5k-ohm pull-down resistor.
- **110** – 5K to V_{CCA}: V_{MID} ramps to V_{CCA} through a 5k-ohm pull-high resistor.
- **111** – Reserved.

Please note that by default V_{MID} does not ramp before POI/PU Macro is finished. So, V_{MID} is held low in POI and PU. If users want to use analog outputs in POI or PU users must configure V_{MID}.

12.4 DEVICE IDENTIFICATION REGISTERS.

By sending the command READ_ID the device responds with a four-byte identification. The first byte reports the ISD15D00 family version. The following three bytes are a JEDEC compliant code indicating the memory type.

13 SPI COMMANDS

The ISD15D00 provides SPI commands including: (1) 11 audio play commands, (2) 3 device status commands, (3) 5 digital commands, and (4) 6 device configuration commands.

The following section contains a list of all SPI commands and their function.

Table 13-1 SPI Commands

Instructions	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4 … Byte n	Description
PLAY_VP	0xA6	Index[15:8]	Index[7:0]			Play Voice Prompt Index
PLAY_VP@Rn	0xAE	n = 0 …7				Play Voice Prompt; Index @ Rn
PLAY_VP_LP	0xA4	Index[15:8]	Index[7:0]	LoopCnt[15:8]	LoopCnt[7:0]	Loop Play Voice Prompt Index
PLAY_VP_LP@Rn	0xB2	n = 0 …7	LoopCnt[15:8]	LoopCnt[7:0]		Loop Play Voice Prompt; Index @ Rn
STOP_LP	0x2E					Stop Loop Play Voice Prompt
EXE_VM	0xB0	Index[15:8]	Index[7:0]			Execute voice macro Index
EXE_VM@Rn	0xBC	n = 0 …7				Execute voice macro; Index @ Rn
PLAY_SIL	0xA8	LEN[7:0]				Play silence for LEN*32ms
STOP	0x2A					STOP current playback operation.
SPI_PCM_READ	0xAC	D0[7:0]	D0[15:8]	D1[7:0]	D1[15:8] …Dn[7:0] Dn[15:8]	Receive 16 bit PCM audio data [low-byte, high-byte] from ISD15D00 via SPI interface.
SPI_SND_DEC	0xC0	D0[7:0]	D1[7:0]	D2[7:0]	D3[7:0] …Dn[7:0]	Send compressed audio data to ISD15D00 via SPI interface for decoding.
READ_STATUS	0x40	XX	XX	XX	…	Query status of ISD15D00.
READ_INT	0x46	XX	XX	XX	…	Query status and clear interrupt flags of ISD15D00.
READ_ID	0x48	XX	XX	XX	XX	Read device ID of ISD15D00.
DIG_READ	0xA2	A[23:16]	A[15:8]	A[7:0]	XX, … XX	Read digital data from address A.
DIG_WRITE	0xA0	A[23:16]	A[15:8]	A[7:0],	D0[7:0], … Dn[7:0]	Write digital data from address A.
ERASE_MEM	0x24	SA[23:16]	SA[15:8]	SA[7:0]	EA[23:16], EA[15:8], EA[7:0]	Erase sectors of memory from sector containing SA to sector containing EA.
CHIP_ERASE	0x26	0x01				Initiate a mass erase of memory.
CHECKSUM	0xF2	EA[23:16]	EA[15:8]	EA[7:0]		Calculate checksum from very beginning to the specified end address.
PWR_UP	0x10					Power up ISD15D00
PWR_DN	0x12					Power down ISD15D00
SET_CLK_CFG	0xB4	CFG_CLK[7:0]				Set clock configuration register.

Instructions	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4 … Byte n	Description
RD_CLK_CFG	0xB6	XX				Read clock configuration register.
WR_CFG_REG	0xB8	REG[7:0]	D0[7:0], ...Dn[7:0]			Write data D0..Dn to configuration register(s) starting at configuration register REG.
RD_CFG_REG	0xBA	REG[7:0]	XX, ...XX			Read configuration register(s) starting at configuration register REG.

Each command will be accepted if certain conditions are met as in the following table, or a CMD_ERR interrupt will be generated and the command ignored.

Table 13-2 Commands vs. Status

Instructions	Op Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PD	DBUF_RDY	INT	-	TALARM	VM_BSY	CBUF_FUL	CMD_BSY
PLAY_VP	0xA6	0	***1***	x	-	x	0	0	x
PLAY_VP@Rn	0xAE	0	***1***	x	-	x	0	0	x
PLAY_VP_LP	0xA4	0	***1***	x	-	x	0	0	x
PLAY_VP_LP@Rn	0xB2	0	***1***	x	-	x	0	0	x
STOP_LP	0x2E	0	***1***	x	-	x	x	x	x
EXE_VM	0xB0	0	***1***	x	-	x	0	0	0
EXE_VM@Rn	0xBC	0	***1***	x	-	x	0	0	0
PLAY_SIL	0xA8	0	***1***	x	-	x	0	0	x
STOP	0x2A	0	***1***	x	-	x	x	x	x
SPI_PCM_READ	0xAC	0	***1***	x	-	x	x	x	x
SPI_SND_DEC	0xC0	0	***1***	x	-	x	0	0	0
READ_STATUS	0x40	x	x	x	-	x	x	x	x
READ_INT	0x46	x	x	x	-	x	x	x	x
READ_ID	0x48	0	***1***	x	-	x	x	x	x
DIG_READ	0xA2	0	***1***	x	-	x	x	x	x
DIG_WRITE	0xA0	0	***1***	x	-	x	x	x	x
ERASE_MEM	0x24	0	***1***	x	-	x	0	0	0
CHIP_ERASE	0x26	0	***1***	x	-	x	0	0	0
CHECKSUM	0xF2	0	***1***	x	-	x	0	0	0
PWR_UP	0x10	***1***	0	x	-	x	x	x	x
PWR_DN	0x12	0	***1***	x	-	x	x	x	x
SET_CLK_CFG	0xB4	0	***1***	x	-	x	0	0	0
RD_CLK_CFG	0xB6	0	***1***	x	-	x	x	x	x
WR_CFG_REG	0xB8	0	***1***	x	-	x	x	x	x

Instructions	Op Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PD	DBUF_RDY	INT	-	TALARM	VM_BSY	CBUF_FUL	CMD_BSY
RD_CFG_REG	0xBA	0	*1*	x	-	x	x	x	x

13.1 AUDIO PLAY COMMANDS

This section describes the 11 audio commands that can be sent to the device.

13.1.1 Play Voice Prompt

PLAY_VP				
Byte Sequence:	Host controller	0xA6	*Index*[15:8]	Index[7:0]
	ISD15D00	Status Byte	Status Byte	Status Byte
Description:	Play Voice Prompt *Index*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command initiates a play of a pre-recorded voice-prompt. Before execution of command a valid signal path must be set up, and the device must have space in the audio command buffer. After completion of playback, the device will generate an interrupt. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once playback is finished a CMD_FIN interrupt will be generated.

13.1.2 Play Voice Prompt @Rn, n = 0 ~ 7

PLAY_VP@Rn				
Byte Sequence:	Host controller	0xAE	*n = 0 ~ 7*	
	ISD15D00	Status Byte	Status Byte	
Description:	Play Voice Prompt, *Index@Rn*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command is same as PlayVP except that the 16bit index is stored in Rn, n = 0 ~ 7.

- R0[7:0] = CFG20, R0[15:8] = CFG21
- R1[7:0] = CFG22, R1[15:8] = CFG23
- R2[7:0] = CFG24, R2[15:8] = CFG25
- R3[7:0] = CFG26, R3[15:8] = CFG27
- R4[7:0] = CFG28, R4[15:8] = CFG29
- R5[7:0] = CFG2A, R5[15:8] = CFG2B
- R6[7:0] = CFG2C, R6[15:8] = CFG2D
- R7[7:0] = CFG2E, R7[15:8] = CFG2F

13.1.3 Play Voice Prompt, Loop

PLAY_VP_LP						
Byte Sequence:	Host controller	0xA4	*Index*[15:8]	Index[7:0]	LoopCnt[15:8]	LoopCnt[7:0]
	ISD15D00	Status Byte	Status Byte	Status Byte	Status Byte	Status Byte
Description:	Play Voice Prompt *Index, Loop*					
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.					

This command initiates a loop-play of a pre-recorded voice-prompt. Number of play-loops is specified in LoopCnt[15:0]. Setting LoopCnt to 0 makes an endless play, which can only be ended by a STOP or STOP_LP command. Before execution of command a valid signal path must be set up, and the device must have space in the audio command buffer. After completion of playback, the device will generate an interrupt. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once playback is finished a CMD_FIN interrupt will be generated.

13.1.4 Play Voice Prompt, Loop, @Rn, n = 0 ~ 7

PLAY_VP_LP@Rn					
Byte Sequence:	Host controller	0xB2	*n = 0 ~ 7*	LoopCnt[15:8]	LoopCnt[7:0]
	ISD15D00	Status Byte	Status Byte	Status Byte	Status Byte
Description:	Play Voice Prompt, Loop, *Index@Rn*				

Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.

This command is same as PlayVP_LP except that the 16bit index is stored in Rn, n = 0 ~ 7.

- R0[7:0] = CFG20, R0[15:8] = CFG21
- R1[7:0] = CFG22, R1[15:8] = CFG23
- R2[7:0] = CFG24, R2[15:8] = CFG25
- R3[7:0] = CFG26, R3[15:8] = CFG27
- R4[7:0] = CFG28, R4[15:8] = CFG29
- R5[7:0] = CFG2A, R5[15:8] = CFG2B
- R6[7:0] = CFG2C, R6[15:8] = CFG2D
- R7[7:0] = CFG2E, R7[15:8] = CFG2F

13.1.5 Stop Loop-Play Command

STOP_LP				
Byte Sequence:	Host controller	0x2E		
	ISD15D00	Status Byte		
Description:	Stop current loop-play command and flush command buffer.			
Interrupt Generation:	Command itself does not generate interrupt, only those commands that it is stopping.			

This command stops any current PLAY_VP_LP or PLAY_VP_LP@Rn command active in the ISD15D00. The STOP_LP command does not flush the audio command buffer; that is, any command queued in the buffer when a STOP_LP is issued will be executed thereafter. When device has finished the active command a CMD_FIN interrupt will be generated. If there is no active command then STOP will have no effect.

13.1.6 Execute Voice Macro

EXE_VM				
Byte Sequence:	Host controller	0xB0	*Index*[15:8]	Index[7:0]
	ISD15D00	Status Byte	Status Byte	Status Byte
Description:	Play voice macro *Index*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command initiates the execution of a pre-recorded voice macro. After completion of the voice macro the device will generate a CMD_FIN interrupt. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once voice macro execution is finished a CMD_FIN interrupt will be generated.

13.1.7 Execute Voice Macro @Rn, n = 0 ~ 7

EXE_VM@Rn				
Byte Sequence:	Host controller	0xBC	*n = 0 ~ 7*	
	ISD15D00	Status Byte	Status Byte	
Description:	Play voice macro *Index@Rn*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command is same as EXE_VM except that the 16bit index is stored in Rn, n = 0 ~ 7.

- R0[7:0] = CFG20, R0[15:8] = CFG21
- R1[7:0] = CFG22, R1[15:8] = CFG23
- R2[7:0] = CFG24, R2[15:8] = CFG25
- R3[7:0] = CFG26, R3[15:8] = CFG27
- R4[7:0] = CFG28, R4[15:8] = CFG29
- R5[7:0] = CFG2A, R5[15:8] = CFG2B
- R6[7:0] = CFG2C, R6[15:8] = CFG2D
- R7[7:0] = CFG2E, R7[15:8] = CFG2F

13.1.8 Play Silence

PLAY_SIL				
Byte Sequence:	Host controller	0xA8	*LEN*[7:0]	
	ISD15D00	Status Byte 0	Status Byte 0	
Description:	Play silence for LEN*32ms			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when silence playback complete.			

This command plays a period of silence to the signal path. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. After completion, the device will generate an interrupt. The length of silence played is determined by the data byte, LEN, sent. Silence is played in 32ms increments (at signal path sampling frequency of 32kHz), total silence played is LEN*32ms.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once silence play is finished a CMD_FIN interrupt will be generated.

13.1.9 Stop Command

STOP				
Byte Sequence:	Host controller	0x2A		
	ISD15D00	Status Byte		
Description:	Stop current audio command and flush command buffer.			
Interrupt Generation:	Command itself does not generate interrupt, only those commands that it is stopping.			

This command stops any current audio command active in the ISD15D00. If a PLAY_VP, EXE_VM or PLAY_SIL command is active playback is stopped immediately. The STOP command flushes the audio command buffer, that is any command queued in the buffer when a STOP is issued will not be executed. When device has finished the active command a CMD_FIN interrupt will be generated. STOP will not stop an ERASE_MEM operation. If there is no active command then STOP will have no effect.

13.1.10 SPI Read PCM Data

SPI_PCM_READ							
Byte Sequence:	Host controller	0xAC					
	ISD15D00	Status Byte	D0[7:0]	D0[15:8]	….	Dn[7:0]	Dn[15:8]
Description:	Read audio data via SPI interface.						
Interrupt Generation:	OVF_ERR if RDY/BSY violated.						

This command allows the user to receive audio data, in 16bit PCM format, from the SPI interface for feed-through or playback. Before execution of command a valid signal path must be set up.

If receiving audio data from memory (SPI playback), then: (1) signal path must be set up for SPI output from the compressor. (2) A valid play command is then sent; valid play commands include PlayVP, PlayVP@Rn, PlayVP_LP, PlayVP_LP@Rn, ExeVM and ExeVM@Rn. (3) Followed by the SPI_PCM_READ command. Multiple SPI_PCM_READ commands can be sent. (4) To finish receiving data a STOP command is sent and device will generate a CMD_FIN interrupt.

When the end of message is reached a CMD_FIN interrupt will be generated and zero will be sent as data. If the valid play command in step (2) is ExeVM, then a CMD_FIN interrupt will be generated at the end of voice macro.

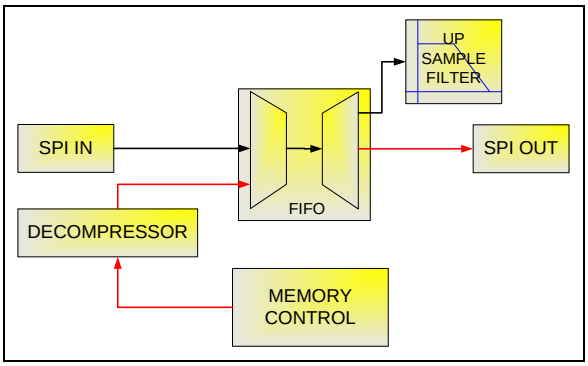


Figure 13-1 SPI Playback

The RDY/BSYB pin will go low whenever the internal FIFO is empty. If no path or playback operation is set up then RDY/BSYB pin will be low until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated.

13.1.11 SPI Send Compressed Data to Decode

SPI_SND_DEC						
Byte Sequence:	Host controller	0xC0	D0[7:0]	D1[7:0]	….	Dn[7:0]
	ISD15D00	Status Byte				
Description:	Write compressed audio data via SPI interface.					
Interrupt Generation:	OVF_ERR if RDY/BSYB violated.					

This command allows the user to send compressed audio data, in a byte formatted bit stream, down the SPI interface to the de-compressor and signal path. Before execution of command (1) a valid signal path must be set up. Valid paths are similar to a standard playback. (2) Multiple SPI_SND_DEC commands can be issued to send data to the ISD15D00. (3) To finish decoding a STOP command is sent and device will respond with a CMD_FIN interrupt. RDY/BSYB pin will handshake dataflow if device cannot accept any further data for decompression. If host cannot keep up with data rate audio output will be corrupted.

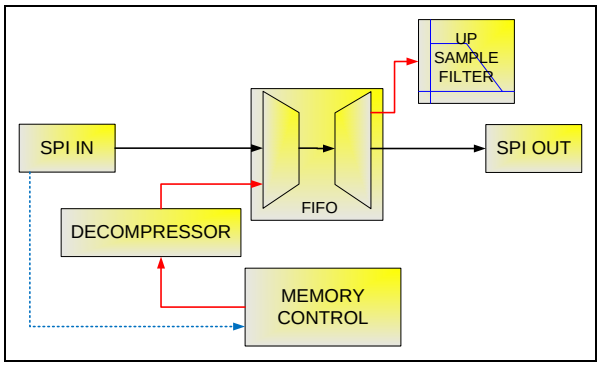


Figure 13-2 SPI Send Compressed Data to Decode

The RDY/BSYB pin will go low whenever the internal FIFO is full. If no path set up to accept audio data then RDY/BSYB pin will not return high until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated. The SPI_SND_DEC command is accepted if no current play operation is active. If command is not accepted a CMD_ERR interrupt will be generated. It is possible to perform digital memory operations between SPI_SND_DEC operations, however care must be taken to maintain the required data rate to avoid audio corruption.

13.2 DEVICE STATUS COMMANDS.

This section describes the 3 status commands that can be sent to the device.

13.2.1 Read Status

Powered up:

READ_STATUS			
Byte Sequence:	Host controller	0x40	0xXX
	ISD15D00	Status Byte	Interrupt Status Byte
Description:	Query device status.		

Powered down:

READ_STATUS			
Byte Sequence:	Host controller	0x40	0xXX
	ISD15D00	Status Byte 80h	00h
Description:	Query device status.		

This command queries the ISD15D00 device status. For details of device status see Section 12.2. If device is powered up, the two status bytes will be repeated for each two dummy bytes sent to the SPI interface. If device is powered down, only one status byte 80h shows up to the SPI interface at the same time the command is sent. This command is always accepted.

13.2.2 Read Interrupt

READ_INT				
Byte Sequence:	Host controller	0x46	0xXX	
	ISD15D00	Status Byte	Interrupt Status Byte	
Description:	Query device status and clear interrupt flags.			

This command queries the ISD15D00 device status and clears any pending interrupts. After this command the hardware interrupt line will return inactive. The INT bit of the status register along with any status error bits will return inactive.

This command is accepted whenever device is powered up.

13.2.3 Read ISD15D00 ID

READ_ID						
Byte Sequence:	Host controller	0x48	0xXX	0xXX	0xXX	0xXX
	ISD15D00	Status Byte	PART_ID	MAN_ID	MEM_TYPE	DEV_ID
Description:	Return memory ID of internal memory					

This command queries the ISD15D00 to returns four bytes to indicate the ISD15D00 family member and the manufacturer, size and type of internal memory of the device.

The four bytes returned are:

- One byte ISD15D00 Family ID, which is 0x04.
- Three bytes Flash JEDEC ID.

13.3 DIGITAL MEMORY COMMANDS.

This section describes the 5 digital data commands that can be sent to the device. Digital commands are ones that read, write or erase data directly in the flash memory through a separate interface than the audio data command interface. Digital memory commands other than erase, can occur simultaneously with audio memory commands.

13.3.1 Digital Read

DIG_READ								
Byte Sequence:	Host controller	0xA2	A[23:16]	A[15:8]	A[7:0]	0xXX	…	0xXX
	ISD15D00	Status	Status	Status	Status	D0	…	Dn
Description:	Initiates a digital read of memory from address A[23:0].							
Interrupt Generation:	ADDR_ERR if memory protected or RDY/BSYB violated. OVF_ERR if read past end of array.							

This command initiates a read of flash memory from address A[23:0]. Following the three address bytes, data can be read out of memory in a sequential manner. The RDY/BSYB pin is used to control flow of data. If RDY/BSYB pin goes low, transfer must be paused until RDY/BSYB pin returns high. The user should check RDY/BSYB pin before every byte is sent/read including the command and address bytes. As many bytes of data as required can be read, command is terminated by raising SSB high, finishing the SPI transaction. If an attempt is made to read past the end of memory, status byte will be read back.

The command will always be accepted, and RDY/BSYB pin will go low until any active digital memory command is complete. If a digital read is attempted in read protected memory, status byte will be read back and an ADDR_ERR interrupt will be generated. If a read past the end of memory is attempted an OVF_ERR interrupt will be generated. If RDY/BSYB is violated then zero data will be read back and an ADDR_ERR interrupt will be generated.

13.3.2 Digital Write

DIG_WRITE								
	Host controller	0xA0	A[23:16]	A[15:8]	A[7:0]	D0	…	Dn

Byte Sequence:	ISD15D00	Status	Status	Status	Status	Status	…	Status
Description:	Initiates a digital write to memory from address A[23:0].							
Interrupt Generation:	ADDR_ERR if memory protected or RDY/BSYB violated. OVF_ERR if write past end of array.							

This command initiates a write to flash memory from address A[23:0]. Following the three address bytes, data can be written to memory in a sequential manner. The RDY/BSYB pin is used to control flow of data. If RDY/BSYB pin goes low, transfer must be paused until RDY/BSYB pin returns high. The user should check RDY/BSYB pin before every byte is sent including the command and address bytes. As many bytes of data as required can be written, command is terminated by raising SSB high, finishing the SPI transaction.

The command will always be accepted, and RDY/BSYB pin will go low until any active digital memory command is complete. If a digital write is attempted in write protected memory, data will be ignored and an ADDR_ERR interrupt will be generated. If a write is attempted past the end of memory an OVF_ERR interrupt will be generated. If RDY/BSYB is violated then data will ignored and an ADDR_ERR interrupt will be generated. Once the SPI transaction has ended the ISD15D00 will finish the flash write operation. When this operation is complete the ISD15D00 will generate a WR_FIN interrupt. While device is actively writing to flash memory the CMD_BSY bit will be active.

13.3.3 Erase Memory

ERASE_MEM								
Byte Sequence:	Host controller	0x24	SA[23:16]	SA[15:8]	SA[7:0]	EA[23:16]	EA[15:8]	EA[7:0]
	ISD15D00	Status	Status	Status	Status	Status	Status	Status
Description:	Erases memory from sector containing SA to sector containing EA.							
Interrupt Generation:	ADDR_ERR if memory protected. CMD_ERR if device is busy. CMD_FIN when erase operation complete.							

This erases memory from the sector containing start address SA to the sector containing end address EA. The minimum erase block of internal memory is a 4kByte sector.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory is write-protected an ADDR_ERR interrupt is generated. Upon completion of erase a CMD_FIN interrupt is generated.

While the device is erasing no other commands will execute. If a PLAY is sent it is queued in the command buffer and will not execute until the erase is finished. If a DIG_RD or DIG_WR command is sent to the device, RDY/BSYB pin will hold off any data transfer until the ERASE_MEM has completed.

When ERASE_MEM is in progress, the Status bit 0 CMD_BSY goes high. Users could poll the status to see if the erasing is done.

13.3.4 Chip Erase

CHIP_ERASE			
Byte Sequence:	Host controller	0x26	0x01
	ISD15D00	Status Byte	Status Byte
Description:	Initiate a mass erase of memory.		
Interrupt Generation:	CMD_ERR if device is busy and cannot accept command. CMD_FIN when erase operation complete.		

This erases the entire contents of the internal memory.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory is mass erase protected an ADDR_ERR interrupt is generated. Upon completion of erase a CMD_FIN interrupt is generated.

While the device is erasing no other commands will execute. If a PLAY is sent it is queued in the command buffer and will not execute until the erase is finished. If a DIG_RD or DIG_WR command is sent to the device, RDY/BSYB pin will hold off any data transfer until the CHIP_ERASE has completed.

When CHIP_ERASE is in progress, the Status bit 0 CMD_BSY goes high. Users could poll the status to see if the erasing is done.

13.3.5 CHECKSUM

CHECKSUM					
Byte Sequence:	Host controller	0xF2	EA[23:16]	EA[15:8]	EA[7:0]
	ISD15D00	Status Byte	Status	Status	Status
Description:	Initiate a checksum of memory.				
Interrupt Generation:	CMD_ERR if device is busy and cannot accept command. CMD_FIN when erase operation complete.				

This initiates a 4-byte checksum calculation from the very beginning to the specified end address. The calculated checksum is stored in register 0x31[7:0] 0x32[15:8] 0x33[23:16] 0x34[31:24]. To re-calculate the checksum with a different end address, users have to set register 0x30 bit-1 to clear the registers 0x31 ~ 0x34.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory is mass erase protected an ADDR_ERR interrupt is generated. Upon completion of erase a CMD_FIN interrupt is generated.

When CHECKSUM is in progress, the Status bit 0 CMD_BSY goes high. Users could poll the status to see if the erasing is done.

13.4 DEVICE CONFIGURATION COMMANDS.

This section describes 6 commands used to configure the ISD15D00. These commands are used to:

- Set up the clocking regime of the device including clock source and setting the master sample rate.
- Configure the audio signal path.

The signal path, compression and sample rate configuration are controlled by forty-eight bytes of configuration register. These forty-eight bytes can be written individually or in a continuous sequential manner. These configuration registers are double buffered such that a new configuration can be loaded and only set active when the user desires.

13.4.1 PWR_UP – Power up

PWR_UP				
Byte Sequence:	Host controller	0x10		
	ISD15D00	Status		…
Description:	Powers up device and initiates the power up sequence.			

This command powers up the device. If device already powered up this command has no effect. If powered down, then the internal power up sequence is initiated. If the PU voice macro is present this is executed, otherwise the device defaults to power up the internal oscillator. When power up is complete the PD bit of the status register will go low and the RDY bit high. Until this event no other commands will be accepted by the ISD15D00.

A formal power-up procedure is as follows:

- Send PWR_UP command.
- Poll Status until bit-6 DBUF_RDY goes high, which means ready.
- Poll Status until bit-2 VM_BSY goes low, which means voice macro 1 finishes.

13.4.2 PWR_DN – Power Down

PWR_DN				
Byte Sequence:	Host controller	0x12		
	ISD15D00	Status		…
Description:	Powers down the device after any active commands finish			

This command powers down the device. If the device is currently executing a command the device will powers down when the command finishes. If playing or executing a voice macro, device will power down after playback is finished. The PWR_DN command will not generate an interrupt. PWR_DN has executed when PD bit of status goes high.

13.4.3 SET_CLK_CFG – Set Clock Configuration Register

SET_CLK_CFG				
Byte Sequence:	Host controller	0xB4	CFG_CLK[7:0]	
	ISD15D00	Status Byte	Status Byte	
Description:	Loads clock configuration register.			

This sets the clock configuration register. The part reconfigures the clock and PLL configuration and waits for stable clock conditions before accepting new commands. When the configuration is changed, CMD_BSY will go high until clock configuration is complete. No new commands should be sent until the device status shows device not busy. This command does not generate an interrupt.

13.4.4 RD_CLK_CFG – Read Clock Configuration Register

This reads the clock configuration register.

RD_CLK_CFG				
Byte Sequence:	Host controller	0xB6	0xXX	
	ISD15D00	Status Byte	CFG_CLK[7:0]	
Description:	Reads clock configuration register.			

13.4.5 WR_CFG_REG – Write Configuration Register

WR_CFG_REG						
Byte Sequence:	Host controller	0xB8	REG[7:0]	D0	…	Dn
	ISD15D00	STATUS0			…	
Description:	Loads configuration register CFG[REG] with D0. Data bytes 1..n can be sent to load CFG[REG+1] with D1 to CFG[REG+n] with Dn.					

This command loads configuration registers starting at the address specified. If multiple data bytes are sent, additional configuration registers are loaded. See Section 12.3 for details on configuration registers. There are forty-eight configuration registers in the ISD15D00, REG0 – REG2F.

13.4.6 RD_CFG_REG – Read Configuration Register

RD_CFG_REG						
Byte Sequence:	Host controller	0xBA	REG[7:0]	X	…	X
	ISD15D00	STATUS0		D0	…	Dn
Description:	Reads configuration register CFG[REG] and outputs to SPI as D0. Data bytes 1..n can be read sequentially from CFG[REG+1] to CFG[REG+n].					

This command reads the configuration register starting at the address specified. If multiple data bytes are sent, additional configuration registers are read.

See Section 12.3 for details on configuration registers.

14 ELECTRICAL CHARACTERISTICS

14.1 ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	CONDITION	MIN	MAX	UNITS
DC Power Supply	V_{CCD}	$V_{CCD} – V_{SSD}$	-0.3	+6.0	V
	V_{CCA}	$V_{CCA} – V_{SSA}$	-0.3	+6.0	V
	V_{CCSPK}	$V_{CCSPK} – V_{SSSPK}$	-0.3	+6.0	V
Digital Input Voltage	DV_{IN}	DV_{IN} - V_{SSD}	V_{SSD} – 0.3	V_{CCD} + 0.3	V
Analog Input Voltage	AV_{IN}	AV_{IN} - V_{SSA}	V_{SSA} – 0.3	V_{CCA} + 0.3	V
Junction Temperature	T_J	-	-40	+125	°C
Storage Temperature	T_{st}	-	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

14.2 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Digital Supply voltage (V_{CCD}) [1]	+2.7V to +5.5V
Digital Ground voltage (V_{SSD}) [2]	0V
Analog Supply voltage (V_{CCA}) [3]	+2.7V to +5.5V
Analog Ground voltage (V_{SSA}) [2]	0V
Speaker Supply voltage (V_{CCSPK}) [3]	+2.7V to +5.5V
Speaker Ground voltage (V_{SSSPK}) [2]	0V
Flash Source Supply voltage (V_{CCFS}) [4] – to regulate V_{CCF}	+2.7V to +5.5V
Flash Source Supply voltage (V_{CCFS}) [4] – tied to V_{CCF}	+2.25V to +3.6V
Flash Supply voltage - (V_{CCF}) [4] – regulated from V_{CCFS}	+2.4V to +3.0V
Flash Supply voltage - (V_{CCF}) [4] – tied to V_{CCFS}	+2.25V to +3.6V

NOTES:

[1] V_{CCD} 2.7 ~ 5.5V; No restrictions with respect to V_{CCA} and V_{CCSPK}.

[2] $V_{SSD} = V_{SSA} = V_{SSSPK}$

[3] In Class-AB mode: V_{CCSPK} must equal V_{CCA}. Otherwise: $V_{CCSPK} \geq V_{CCA}$.

[4] If V_{CCFS} is guaranteed to be below 3.6V (or upper flash supply limit), then V_{CCF} should be tied to V_{CCFS}.

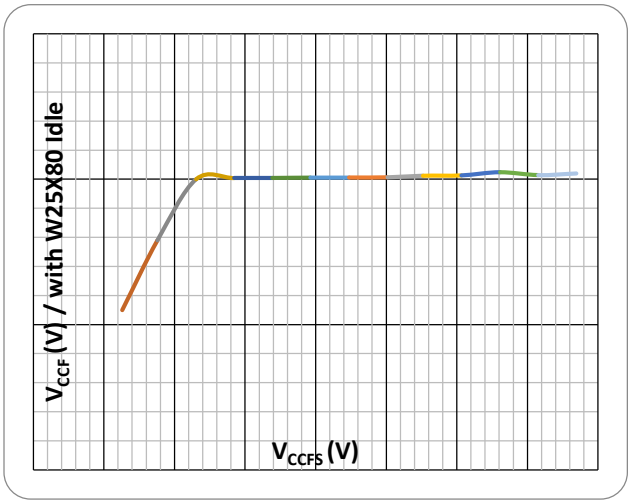


Figure 14-1 V_{CCF} vs. V_{CCFS} – V_{CCF} is regulated internally from V_{CCFS}[4]

14.3 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Digital Supply Voltage	V_{CCD}	2.7		5.5	V	
Analog Supply Voltage	V_{CCA}	2.7		5.5	V	
Speaker Supply Voltage	V_{CCSPK}	2.7		5.5	V	
Flash Source Supply Voltage	V_{CCFS}	2.7		5.5	V	to regulate V_{CCF}
		2.25		3.6		tied to V_{CCF}
Flash Supply Voltage (refer to Figure 14-1)	V_{CCF}		V_{CCFS} -0.3		V	regulated from V_{CCFS} V_{CCFS} = 2.7 ~ 3.3V
			3.0			regulated from V_{CCFS} V_{CCFS} = 3.3 ~ 5.5V
		2.25		3.6		tied to V_{CCFS}
Input Low Voltage	V_{IL}	V_{SSD}-0.3		0.3xV_{CCD}	V	
Input High Voltage	V_{IH}	0.7xV_{CCD}		V_{CCD}	V	
Output Low Voltage	V_{OL}	V_{SSD}-0.3		0.3xV_{CCD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{CCD}		V_{CCD}	V	I_{OH} = -1mA
INTB Output Low Voltage	V_{OH1}			0.4	V	
Playback Current	$I_{DD\_Playback}$		10	30	mA	No load
Standby Current	I_{SB}		1	10	µA	V_{CCD} = 3.0v
Input Leakage Current	I_{IL}	-1		+1	µA	Force V_{CCD}

Notes: [1] Conditions V_{CCD}=V_{CCA}=V_{CCSPK}=V_{CCFS}=3V, T_A=25°C unless otherwise stated

14.4 AC PARAMETER

14.4.1 Internal Oscillator

Parameter	Symbol	Min	Typ	Max	Units	CONDITIONS
Internal oscillator with internal reference	F_{INT}	-1%	2.048 MHz	+1%	MHz	V_{CCD} = 3.3V. At room temperature.
Internal oscillator with external reference	F_{EXT}	-2%	2.048 MHz	+2%	MHz	With ±1% precision resistor, 80kohm. V_{CCD} = 3.3V. At room temperature.

14.4.2 Input

AUX-IN:

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK}, MCLK = 16.384MHz, T_A = +25°C, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Auxiliary Analog Inputs (AUXIN)						
Full scale input signal [1]		Gain = 0dB		1.0 0		Vrms dBV
AUX Programmable gain			0		9	dB
AUX programmable gain step size		Guaranteed Monotonic		3		dB
Input resistance		Aux direct-to-out path, only Input gain = +9.0dB Input gain = +6.0dB Input gain = +3.0dB Input gain = 0dB		 21 27 33 40		 kΩ kΩ kΩ kΩ
Aux-in Gain Accuracy	$A_{AUX(GA)}$		-0.5dB		+0.5dB	dB

Note: V_{CCA} = V_{CCSPK}=3.3V or V_{CCA} = V_{CCSPK}=5.0V

14.4.3 Output

AUX-OUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		85		dB
Total harmonic distortion [2]	THD+N	R_L = 5kΩ; full-scale signal A-weighted		-80		dB

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		80		dB
Total harmonic distortion [2]	THD+N	R_L = 5kΩ; full-scale signal A-weighted		-77		dB

PWM OUTPUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Signal-to-noise ratio[3]	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion [2]	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load		85		%

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Signal-to-noise ratio[3]	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion [2]	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load		80		%

CLASS-AB BTL OUTPUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Full scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		90		dB
Total harmonic distortion [2]	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load		50		%

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Full scale output [1s]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		84		dB
Total harmonic distortion [2]	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load		50		%

Notes:

1. Full Scale is relative to the magnitude of VCCA and can be calculated as FS = VCCA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. SNR measured with a -100dbFS signal at input.

SPEAKER OUTPUT POWER

Conditions: V_{CCD} = 3.3V, 16KHz sample rate, 12bit PCM, T_A = +25°C, 1kHz signal

Parameter	Symbol	mode	Min	Typ.	Max	Unit	Comment/Condition[1]
Output Power	P_{OUT_SPK}	Class-D PWM		260		mW	@ 3.3V, Load 8Ω, 1% THD
				640		mW	@ 5.0V, Load 8Ω, 1% THD
				770		mW	@ 5.5V, Load 8Ω, 1% THD
				335		mW	@ 3.3V, Load 4Ω, 10% THD
				840		mW	@ 5.0V, Load 4Ω, 10% THD
				1.00		W	@ 5.5V, Load 4Ω, 10% THD
		Class-AB BTL		255		mW	@ 3.3V, Load 8Ω, 0.3% THD
				610		mW	@ 5.0V, Load 8Ω, 0.3% THD
				750		mW	@ 5.5V, Load 8Ω, 0.3% THD
				330		mW	@ 3.3V, Load 4Ω, 10% THD
				800		mW	@ 5.0V, Load 4Ω, 10% THD
				950		mW	@ 5.5V, Load 4Ω, 10% THD

Note:

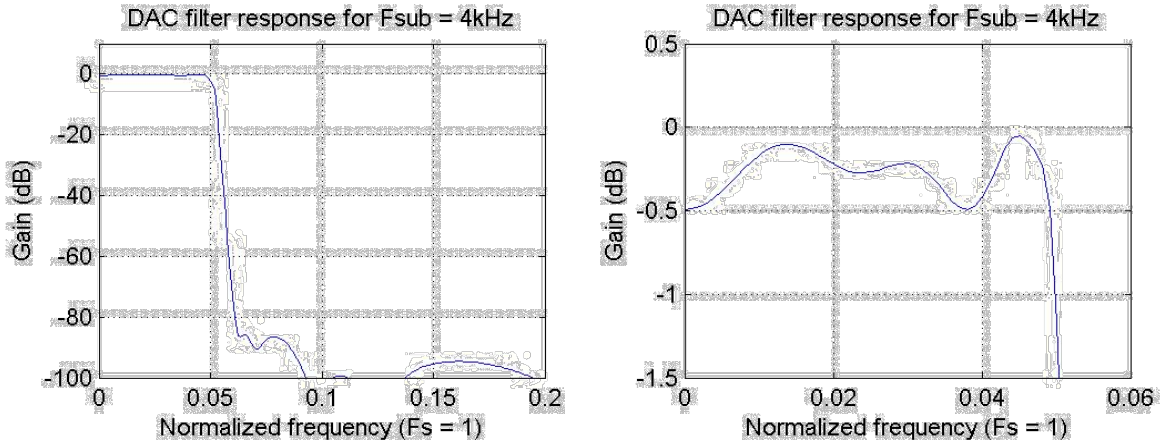
1. VCCA=VCCSPK.

14.4.4 DAC Frequency Responses

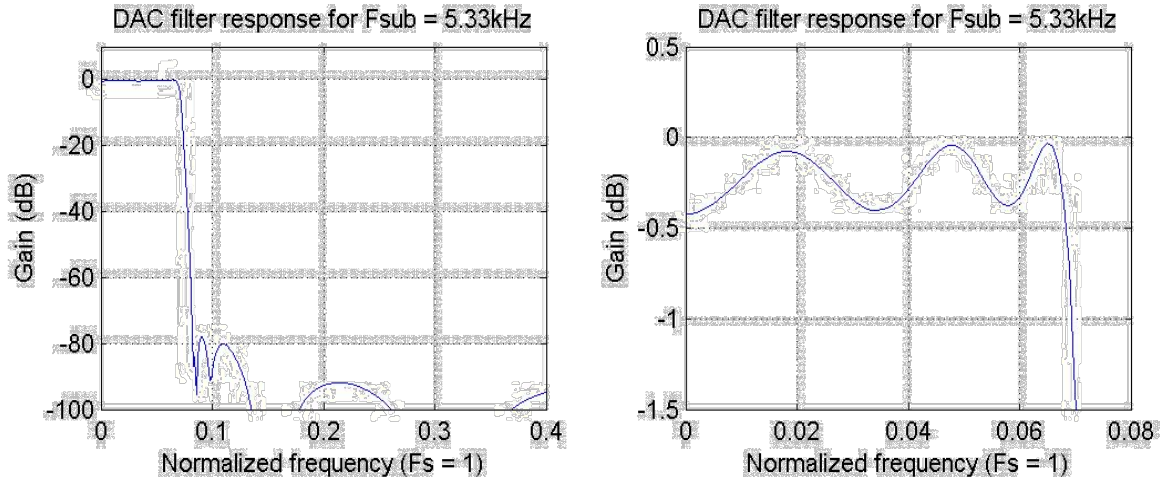
The following graphs show the frequency responses of the signal path for analog or digital audio inputs. The data presented is for a master sample rate Fs=32kHz. For other values of Fs, Fsub scales accordingly.

There is a built-in high-pass filter with cutoff 200Hz following the ADC filter. The graphs below show a combined effect.

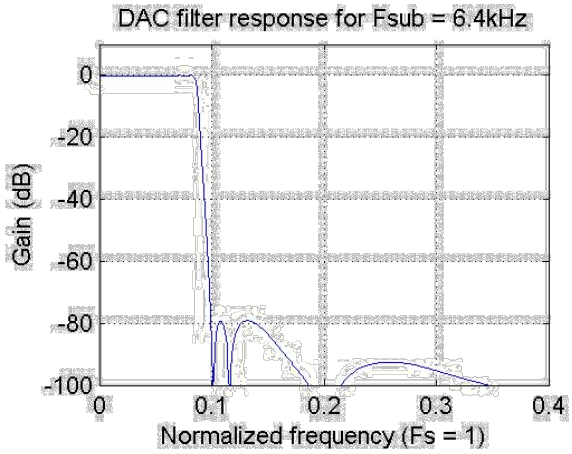
Playback Frequency Response Fs = 32kHz, Fsub = 4kHz

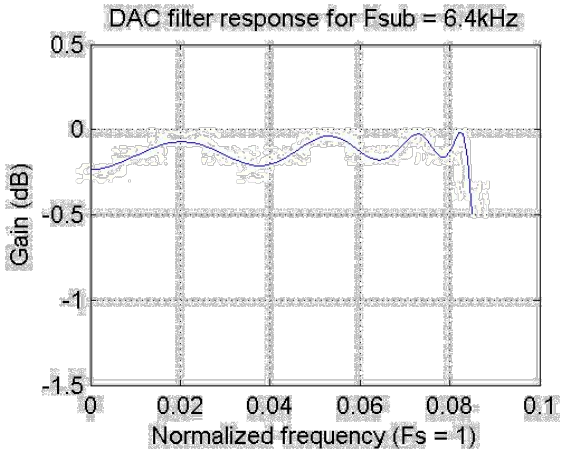


Playback Frequency Response Fs = 32kHz, Fsub = 5.33kHz

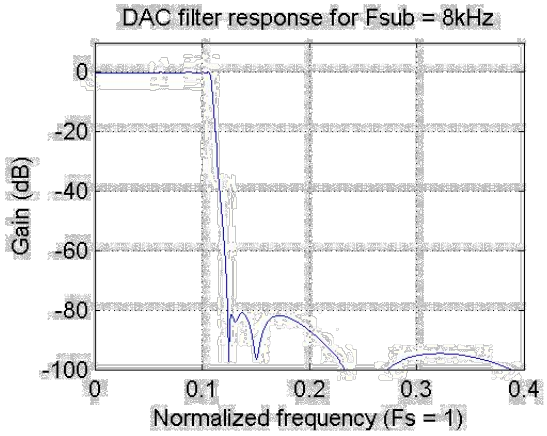


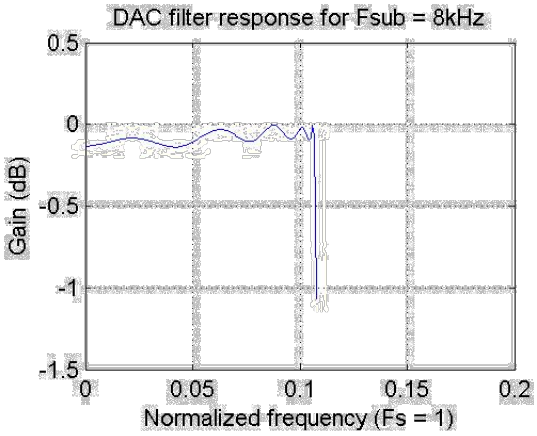
Playback Frequency Response Fs = 32kHz, Fsub = 6.4kHz



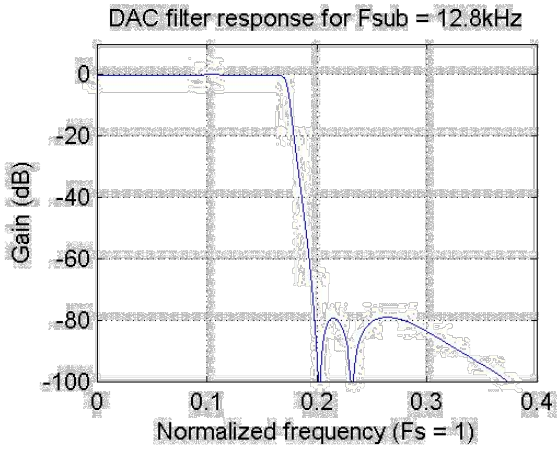


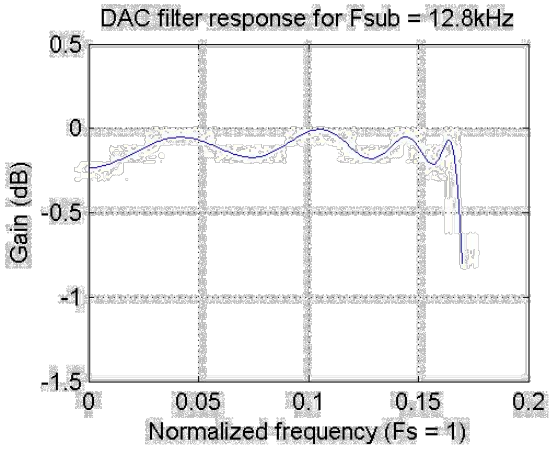
Playback Frequency Response Fs = 32kHz, Fsub = 8kHz



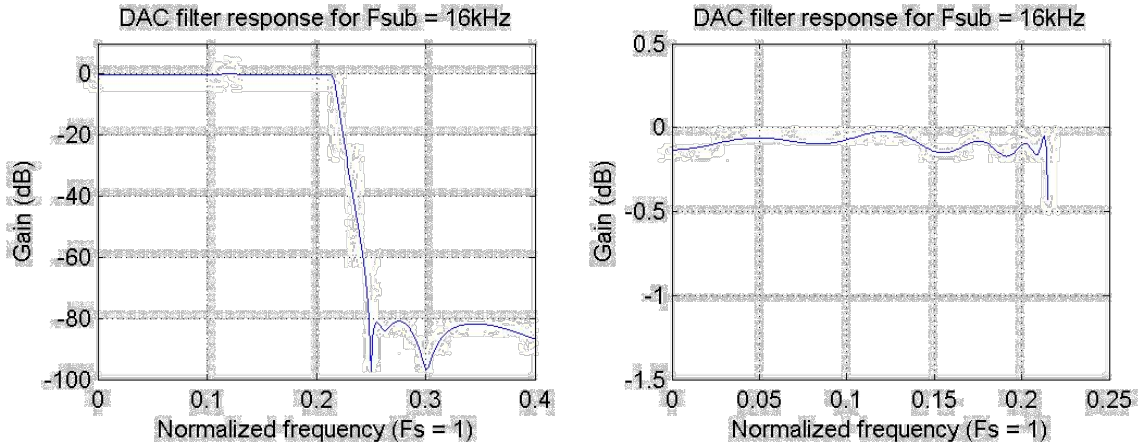


Playback Frequency Response Fs = 32kHz, Fsub = 12.8kHz

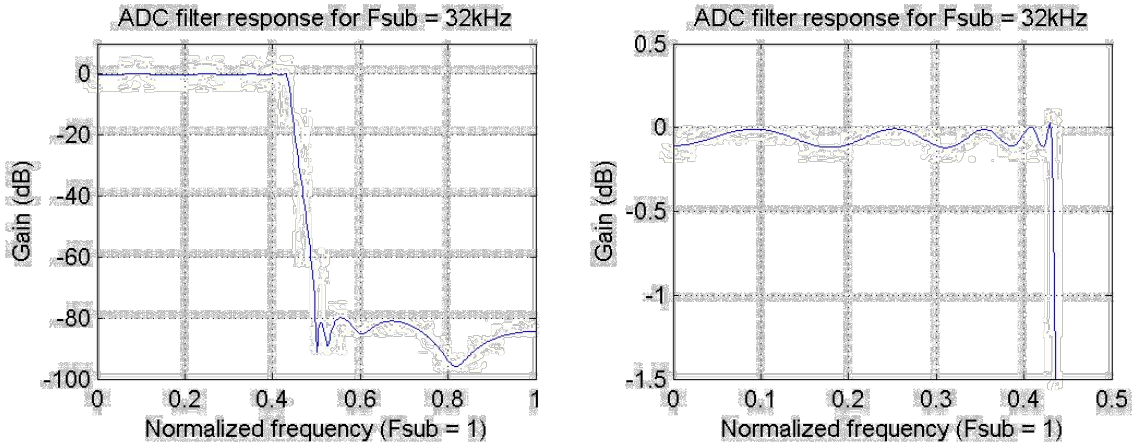




Playback Frequency Response Fs = 32kHz, Fsub = 16kHz



Playback Frequency Response Fs = 32kHz, Fsub = 32kHz



14.4.5 SPI Timing

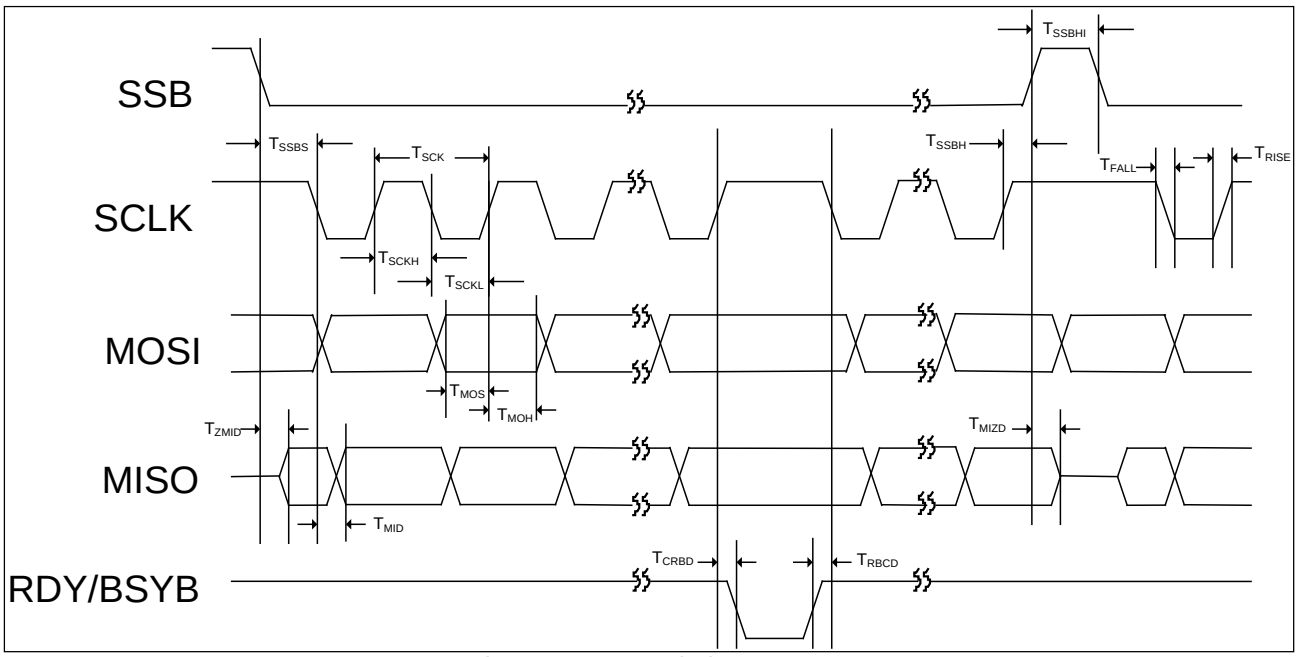


Figure 14-2 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

14.4.6 I²S Timing

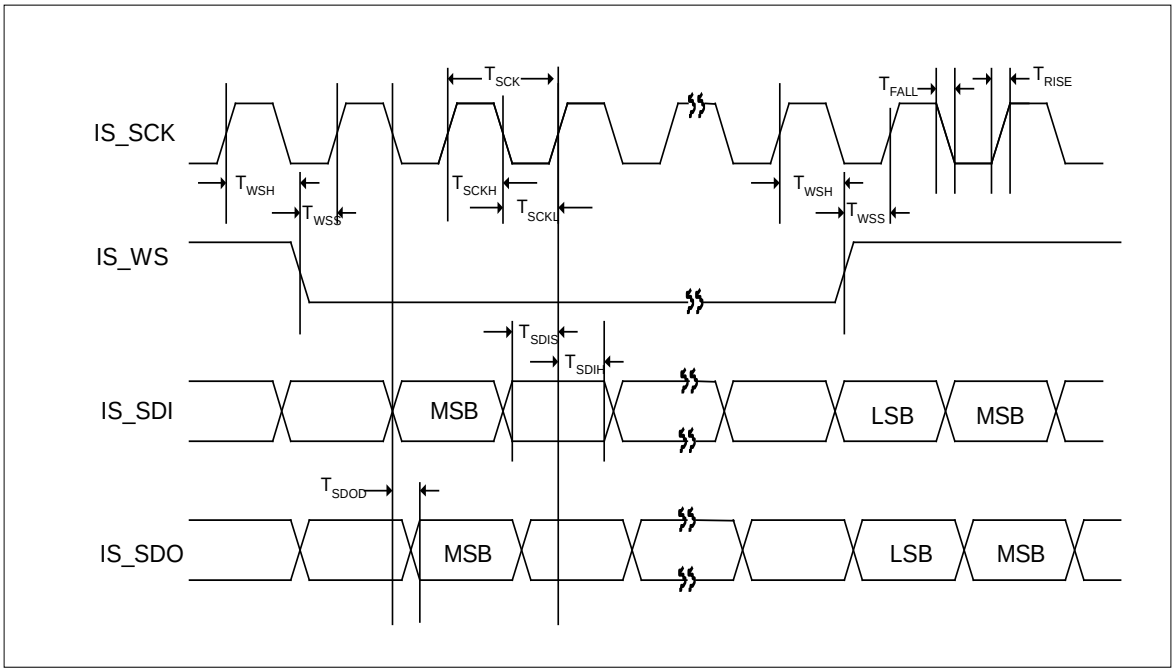


Figure 14-3 I²S Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	IS_SCK Cycle Time	60	---	---	ns
T_{SCKH}	IS_SCK High Pulse Width	25	---	---	ns
T_{SCKL}	IS_SCK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{WSS}	WS to IS_SCK Rising Edge Setup Time	20	---	---	ns
T_{WSH}	IS_SCK Rising Edge to IS_WS Hold Time	20	---	---	ns
T_{SDIS}	IS_SDI to IS_SCK Rising Edge Setup Time	15	---	---	ns
T_{SDIH}	IS_SCK Rising Edge to IS_SDI Hold Time	15	---	---	ns
T_{SDOD}	Delay Time from IS_SCLK Falling Edge to IS_SDO	---	---	12	ns

15 APPLICATION DIAGRAM

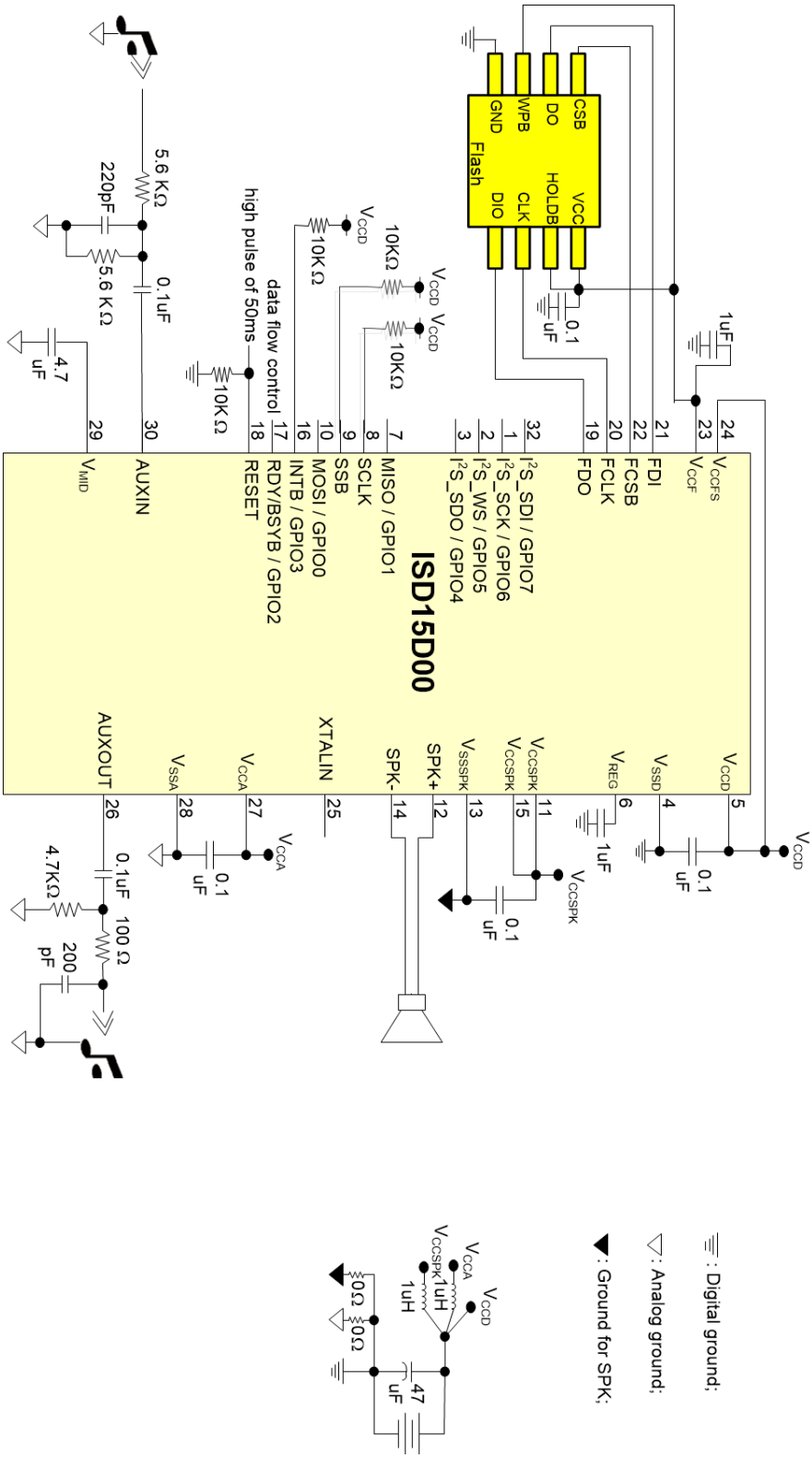


Figure 15-1 ISD15D00 Application Diagram – V_{CCF} is regulated internally from V_{CCFS}

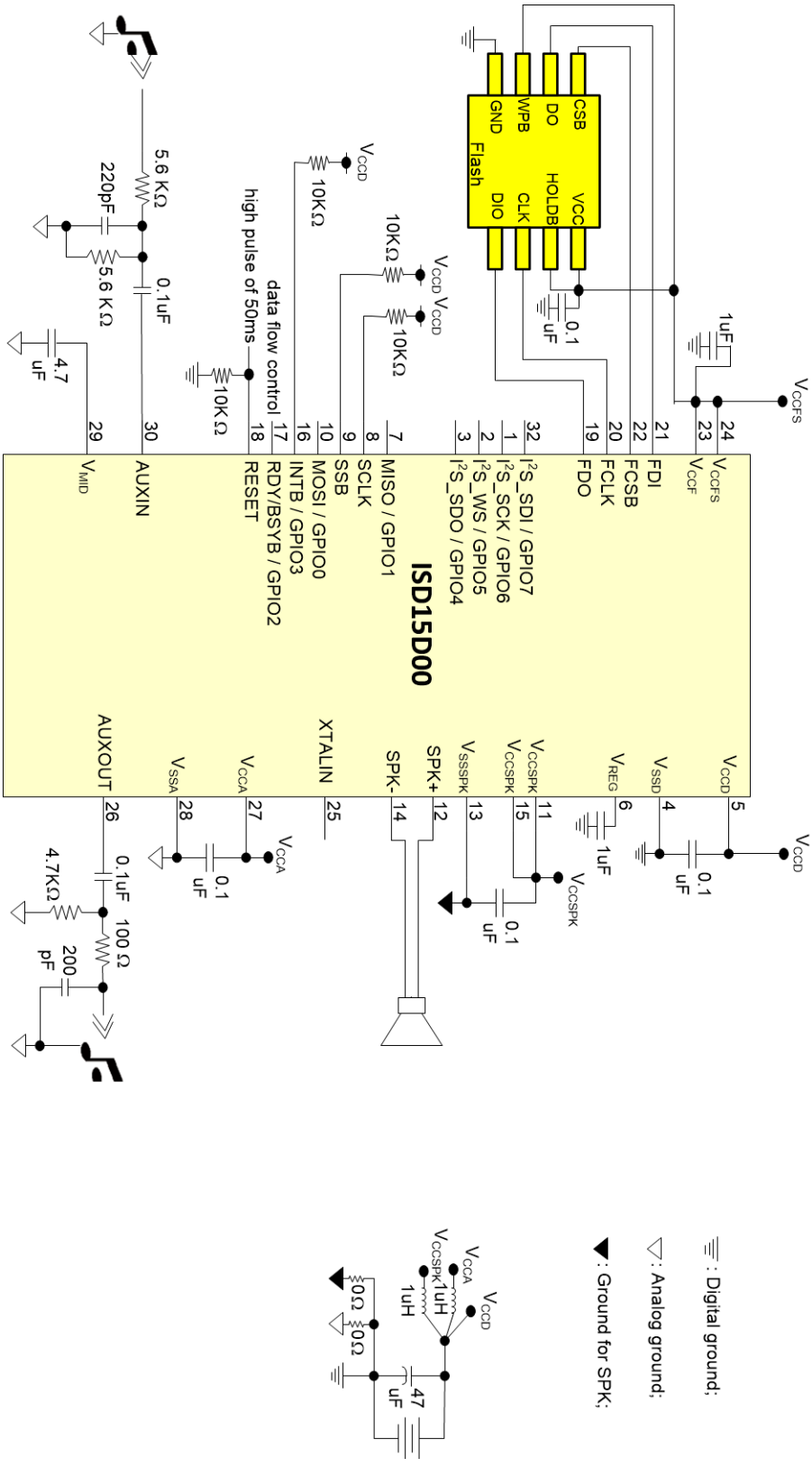
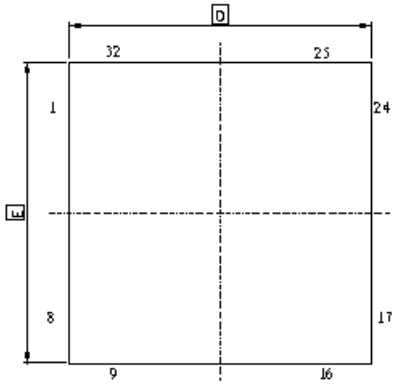


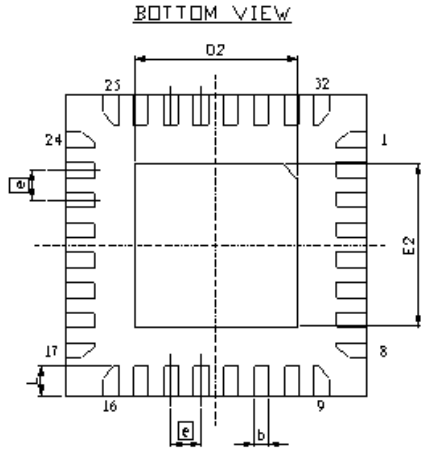
Figure 15-2 ISD15D00 Application Diagram – V_{CCF} is tied to V_{CCFS}

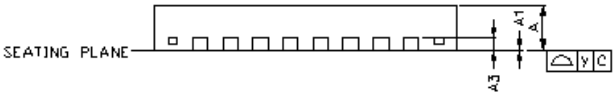
The above application examples are for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

16 PACKAGE SPECIFICATION

16.1 32 LEAD QFN (5X5 MM^2, THICKNESS 0.8MM ,PITCH 0.5 MM)

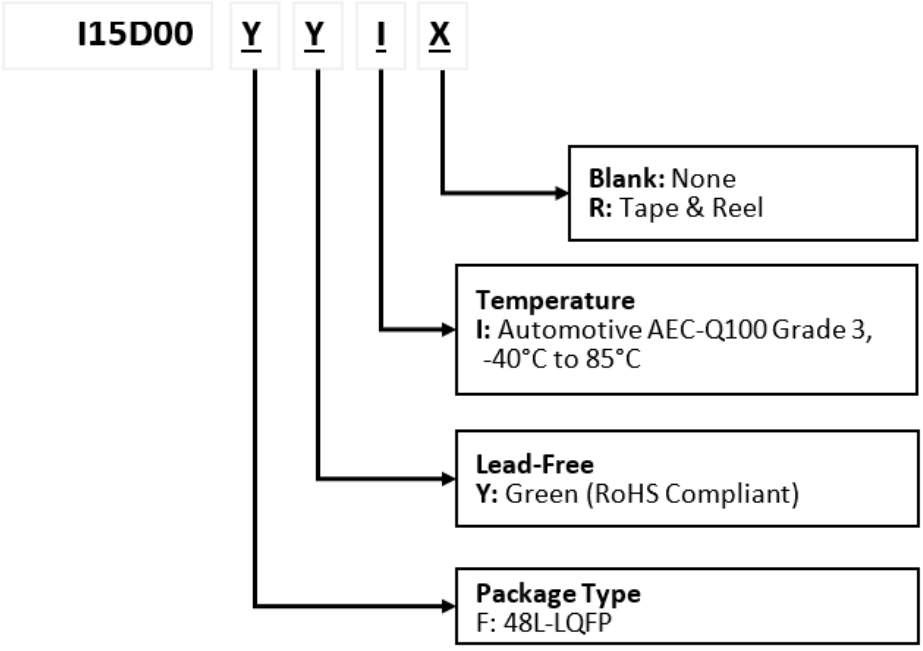






SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		5.00 BSC			0.197 BSC	
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E		5.00 BSC			0.197 BSC	
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e		0.50 BSC			0.0197 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
y		0.10			0.0039	

17 ORDERING INFORMATION



Part Number	Duration	Package	Temperature	Notes
I15D00YYI	Ext. Flash 128Mbit / 64 Minutes	48L-LQFP	Automotive AEC-Q100 Grade 3 -40°C to 85°C	
I15D00YYIR	Ext. Flash 128Mbit / 64 Minutes	48L-LQFP, Tape & Reel	Automotive AEC-Q100 Grade 3 -40°C to 85°C	

18 REVISION HISTORY

Version	Date	Description
1.0	Aug 23, 2013	Add internal oscillator characteristics.
1.1	Jun 13, 2014	Update current consumption characteristic data
1.2	Jan 20,2017	Add Absolute Maximum Ratings. Add Talarm temperature threshold typical value. Application diagram update. MOSI pin description update.
1.3	Mar 27, 2020	Update Document Format
1.4	May 21, 2021	Update Package Information
1.5	May 24, 2021	Update Ordering info part number
1.6	Jun 15, 2021	Update Ordering Information Update output power Remove buzzer description

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.