ISD ChipCorder®
ISD15C00 Series
Design Guide

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The ISD15C00 is a multi-message ChipCorder® featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The message management feature is designed to make message recording simple and address-free as well as make code development easier for playback-only applications. The ISD15C00 utilizes winbond's 25X and 25Q series flash memory to provide non-volatile audio record/playback for a two-chip solution. Unlike other ChipCorder series, the ISD15C00 provides an I²S digital audio interface, faster digital recording, higher sampling frequency, and a signal path with SNR equivalent to 12bit resolution.

The ISD15C00 can take digital audio data via I²S or SPI interface. When I²S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD15C00 supported sample rates.

The ISD15C00 has built-in analog audio inputs, analog audio line driver, and speaker driver output. The two analog audio inputs to the device are: (1) AUXIN has a fixed gain configured by SPI command, and (2) ANAIN/ANAOUT has a fixed gain amplifier with the gain set by two external resistors. ANAIN/ANAOUT can also be used as a microphone differential input (ANAIN/ANAOUT becomes MIC+/MIC-) in conjunction with an automatic gain control (AGC) circuit configured by SPI command. Analog outputs are available in three forms: (1) AUXOUT is a single-ended voltage output; (2) AUDOUT can be configured as either a single-ended voltage output or a single-ended current output; (3) BTL (bridge-tied-load) is a differential voltage output.

2 FEATURES

- External Memory: support winbond's 25X and 25Q SpiFlash.
  - The addressing ability of ISD15C00 is up to 128Mbit[1], which is 64-minute recording time based on 8kHz/4bit ADPCM.
- Fast Digital Programming
  - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Message Management
  - Perform address-free recording: The ISD15C00 allocates memory for new recording requests and upon completion, returns a start address to the host via SPI interface
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences and message recordings.
- Sample Rate
  - Seven record and playback sampling frequencies are available for a given master sample rate. For example, the record and playback sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate.
  - For I²S operation, 32, 44.1 and 48kHz master sample rates are available with record and playback sampling frequencies scaling accordingly.
- Compression Algorithms
  - For recording
    - ADPCM: 2, 3, 4 or 5 bits per sample
    - µ-Law: 6, 7 or 8 bits per sample
    - Differential µ-Law: 6, 7 or 8 bits per sample
    - PCM: 8, 10 or 12 bits per sample. Each sampled value is stored as a code, offering no compression but preserving maximum resolution
  - For Pre-Recorded Voice Prompts
    - µ-Law: 6, 7 or 8 bits per sample
    - Differential µ-Law: 6, 7 or 8 bits per sample

[1] Note: For details please refer to Section 8.

        - PCM: 8, 10 or 12 bits per sample
        - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
        - Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
    - Internal oscillator with internal reference: 2.048 MHz with ±10% deviation
    - Internal oscillator with external resistor: 2.048 MHz with ±5% deviation when Rosc is 80k-ohm
    - External crystal or clock input
    - I^2S bit clock input
    - Crystals and resonators support standard audio sampling rates of 2.048, 4.096, 8.192, 12.288 and11.2896MHz
- Input
    - AUXIN: Analog input with 2-bit gain control configured by SPI command
    - ANAIN/ANAOUT:
        - Analog input with the gain set by two external resistors from ANAOUT to ANAIN, or
        - Microphone differential input (ANAIN/ANAOUT becomes MIC+/MIC-)
    - Digital AGC:
        - Automatic gain control of digitized data from the analog input
- Output
    - PWM: Class D speaker driver which can deliver typical output power:
        - 8Ω load: 350mW @3.3v, 420mW @3.6v 8Ω load.
        - 4Ω load: 520mW @3.3v, 620mW @3.6v 8Ω load.
    - AUDOUT: configurable as a current or voltage single-ended line driver
    - AUXOUT: a single-ended voltage output
    - BTL: differential voltage output which can deliver typical output power:
        - 63mW for 8Ω load, 115mW for 4Ω load.
- I/O
    - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
    - I^2S interface: I^2S_CLK, I^2S_WS, I^2S_SDI, I^2S_SDO for digital audio data
    - 8 GPIO pins (4 of the 8 GPIO pins share with I^2S).
- Three 8-bit Volume Control set by SPI command for flexible mixing
    - VOLA: volume control for the digital audio data from I^2S or analog inputs
    - VOLB: volume control for the digital audio data from decompression block or SPI
    - VOLC: master volume control for PWM, AUDOUT, AUXOUT and I^2S outputs
- Operating Voltage: 2.7-3.6V
- Standby Current: 1uA typical
- Package: Green 48L-LQFP
- Automotive grade:
    - AEC-Q100 grade 3 operating temperature range -40ºC to 85ºC
    - Tested to a high reliability standard [2]

[2] Contact Nuvoton sale representatives for details.

3 DBLOCK DIAGRAM

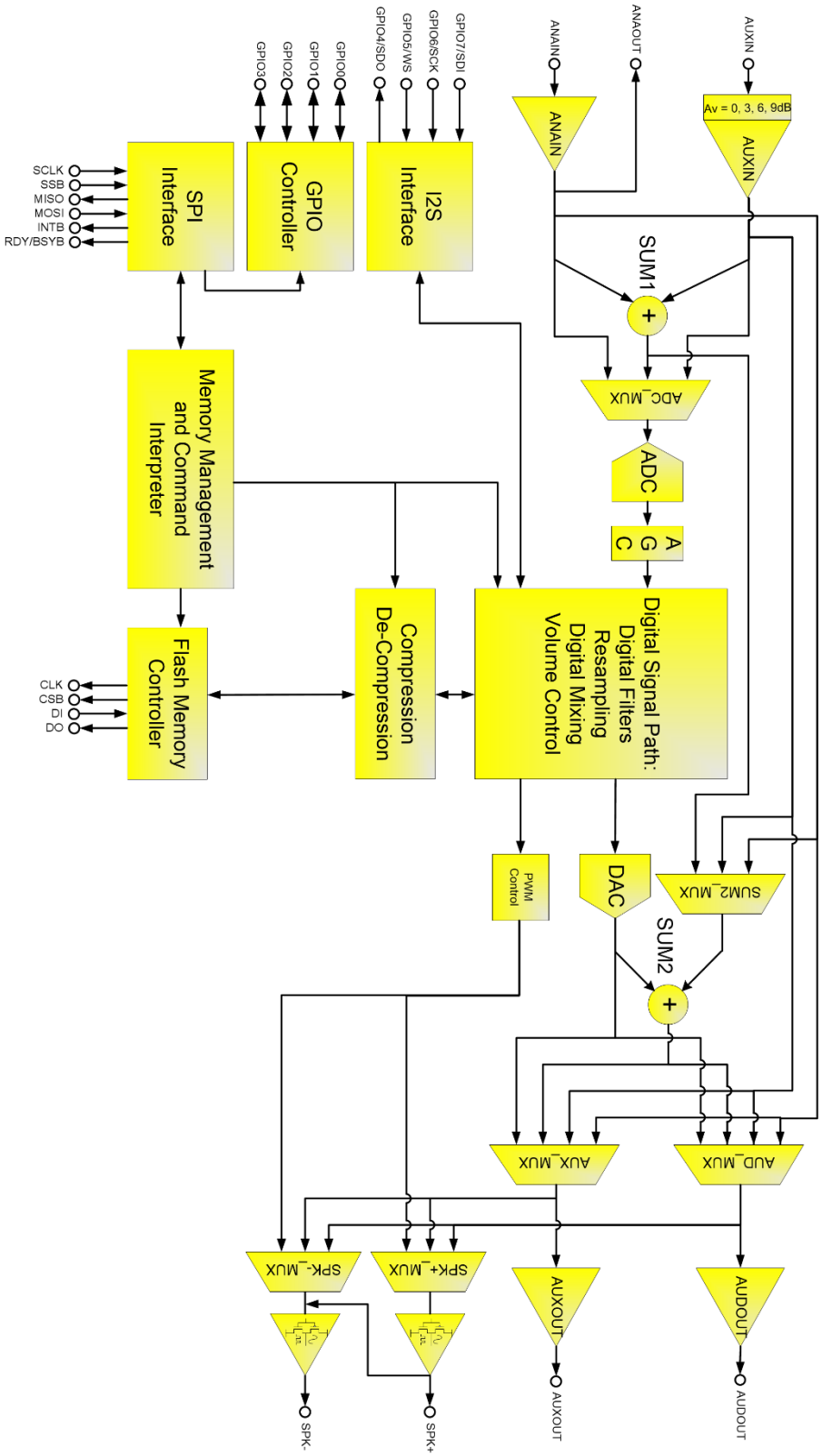


Figure 3-1 ISD15C00 Block Diagram, ANAIN Selected

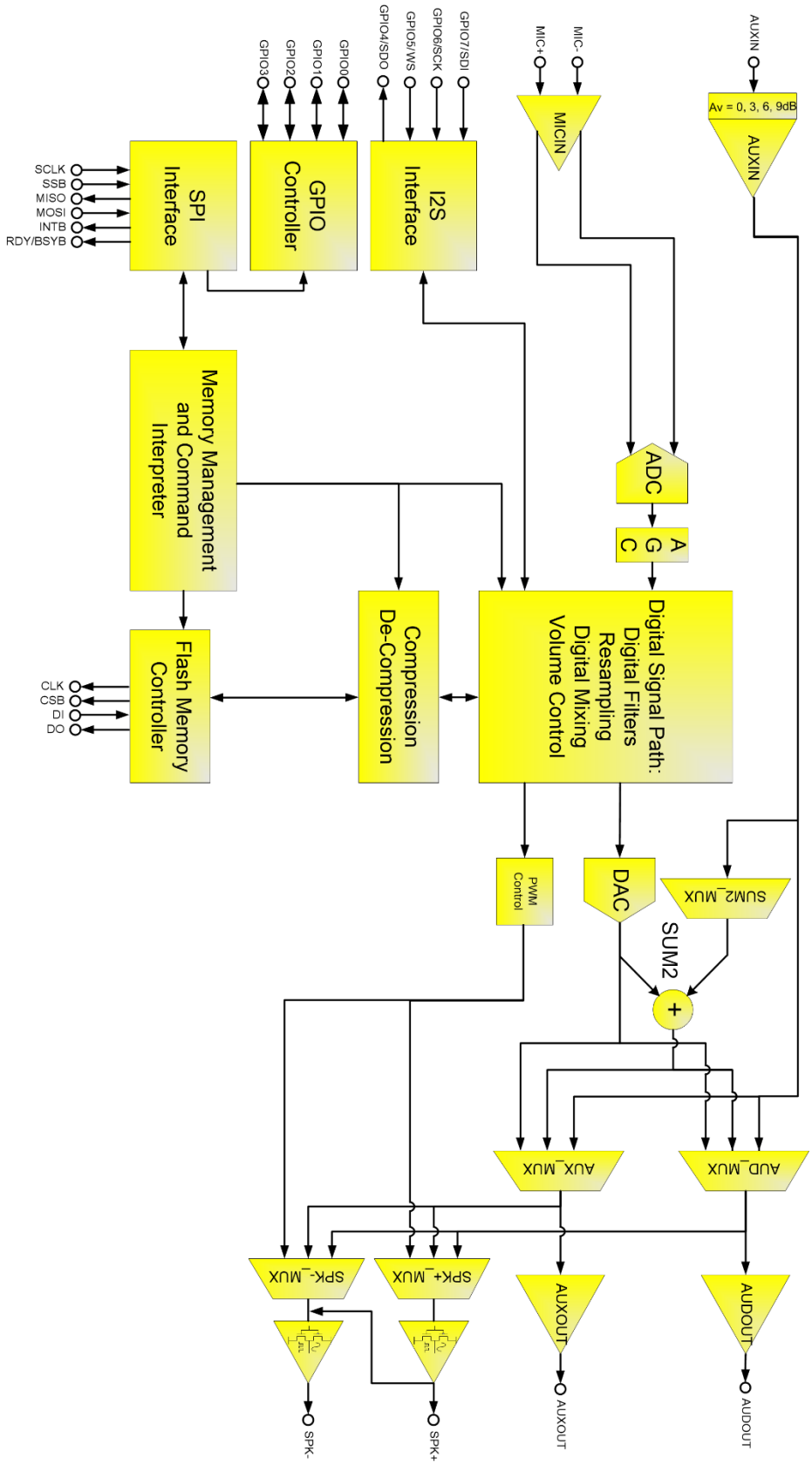


Figure 3-2 ISD15C00 Block Diagram, MICIN Selected

4 PINOUT CONFIGURATION

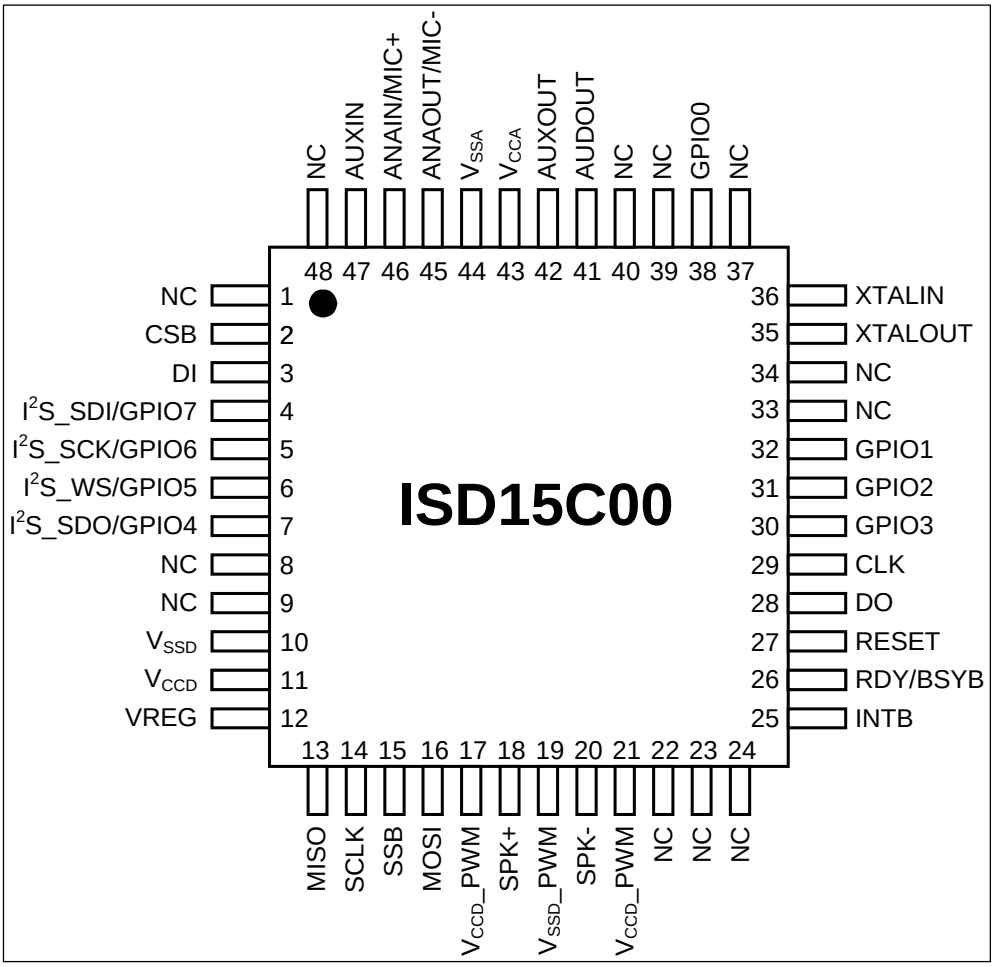


Figure 4-1 ISD15C00 48-Lead LQFP Pin Configuration.

5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	NC		This pin should be left unconnected.
2	CSB	O	Chip Select Bar of the external serial flash interface.
3	DI	I	Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory.
4	I^2S_SDI/ GPIO7	I	Serial Data Input of the I^2S interface (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
5	I^2S_SCK/ GPIO6	I/O	Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I^2S is not used (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
6	I^2S_WS/ GPIO5	I/O	Word Select (WS) input in slave mode or WS output in master mode (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
7	I^2S_SDO/ GPIO4	O	Serial Data Output of the I^2S Interface (If I2S is not used, this pin should be left unconnected). Or, can be configured as a GPIO pin.
8	NC		This pin should be left unconnected.
9	NC		This pin should be left unconnected.
10	V_{SSD}	I	Digital Ground.
11	V_{CCD}	I	Digital power supply.
12	VREG	O	A 1.8V regulator to supply the internal logic. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability.
13	MISO	O	Master-In-Slave-Out. Serial output from the ISD15C00 to the host. This pin is in tri-state when SSB=1.
14	SCLK	I	Serial Clock input to the ISD15C00 from the host.
15	SSB	I	Slave Select input to the ISD15C00 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
16	MOSI	I	Master-Out-Slave-In. Serial input to the ISD15C00 from the host.
17	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
18	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker. During power down this pin is in tri-state. Or, can be configured as BTL which, together with SPK- pin, provide a differential voltage output. Or, can independently switch to AUDOUT or AUXOUT.
19	V_{SSD}_PWM	I	Digital Ground for the PWM Driver.
20	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker. During power down this pin is tri-state.

Pin Number	Pin Name	I/O	Function
			Or, can be configured as BTL which, together with SPK+ pin, provide a differential voltage output. Or, can independently switch to AUDOUT or AUXOUT.
21	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
22	NC		This pin should be left unconnected.
23	NC		This pin should be left unconnected.
24	NC		This pin should be left unconnected.
25	INTB	O	Active low interrupt request pin. This pin is an open-drain output.
26	RDY/BSYB	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD15C00 is ready to accept new SPI commands or data.
27	RESET	I	Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)
28	DO	O	Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash.
29	CLK	O	Serial data CLK of the external serial flash interface.
30	GPIO3	I/O	GPIO
31	GPIO2	I/O	GPIO
32	GPIO1	I/O	GPIO
33	NC		This pin should be left unconnected.
34	NC		This pin should be left unconnected.
35	XTALOUT	O	Crystal interface output pin.
36	XTALIN	I	The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected.
37	NC		This pin should be left unconnected.
38	GPIO0	I/O	GPIO
39	NC		This pin should be left unconnected.
40	NC		This pin should be left unconnected.
41	AUDOUT	O	Audio Out. This pin can be either a voltage output or a current output configured by the internal registers via SPI command. If AUDOUT is not used, this pin should be left unconnected.
42	AUXOUT	O	Aux Out. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected.
43	V_{CCA}	I	Analog power supply pin.
44	V_{SSA}	I	Analog ground pin.

Pin Number	Pin Name	I/O	Function
45	ANAOUT/ MIC-	O	Variable gain analog output with the gain set by feedback resistance to ANAIN. Or, can be configured as MIC- which, together with MIC+, provides a microphone differential input. If ANAIN/ANAOUT is not used, this pin should be left unconnected.
46	ANAIN/ MIC+	I	Variable gain analog input. Or, can be configured as MIC+ which, together with MIC-, provides a microphone differential input. If ANAIN/ANAOUT is not used, this pin should be left unconnected.
47	AUXIN	I	Auxiliary input with the gain set by SPI command If AUXIN is not used, this pin should be left unconnected.
48	NC		This pin should be left unconnected.

6 SPI INTERFACE

This is a standard four-wire interface used for communication between ISD15C00 and the host. It consists of an active low slave-select (SSB), a serial clock (SCLK), a data input (Master Out Slave In - MOSI), and a data output (Master In Slave Out - MISO). In addition, for some transactions requiring data flow control, a RDY/BSYB signal (pin) is available.

The ISD15C00 supports SPI mode 3: (1) SCLK must be high when SPI bus is inactive, and (2) data is sampled at SCLK rising edge. A SPI transaction begins on the falling edge of SSB and its waveform is illustrated below:

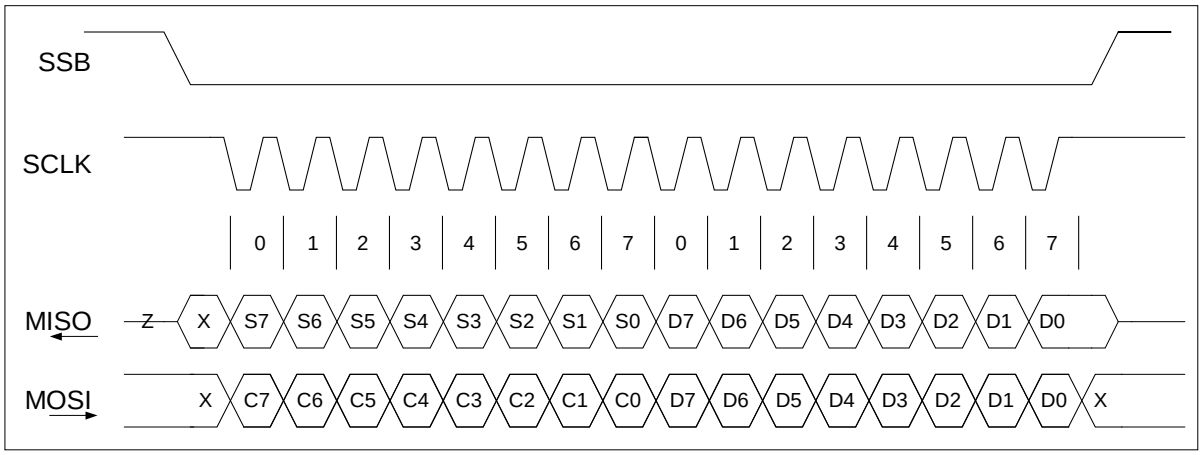


Figure 6-1 SPI Data Transaction.

A transaction begins with sending a command byte (C7-C0) with the most significant bit (MSB – C7) sent in first. During the byte transmission, the status (S7-S0) of the device is sent out via the MISO pin. After the byte transmission, depending upon the command sent, one or more bytes of data will be sent via the MISO pin.

RDY/BSYB pin is used to handshake data into or out of the device. Upon completion of a byte transmission, RDY/BSYB pin could change its state after the rising edge of the SCLK if the built-in 32-byte data buffer is either full or empty. At this point, SCLK must remain high until RDY/BSYB pin returns to high, indicating that the ISD15C00 is ready for the next data transmission. See below for timing diagram.

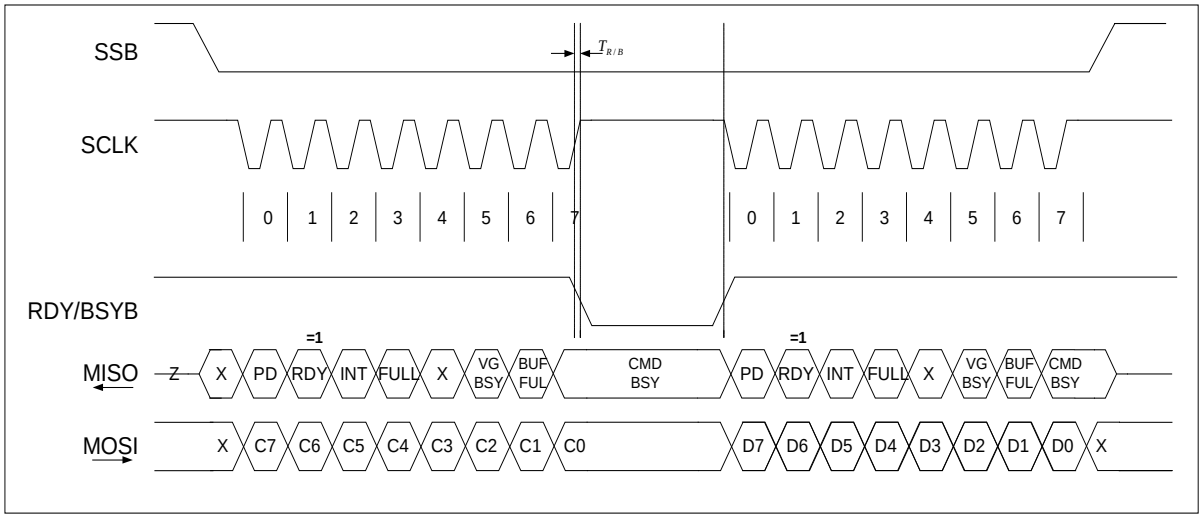


Figure 6-2 R/B Timing for SPI Writing Transactions.

If the SCLK does not remain high, RDY bit of the status register will be set to zero and be reported via the MISO pin so the host can take the necessary actions (i.e., terminate SPI transmission and re-transmit the data when the RDY/BSYB pin returns to high).

For commands (i.e., DIG_READ, SPI_PCM_READ and SPI_RCV_ENC) that read data from ISD15C00, MISO is used to read the data; therefore, the host must monitor the status via the RDY/BSYB pin and take the necessary actions.

The INT pin will go low to indicate (1) data overrun/overflow when sending data to the ISD15C00; or (2) invalid data from ISD15C00. See Figure 6-3 for the timing diagram.

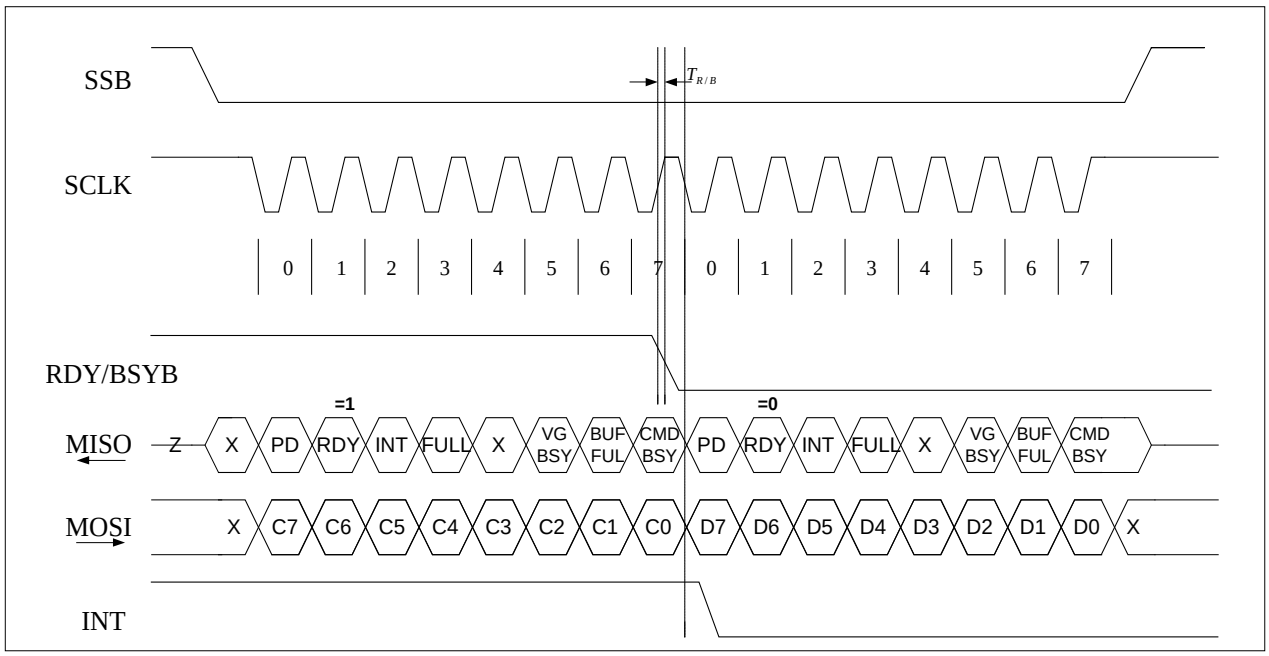


Figure 6-3 SPI Transaction Ignoring RDY/BSYB

7 ANALOG AND DIGITAL SIGNAL PATH

7.1 ANALOG SIGNAL PATH

Analog signal path provides a configurable set of two analog inputs and three analog outputs along with multiplexing and summation blocks to route signals between analog blocks and the digital signal path.

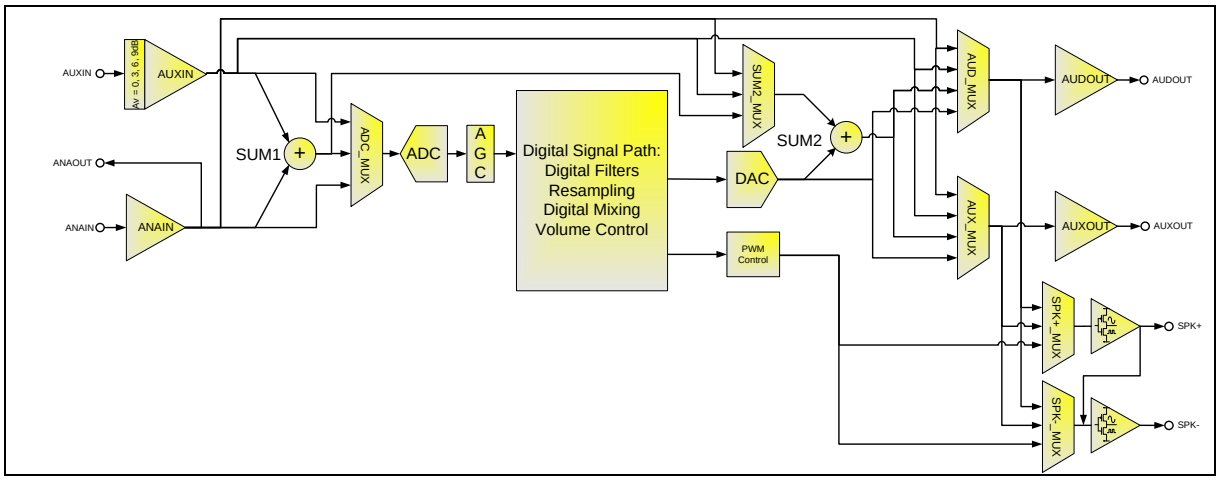


Figure 7-1 Analog Signal Path, ANAIN Selected

Analog inputs consist of variable gain input amplifiers:

- AUXIN can be configured by SPI command
- ANAIN is determined by a selection of external resistors. ANAIN can also be configured as MICIN (ANAIN/ANAOUT becomes MIC+/MIC-), which provides a microphone differential input.

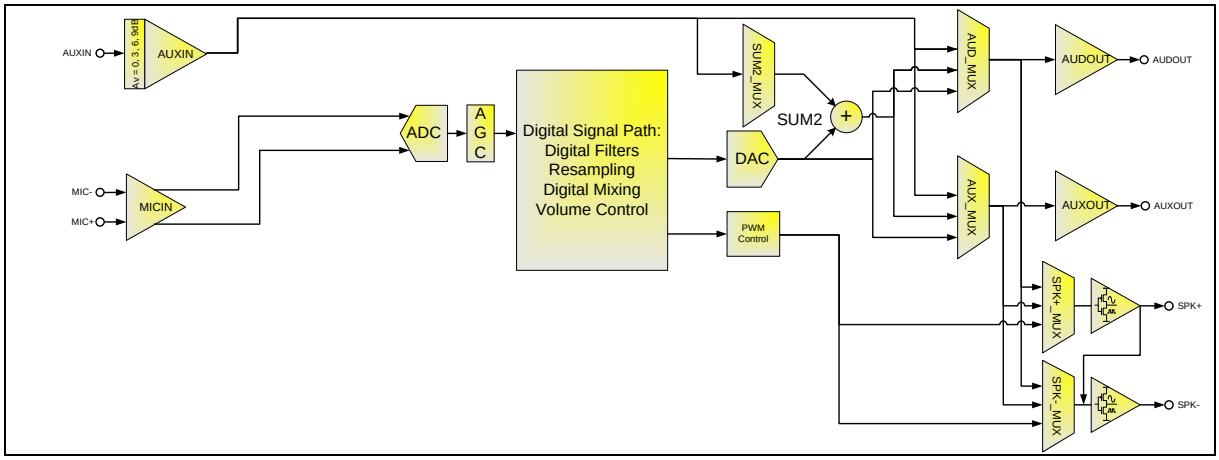


Figure 7-2 Analog Signal Path, MICIN Selected

Analog outputs consist of:

- AUXOUT is a single-ended voltage output
- AUDOUT can be configured as a single-ended voltage output or a single-ended current output. When configured as a voltage output, AUDOUT is exactly the same as the AUXOUT.
- BTL (bridge-tied-load) is a differential voltage output, which shares the same two pins of PWM (SPK+/SPK-). Signal source of BTL could be either from AUD_MUX or AUX_MUX.
  - Besides BTL, SPK+ and/or SPK- can also be configured individually:
    - SPK+ can switch to AUDOUT or AUXOUT
    - SPK- can switch to AUDOUT or AUXOUT

The analog path consists of the following blocks: AUXIN, ANAIN (or MICIN), SUM1, ADC_MUX (SUM1 and ADC_MUX are ineffective when MICIN is selected), SUM2, SUM2_MUX, AUD_MUX, AUX_MUX, SPK+_MUX, and SPK-_MUX. The summation blocks, SUM1 and SUM2, are able to mix two signals together. SUM1 mixes the two analog inputs (AUXIN and ANAIN) for input into the digital signal path. SUM2 mixes the analog input (AUXIN, or ANAIN, or AUXIN plus ANAIN) with the digital signal path output. ADC_MUX provides input selection into the ADC. AUD_MUX and AUX_MUX provide input selection into the AUDOUT and AUXOUT blocks. SPK+_MUX and SPK-_MUX provide input selection into the SPK+ and SPK- blocks. The configuration registers, CFG5-CFG9 & CFG18, control the active path features, allow individual power control of each block and enable the muting of certain path inputs. The details of the path configuration registers are described in Section 12.3.

7.1.1 ANAIN & MICIN Analog Input

Single-ended ANAIN Input

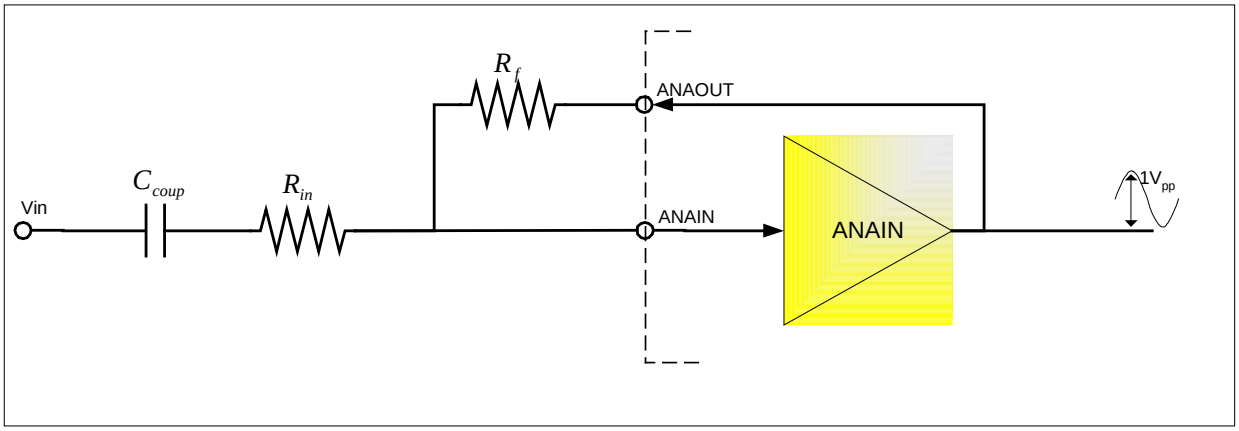


Figure 7-3 ANAIN Input Amplifier

The ANAIN input amplifier is designed to allow a variable gain set via two external resistors. The goal of gain selection is to produce a $1V_{pp}$ signal into the ISD15C00 audio path. Voltage gain is: $A_v = R_f / R_{in}$.

ANAIN supports gain settings from 1 to 100 according to $A_v = R_f / R_{in}$. R_f should satisfy $40k\Omega \le Rf \le 100k\Omega$. To achieve a gain of 100, R_f can be set to $100\,k\Omega$, and R_{in} set to $1\,k\Omega$.

C_{coup} AC couples signals into the ISD15C00, forming a single pole high pass filter. The 3dB frequency is given by:

$$f_{pass} = \frac{1}{2\pi R_{in} C_{coup}}$$

For $C_{coup} = 1\mu F$, $R_{in} = 1k\Omega$, signals above 160Hz will be fed into the audio path.

Differential MICIN Input

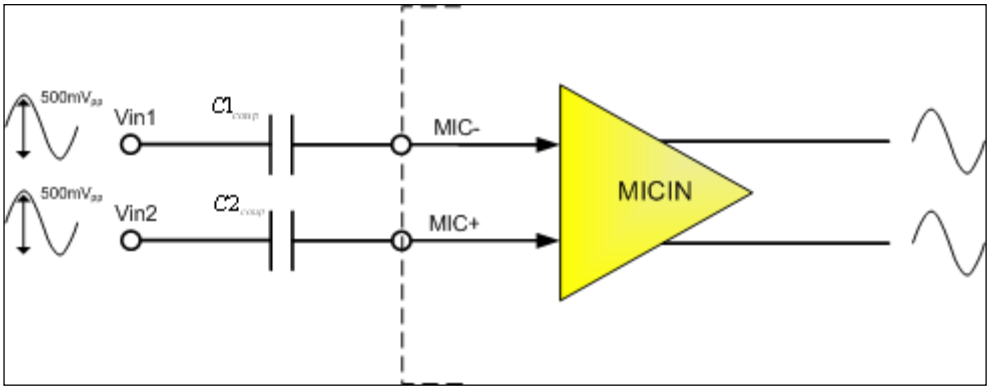


Figure 7-4 Differential MIC Input Amplifier

The ISD15C00 allows the use of pins ANAIN and ANAOUT as differential MIC inputs. In this mode, the ANAIN and ANAOUT pins become MIC+ and MIC- and allow a differential input to be applied to the ADC. This configuration is designed to be used in conjunction with the AGC to amplify microphone signals while achieving good common mode rejection of supply noise. No mixing with AUXIN is possible in this mode.

7.1.2 AUX Analog Input

The AUX Analog Input amplifies input signals with a fixed gain of 0dB, 3dB, 6dB, or 9dB, selectable via SPI command. Similar to ANAIN, the gain setting should be configured so that the output signal has a 1Vpp swing.

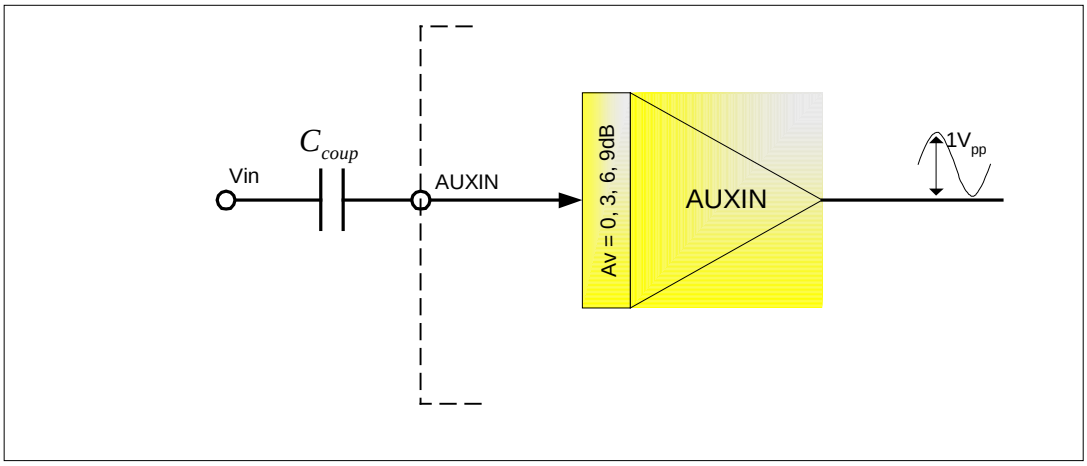


Figure 7-5 AUXIN Input Amplifier

The coupling capacitor, C_{coup}, like in the case of ANAIN, should be set according to the value of R_{in} to allow signals above a certain frequency to pass through. The relationship repeated here is:

$$f_{pass} = \frac{1}{2\pi R_{in} C_{coup}}$$

R_{in} is the input impedance of the AUXIN amplifier and is dependent upon the gain setting as shown in Table 7-1 below.

Table 7-1 Gain Setting Vs. Rin

Setting	Gain dB	Gain	Rin (kOhms)
00	0	1.00	40.0
01	3	1.41	33.2
10	6	2.00	26.7
11	9	2.82	21.0

The minimum value of R_{in} is approximately 20kOhms, so a C_{coup} of 1µF will allow audio signals to pass through under all possible gain settings.

7.1.3 AUX & AUD Analog Output

AUXOUT is a single-ended voltage output. It needs an external amplifier to drive the speaker. AUXOUT together with the external amplifier is usually used when loud volume like 1 watt output is needed.

AUDOUT can be configured as a single-ended voltage output or a single-ended current output. When configured as a voltage output, AUDOUT is exactly the same as the AUXOUT. When configured as a current output, it uses a transistor to drive the speaker. Please note that the signal coming out of AUD_MUX is always voltage regardless configured as a voltage or current output; if configured as a current output, the AUDOUT block that follows the AUD_MUX converts the voltage signal to current signal.

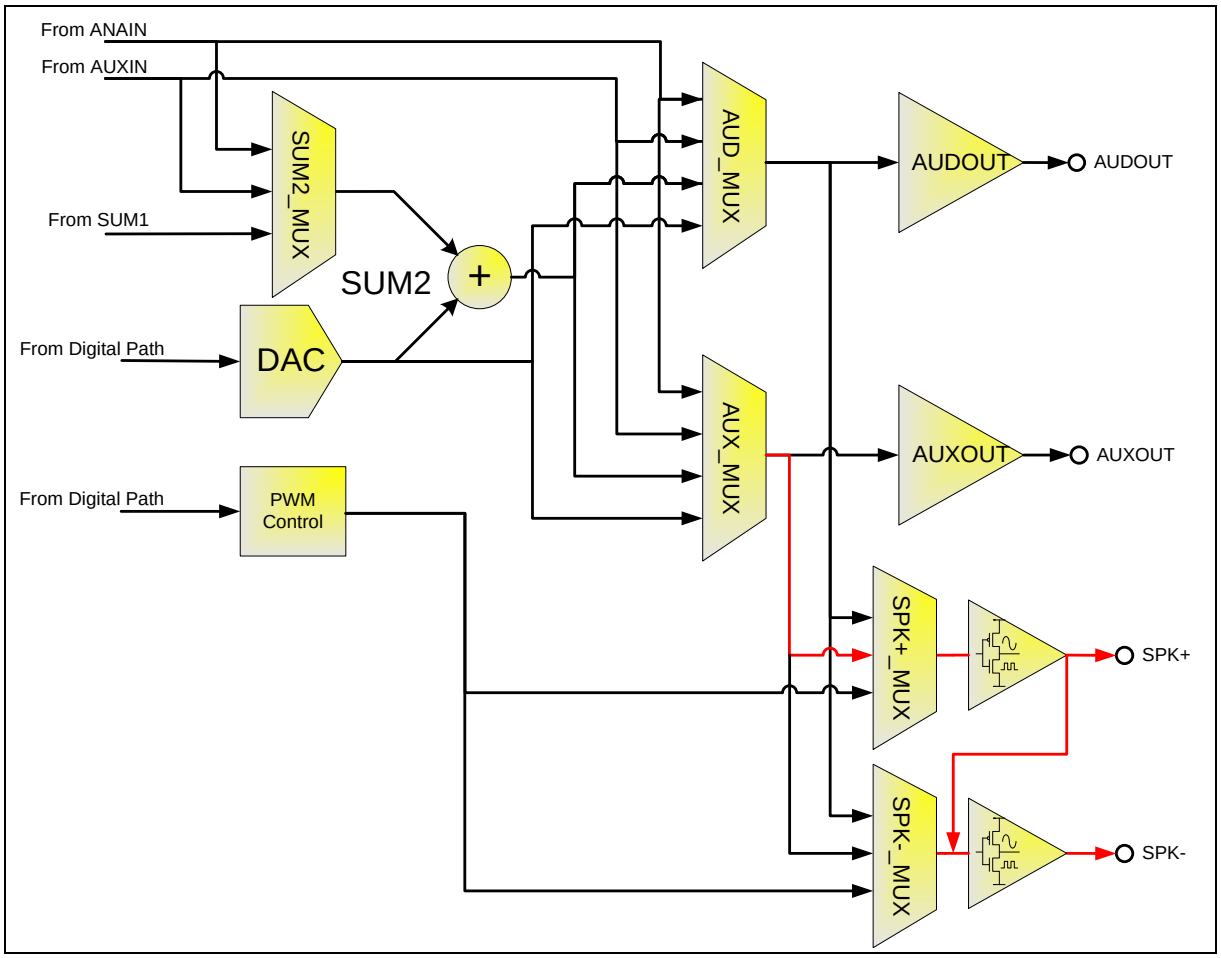


Figure 7-6 Analog Outputs

7.1.4 BTL Analog Output

BTL (bridge-tied-load) is a differential voltage output, which shares the same two pins of PWM (SPK+ and SPK-). As a differential output, BTL is naturally better than AUXOUT, the single-ended output, in terms of noise rejection.

BTL can directly drive a speaker or drive a speaker via an external amplifier. Since BTL direct-drive cannot reach the volume level that most users require, a usage together with an external amplifier is recommended. Below is a table comparing the BTL, AUXOUT, and PWM:

	BTL	AUXOUT	PWM
Driving Method	Can direct drive, but an external amplifier is required to reach adequate volume level.	Need an external amplifier.	Direct drive.
Driving Ability	High: depends on the external amplifier.	High: depends on the external amplifier.	360 mW.
Quality	Typical 80dB with good noise rejection.	Typical 80dB.	Typical 60dB
Cost	Extra cost of the external amplifier.	Extra cost of the external amplifier.	No extra cost.

Table 7-2 Comparison of BTL, AUXOUT, and PWM

Signal source of BTL could be either from AUD_MUX or AUX_MUX.

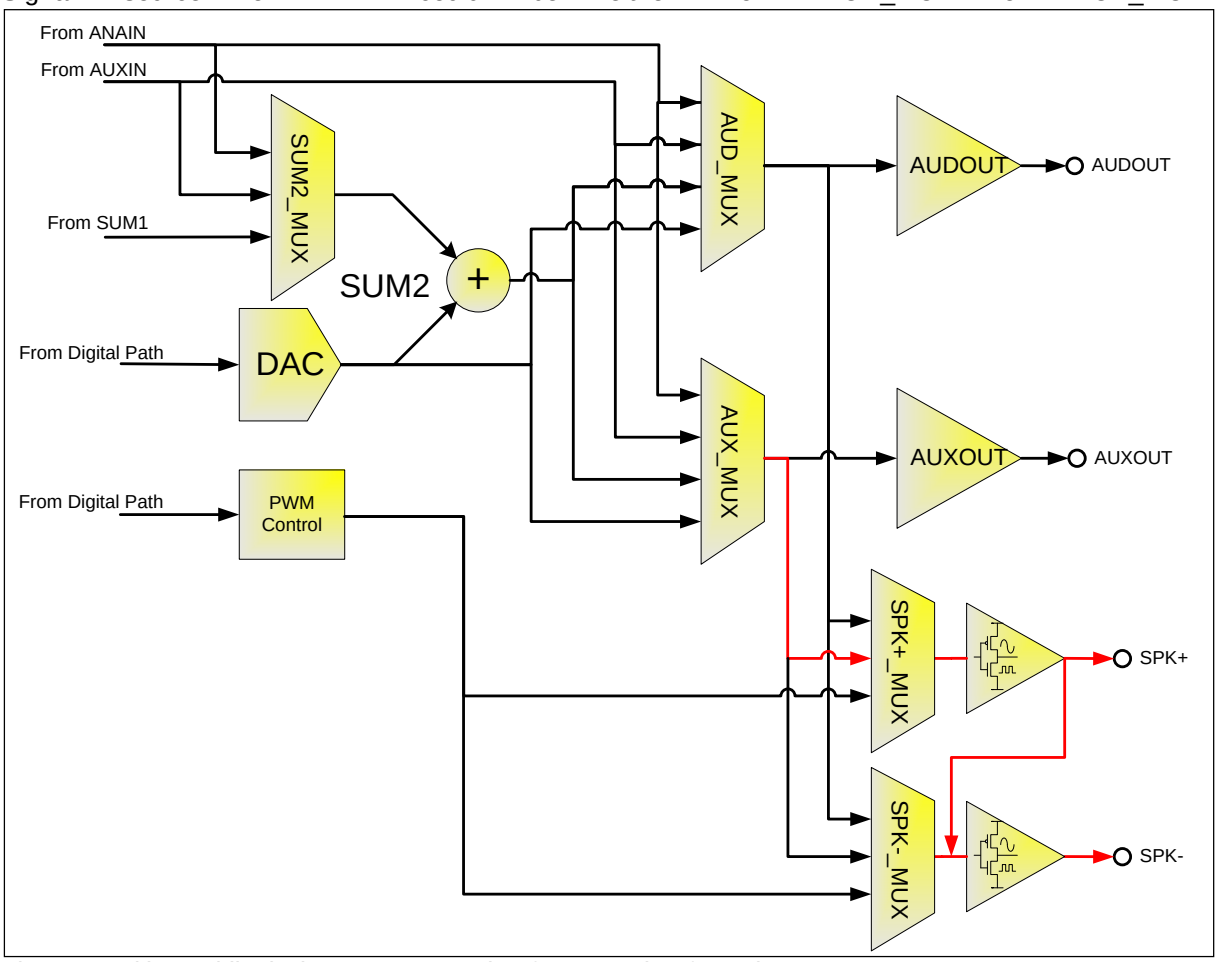


Figure 7-6 (the red line) shows an example of BTL setting from the AUX_MUX.

Besides BTL, SPK+ and/or SPK- can also be configured individually:

- SPK+ can switch to AUDOUT or AUXOUT
- SPK- can switch to AUDOUT or AUXOUT

For detailed settings, please refer to 12.3 Device Configuration Registers, CFG18.

7.2 DIGITAL SIGNAL PATH

The digital signal path performs filtering, sample rate conversion, mixing, volume control and compression. A block diagram of the digital signal path is shown in Figure 7-7.

Figure 7-7The digital signal path operates at a master sample rate Fs (nominally 32kHz) set by the master clock source (see Section 10). It has the ability to up-sample or down-sample to a lower sample-rate, Fsub for record, playback and audio transfer to/from the SPI interface. Audio input at Fs into the signal path comes either from the ADC path or the I²S digital audio interface. Audio at Fsub is up-sampled and can be mixed with the input and level adjusted via VOLA, VOLB and VOLC before going out on the DAC, I²S or PWM driver paths. The FIFO synchronizes audio sources at the sub-sampled bandwidth. One input and one output can be active at a time. The possible combinations are:

SPI_IN → COMPRESS (SPI record)
SPI_IN → UPSAMPLE (SPI feed-through)
DOWNSAMPLE → COMPRESS (record)
DOWNSAMPLE → SPI_OUT (feed-through SPI)
DECOMPRESS → SPI_OUT (SPI playback)
DECOMPRESS → UPSAMPLE (Playback)

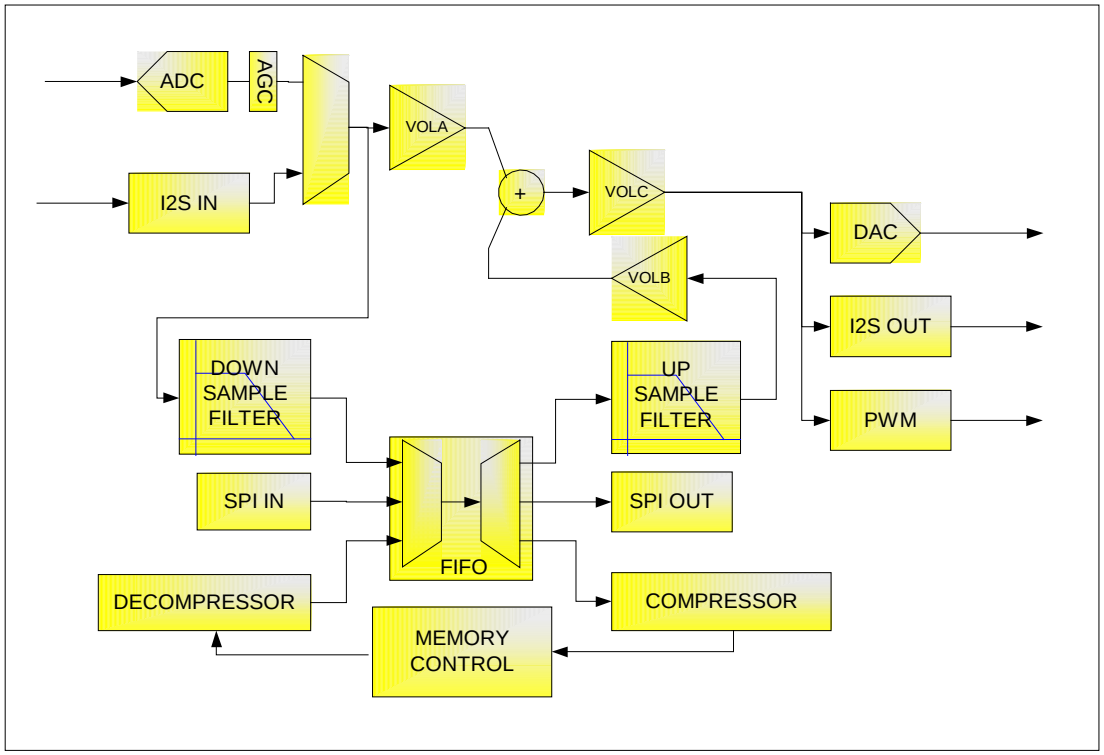


Figure 7-7 Digital Signal Path

8 ISD15C00 MEMORY MANAGEMENT

The ISD15C00 employs several memory management techniques to make audio recording and playback transparent to the host controller. The address space of the ISD15C00 starts at address zero of the external memory. This external memory size can range from 1M to 128M with an erasable sector size of 4kBytes. Please note that Digital Read and Digital Write commands can access up to 64Mbit (0x000000 ~ 0x7FFFFF), while Play, Record, and Erase commands can access up to 128Mbit (0x000000 ~ 0xFFFFFF). The following sections will describe the ISD15C00 memory management architecture and the message management functions.

8.1 ISD15C00 MEMORY FORMAT

The Recording Memory Pointer (RMP) divides the ISD15C00 memory address space into two blocks, Reserved Memory and Recording Memory. The RMP is a two-byte address pointer pointing to a 4kByte memory sector which is the first sector available to users for recording messages. Memory between address zero and the RMP pointer is considered the Reserved Memory for pre-recorded audio (Voice Prompts), pre-programmed macro scripts (Voice Macros), digital read/write access for other applications (User Data) and memory sectors reserved for the first sector of the message recordings and re-recordable pre-recorded messages (Reserved Sectors). The memory between the RMP and the end of memory is considered the Recording Memory allocated for recording messages (Message Recordings).

Figure 8-1 illustrates the memory format with the RMP set at address 4000h or sector 4. Section 8.3 will provide more detail regarding the setting of the RMP.

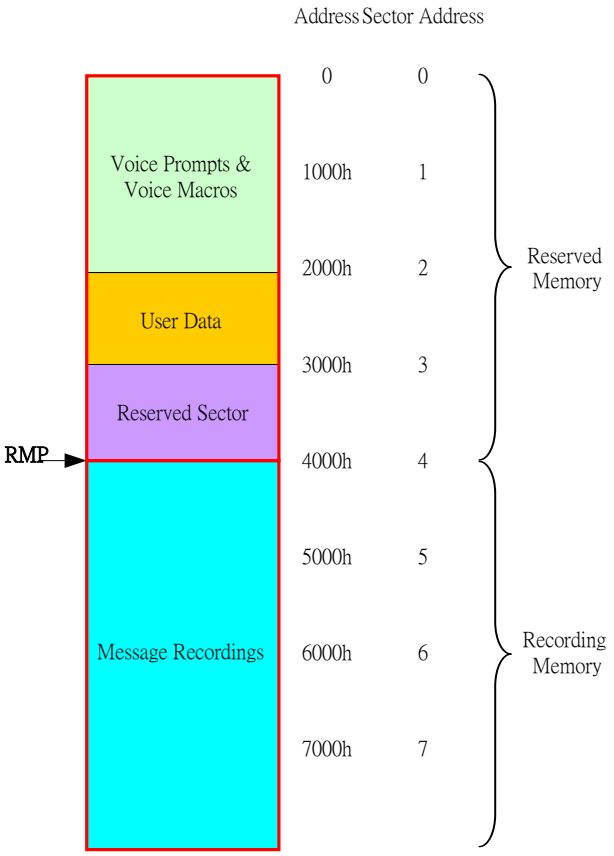


Figure 8-1 ISD15C00 Memory Format

8.2 Message MANAGEMENT

The message management schemes implemented on the ISD15C00 are:

1. Voice Prompts: A collection of pre-recorded audio that can be played back using the PLAY_VP SPI command or Voice Macros.
2. Voice Macros: A powerful voice script allowing users to create custom macros to play Voice Prompts, play message recordings, insert silence and configure the device. Voice Macros are executed with a single SPI command.
3. User Data: Memory sectors defined and allocated by the users for use in other applications
4. Reserved Sectors: Memory sectors reserved for the first sector of the message recordings (Empty Message) and re-recordable pre-recorded messages (Re-recordable Message).
5. Message Recordings: Messages recorded, played and erased “on the fly” by the users.

8.2.1 Voice Prompts

Voice prompts are pre-recorded audio of any length, from short words, phrases or sound effects to long passages of music. These Voice Prompts can be played back in any order as determined by the users and applications. A Voice Prompt consists of two components:

1. An index pointing to the pre-recorded audio
2. Pre-recorded audio

To play a Voice Prompt, the ISD15C00 use the index of the Voice Prompt to locate and play the pre-recorded audio. This approach allows users to easily manage the pre-recorded audio without the need to update the code on the host controller. In addition, the users can store a multitude of pre-recorded audio without the overhead of maintaining a complicated lookup table. To assist customers in creating the Voice Prompts, a software tool, the ISD15C00 Voice Prompt Editor and writer are available for development purposes.

8.2.2 Voice Macros

Voice Macros are a powerful voice script that allows users to customize their own play patterns such as play Voice Prompts, play message recordings, insert silence, change the master sample clock, power-down the device and configure the signal path, including gain and volume control. Voice Macros are executed using a single SPI command and are accessed using the same index structure as Voice Prompts. This means that a Voice Macro (or Voice Prompt) can be updated on the ISD15C00 without the need to update code on the host micro-controller since absolute addresses are not needed.

The following locations have been reserved for two special Voice Macros:

Index 0: Power-On Initialization (POI)

Index 1: Power-Up (PU)

These Voice Macros allow the users to customize the ISD15C00 power-on and power-up procedures and are executed automatically when utilized. The built-in voice macros will be used when they are not utilized. Please see Section 11 for details.

Here is an example to illustrate the usage of the PU Voice Macro.

- SET_CLK_CFG(0x37)
- WR_CFG_REG(0x05,0x01)
- WR_CFG_REG (0x06,0x02)
- FINISH

The above PU Voice Macro will perform the following:

- Choose a 2.048MHz crystal as a clock source
- Set up a feed-through path from ANAIN to AUDOUT

The following is the complete list of the commands for Voice Macro:

- SET_CLK_CFG(n) – Set clock configuration register to n.
- WR_CFG_REG(reg,n) – Set configuration register reg to value n.
- PWR_DN – Power down the ISD15C00.
- PLAY_VP(i) – Play Voice Prompt index i.
- PLAY_MSG@(sec-addr) – Play message starting at sector address sec-addr
- PLAY_SIL(n) – Play silence for n units. A unit is 32ms at master sampling rate of 32 kHz.
- WAIT_INT – Wait until current play command finishes before executing next macro instruction.
- FINISH – Finish the voice macro and exit.

8.2.3 User Data

User Data consist of 4kByte chunks of erasable sectors defined and allocated by the users for use in other applications. The users have the freedom not to allocate or reserve any memory sectors. A software tool, the ISD15C00 Voice Prompt Editor is available to assist customers in allocating such memory.

8.2.4 Reserved Sectors

Reserved sectors consist of 4kByte chunks of erasable sectors reserved for the Empty Messages and Re-recordable Messages. The Empty Message is an empty sector made of a 4kByte memory sector reserved for message recordings. A SPI record command pointing to the Empty Message starts the message recording into the Empty Message and will continue to record messages in the free memory located in Recording Memory if the message recording is over 4kBytes. The users can send a play, erase or record command pointing to the Empty Message to play, erase the entire message or re-record a brand new message.

The Re-recordable Message, a 4kByte memory sector contains message recordings and a sector address pointer (see Section 8.3 for details) pointing to the message sector located in Recording Memory. Unlike the Empty Message where no message has been recorded, the users can play back a complete message by issuing a SPI play command pointing to the Re-recordable Message. The users can also send an erase or record command pointing to the Re-recordable Message to erase the entire message or re-record a brand new message.

8.2.5 Message Recordings

Message Recordings are messages that can be recorded, played and erased “on the fly” by the users. These messages are recorded in 4kByte chunks of erasable sectors with each message sector containing a header pointing to the next message sector. The ISD15C00’s unique message management architecture allows users to record messages without specifying an address. The ISD15C00 will start recording at the first available sector in Recording Memory and continue to record into free memory until memory is full or a STOP command is issued. Upon completion of the record operation, the users need to read back the message sector start address for subsequent playback.

To playback the message recordings, the users need to send a play command pointing to the message sector start address. For partial message playback, the users can send a play command with a sector offset.

To erase the message recordings, the users need to send an erase command pointing to the message sector start address.

A list of commands for Message Recordings are detailed below:

- REC_MSG – starts a record operation.
- STOP – stops current record operation.
- READ_STATUS – wait until record operation is finished as indicated by the CMD_FIN bit.
- READ_INT – clear the interrupt.
- READ_MSG_ADD – This command returns a three byte starting address (A) of the message along with a two byte sector length. Use A to address the message in subsequent playback operations.
- PLAY_MSG@(A) – Play back the message.
- READ_STATUS – poll status until CMD_FIN bit is set indicating play has finished.
- READ_INT – clear the interrupt.
- ERASE_MSG@(A) – erase the message.
- READ_STATUS – poll status until CMD_FIN bit is set indicating erase has finished.
- READ_INT – clear the interrupt.

8.3 MEMORY AND MESSAGE HEADERS

The Memory and Message headers are located at the initial bytes of the 4kByte memory sector used to determine the format or function of the memory. The Memory Header stores users' configurable information including the memory protection scheme, the RMP and PMP pointers and the index table including POI, PU and other Voice Macros defined by the users. The Message Header located in both Reserved Sectors and Recording Memory stores the information for the device to determine what memory is available for recording and where the subsequent messages are stored.

8.3.1 Memory Header

Table 8-1Memory Header

Initial Bytes of the Memory Header						
Byte0	**Byte1-2**	**Byte3-4**	**Bytes5-10**	**Bytes11-16**	**Byte17-22**	**Byte23-28**
0xCX	RMP[7:0]	PMP[7:0]	POI_VM	PU_VM	VM/VP[2]	VM/VP[3]

The Memory Header contains at least seventeen bytes located at the beginning of the memory space. Byte0 determines whether or not the memory contains a Reserved Memory block as well as the memory protection scheme is used. Byte1-2 and Byte3-4 store the RMP and PMP pointers respectively. After the PMP, it is the start of the Voice Prompt/Voice Macro index table defined by the users. This table consists of six byte entries that are the start and end address of Voice Prompt or Voice Macro. Byte5-10 & Byte11-15 are reserved for the POI and PU Voice Macro which are the first two entries in this table (index 0 and index 1) to be executed on power-on initialization and power-up respectively. If this function is not desired, these entries should be left erased (0xFFFFFF,0xFFFFFF). When a PLAY_VP(i) or EXE_VM(i) command is sent to the ISD15C00, it reads the index table entry at address 6i+5 and executes the VP or VM at the address present in the table.

If the first byte Byte0 of the memory header is 0xFF, it means that no Reserved Memory is allocated, no memory protection is enabled and the whole memory will be available for record and playback only. To allocate the Reserve Memory, the bit4 of the Byte0 has to be set to zero. When Reserved Memory is allocated and memory protection is enabled upon users' definition, the both RMP (Recording Memory Pointer) and PMP (Protected Memory Pointer) will then created and stored at Byte1-2 and Byte3-4 of the Memory Header respectively. The ISD15C00 will not attempt to use memory before the RMP for message recordings. This memory thus can be used for Voice Prompts, Voice Macros, User Data and Reserved Sectors. The PMP points to the boundary of protected memory and is used in conjunction

with the RP, WP and CEP bits to set memory protection indicated below (also see Section 8.6 for details).

Table 8-2 The first byte of the Memory Header

Memory Header Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	0	1	RP	WP	CEP

8.3.2 Message Header

Table 8-3 Message Header

Message Header Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
BOM	EOM	RSVD	-	-	-	-	-

The ISD15C00 adopts a sector-based message management scheme that treats each 4kByte sector as a message frame. Each sector has a header indicating the state of the frame:

- BOM: “0” indicates that this sector is the beginning of a message.
- EOM: “0” indicates that this sector is the end of a message.
- RSVD: “0” indicates that there is a message recorded in this sector or this sector has been reserved for User Data.

Thus the number of the BOMs counted by scanning the Message Header of the Recording Memory will tell the number of the messages recorded in the ISD15C00.

When a sector is not an EOM sector, the next two bytes in the frame are the sector address pointing to the subsequent message. Thus the whole message can be re-composed by tracing sector address until an EOM is found.

It is not recommended to reserve the User Data inside the Recording Memory. However, for those instances where User Data needs to be allocated inside the Recording Memory, it is imperative that the RVSD has set and maintained at “0”. Otherwise, there is a risk that the User Data may be over-written by subsequent recordings.

8.4 DIGITAL ACCESS OF MEMORY

ISD15C00 memory can be accessed as conventional digital memory using the DIG_READ and DIG_WRTIE SPI commands. This allows the user to:

- Reserve areas of memory for use as digital non-volatile memory as User Data
- Update Voice Prompts and macros (pre-recorded audio) in system.
- Read and verify Voice Prompt memory.
- Read sector headers of memory to determine memory usage.

The digital read and write commands can be issued even while an audio record or playback is in progress. The RDY/BSYB pin governs the flow control for all digital operations.

8.5 DEVICE ERASE COMMANDS

ISD15C00 provides several ways to erase the flash memory. The flash memory has a minimum erasable sector size of 4kBytes. The sector erase command is sent with a start and stop sector address. The ISD15C00 also has commands to mass erase the memory.

8.6 MEMORY CONTENTS PROTECTION

Under certain circumstances, it is desirable for the users to protect portions of the external memory from write/erase or interrogation (read). The ISD15C00 provides a method to achieve this by setting a protection memory pointer (PMP) that allows the users to protect external memory for an address range from the beginning of memory to this sector where PMP is pointed. The type of protection is set by three bits in the memory header byte.

- The **CEP** (Chip Erase Protect) bit set to zero enables chip erase protection. This prevents a mass erase function, allowing the device to be configured as a write-once part. With the **CEP** bit set to one, even with write protection enabled, the part can be mass erased. After mass erasure, the initial sector byte defaults to no protection so the device can be re-programmed.
- The **WP** (Write Protect) bit set to zero enables write protection of the external memory below the sector pointed to by the PMP. Write protection means that digital write or erase commands will not function in this memory area. This can be used to ensure that audio or data is not inadvertently erased or overwritten. The **WP** bit does not stop the execution of a REC_MSG@ or ERASE_MSG@ to messages with BOM headers in this memory.
- The **RP** (Read Protect) bit set to zero enables read protection of the external memory below the sector pointed to by the PMP. Read protection means that digital read or audio playback commands through SPI or I^2S will not function in this memory area. This can be used to ensure that external memory contents cannot be digitally copied or read.

Memory protection is activated on power-up of the chip. Therefore, each time the user changes the setting of memory protection, the new setting will not be effective until the chip is reset.

9 I²S INTERFACE

The I²S interface is a digital audio interface that allows the transfer of the audio data between other digital audio devices such as multimedia processors, audio amplifiers or DSPs. The ISD15C00 acts as either a master or a slave device on an I²S bus. As a slave the ISD15C00 accepts SCK and WS clock and frame signals from a bus master. In master mode the ISD15C00 generates SCK and WS. It is capable of both data input and output depending upon configuration. The ISD15C00 is configurable to accept data from either the left or right audio channel or a mono mix of both. It can output data to either the left, right or both channels. It is also capable of feeding through a stereo signal and mixing a playback operation into the signal. In slave mode, to synchronize data transfer, the ISD15C00 must derive its master clock from the I²S SCK or be operating from a synchronous external clock source.

I²S is for high bandwidth audio input/output. High bandwidth audio input comes either from the ADC path or the I²S. High bandwidth audio output goes out on the DAC, I²S or PWM driver paths. It all depends on how you configure the path. However, commanding the ISD15C00 is through SPI commands. For instance, the user could configure the path, through the SPI commands, as: "I²S input -> ADPCM-4bit Compression -> Memory Control", then the user can feed the audio data from I²S.

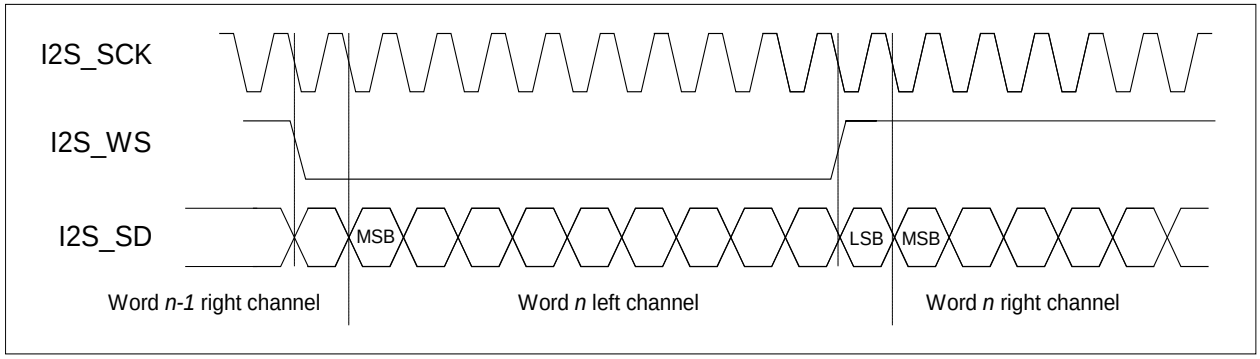


Figure 9-1 I²S Protocol

10 CLOCK GENERATION

The ISD15C00 can derive its master clock from five sources:

1. An external crystal (or resonator) oscillator interface.
2. An external clock input (applied to pin XTALIN and left the XTALOUT unconnected)
3. An internal oscillator controlled by an external resistor (attached to pin XTALIN and GND).
4. An internal oscillator with internal reference.
5. The SCK clock of the I²S interface.

Regardless of source, the selected clock is fed to a phase-locked loop (PLL) to generate the internal master clock (MCLK) of the ISD15C00.

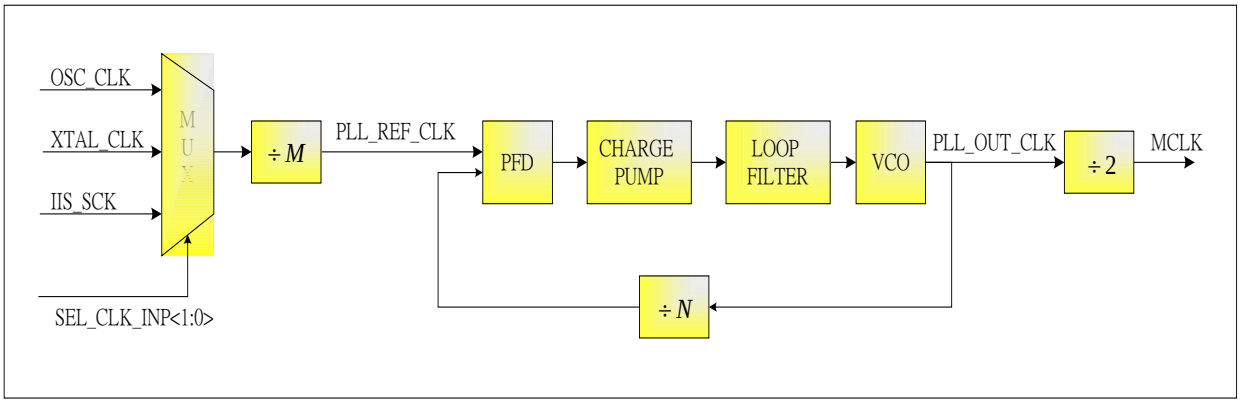


Figure 10-1 PLL Clock Generation on ISD15C00

The goal of clock generation is to generate a master clock rate (MCLK) at 512x the master sample rate (Fs). A table of supported master clock and sample rates is shown below. The master sample frequency can be expressed by the formula:

$$F_{MCLK} = F_{OSC}\frac{N}{2M} \text{ where } M = \{1,2,3\} \text{ and } N = \{8,16,32\}$$

$$F_s = F_{MCLK}\frac{1}{512}$$

Table 10-1 Master Clock and Sample Rates

MCLK (MHz)	Fs (kHz)
16.384	32
24.576	48
22.5792	44.1

For the above master sample rates, Fs, record and playback is available at fixed ratios of the master sample rate.

Table 10-2 Sub-Sample Rates available.

Sub-Sampled ratio	Master Sample Rate Fs (kHz)			Available Sample Rates (kHz)
	32	44.1	48	
8	4	5.5125	6	
6	5.333	7.35	8	
5	6.4	8.82	9.6	
4	8	11.025	12	
2.5	12.8	17.64	19.2	
2	16	22.05	24	
1	32	44.1	48	

10.1 External Crystal Oscillator

The external circuit for attaching a quartz crystal or ceramic resonator is shown in Figure 10-2. In this circuit, Rf is several MΩ and is used to DC bias the internal amplifier. R1, C1 and C2 are chosen so as not to overdrive the crystal and to suppress oscillation at higher crystal harmonics.

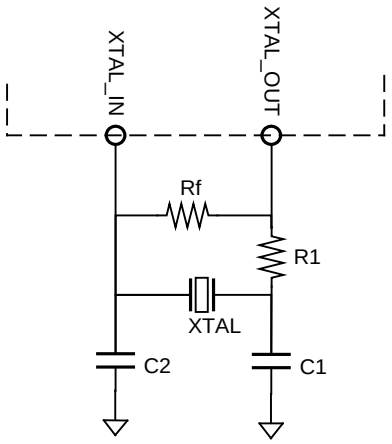


Figure 10-2 Crystal Oscillator

Some common crystal frequencies to achieve desired Fs are shown in Table 10-3.

Table 10-3 Common Crystal Frequency Settings

Xtal (MHz)	M	N	Fs (kHz)
1.024	1	32	32
2.048	2	32	32
3.072	3	32	32
4.096	2	16	32
6.144	3	16	32
8.192	2	8	32
12.288	3	8	32
1.4112	1	32	44.1
2.8224	2	32	44.1
4.2336	3	32	44.1
5.6448	2	16	44.1
8.4672	3	16	44.1
11.2896	2	8	44.1
16.9344	3	8	44.1
1.536	1	32	48
3.072	2	32	48
4.608	3	32	48
6.144	2	16	48
9.216	3	16	48
12.288	2	8	48
18.432	3	8	48

In addition to the above crystals, to achieve standard audio sampling rates, other frequencies could be used that would produce different sample rates. For instance if the user wishes to use the standard USB clock rates of 6 or 12MHz the following master sample rates could be achieved.

Table 10-4 USB Crystal Master Sample Rates

Xtal (MHz)	M	N	Fs (kHz)
12	2	8	46.875
12	3	8	31.25
6	3	16	31.25
6	2	16	46.875

10.2 I²S Clock Usage

The SCK clock of the I²S interface must be used to synchronize the ISD15C00 if an I²S interface is used. The ISD15C00 accepts I²S_SCK clock rates of 32xFs or 64xFs.

Table 10-5 Supported I²S Clock Rates with PLL Settings

I²S_SCK (MHz)	M	N	Fs (kHz)
1.024	1	32	32
2.048	2	32	32
1.4112	1	32	44.1
2.8224	2	32	44.1
1.536	1	32	48
3.072	2	32	48

10.3 Internal Oscillator

The ISD15C00 also provides an internal oscillator that requires only an external resistor to operate. If the device is configured to use the internal oscillator, then a resistor is connected to the XTALIN pin and GND. The internal oscillator with external resistor has an accuracy of ±5% and gives a master sample rate of:

$$F_s = \frac{32 \times 80 \times 10^3}{R_{OSC}} \text{ (kHz) for } M = 2,\ N = 32$$

So if the user connects an 80kohm resistor to the XTALIN and GND, a 32 kHz sample frequency is fed-through the analog path.

11 INITIALIZATION & RECORD/PLAY FLOWCHART

Whenever the ISD15C00 detect as power-on reset condition or a high on the RESET pin of the device it begins a power-on initialization (POI) sequence. Whenever the ISD15C00 receives a power up command (PU) when it is in a power down state, it begins a power-up initialization (PU) sequence. Voice Macros VM(0) and VM(1) are reserved for POI and PU initialization routines. If no reserved memory exists or if the vectors VM(0) or VM(1) are not set, then a default routine is executed. The default sequence for POI is to power-down the ISD15C00. The default PU sequence is to select a clock configuration of internal oscillator with PLL active for Fs=32kHz.

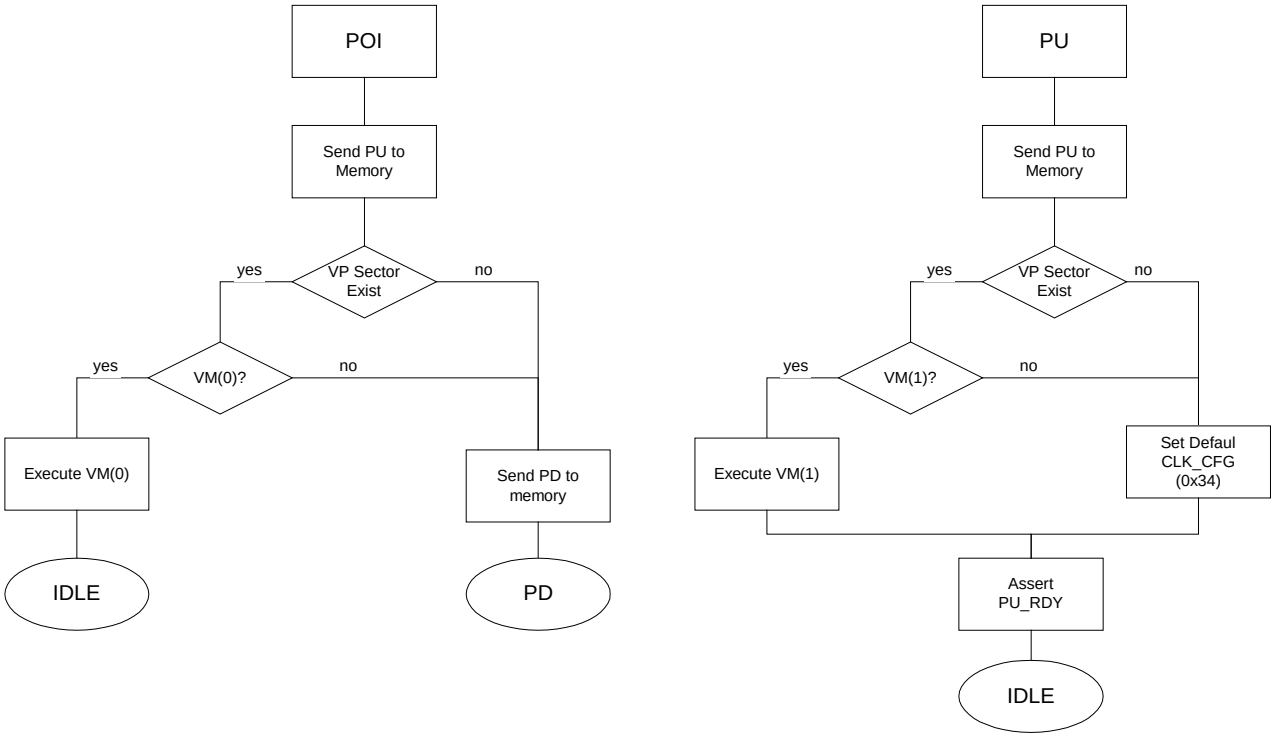


Figure 11-1 POI and PU Initialization Flowcharts

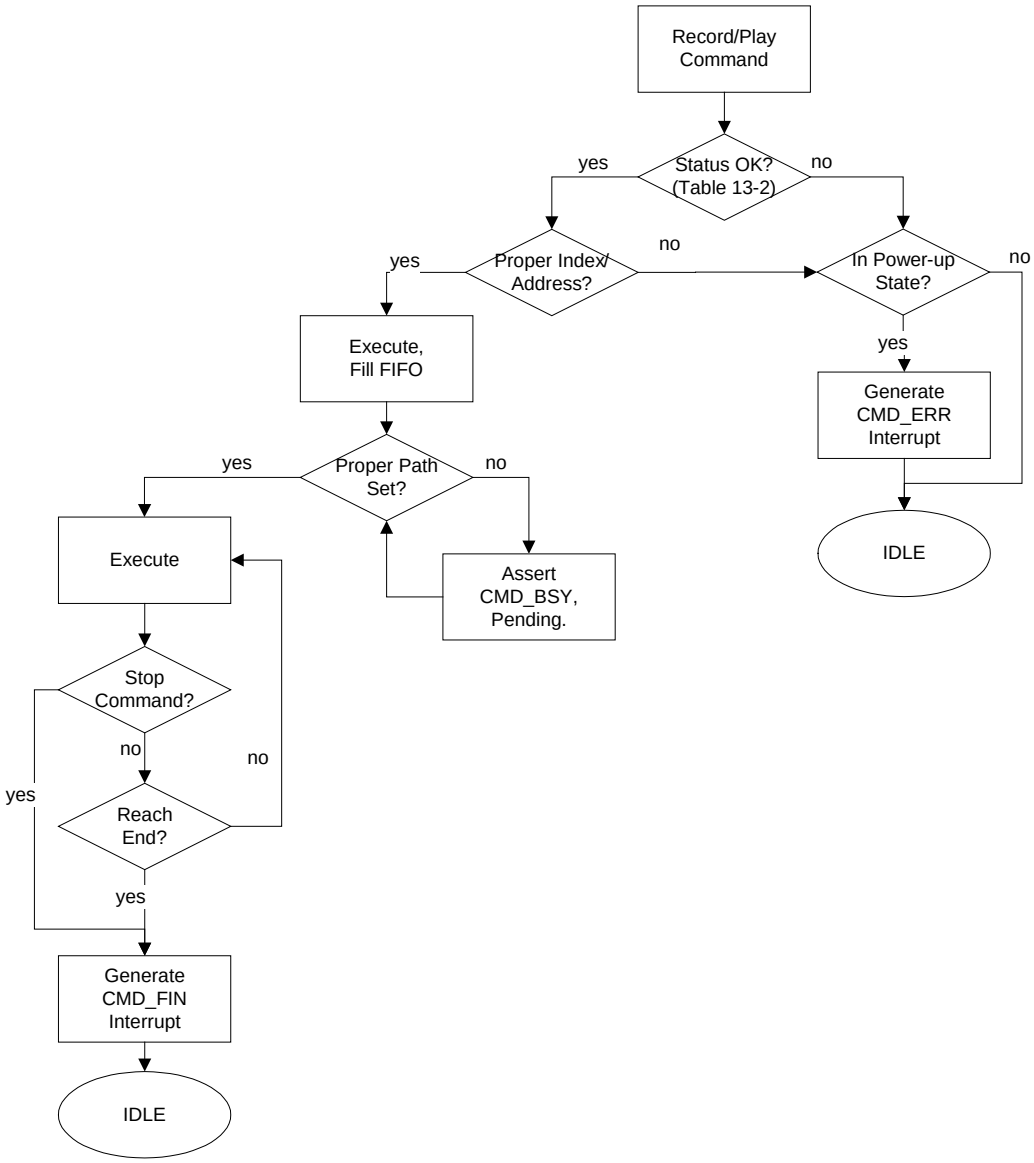


Figure 11-2 Record/Playback Flowchart

12 DEVICE CONFIGURATION AND STATUS

12.1 CLOCK CONFIGURATION

The clock configuration register is accessed via the SET_CLK_CFG command. It configures the clock source of the ISD15C00. The default state of the clock configuration register is0x34, that is internal clock with internal reference, PLL active for 32kHz sample rate and no external clock output. When PLL_BYPASS is set, the PLL is powered down and PLL_REF_CLK is fed directly to MCLK. The CLK_OUT control bits configure the I^2S clock pin, SCK, as a clock output to allow the ISD15C00 to provide an oscillator output to another device such as the host microcontroller.

Table 12-1 Clock Configuration Register Description

CLK_CFG							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CLK_OUT[1:0]		CLK_N_DIV[1:0]		CLK_M_DIV[1:0]		CLK_INP_SEL[1:0]	
00		11		01		00	

Default 0x34:

- Internal clock with internal reference
- PLL active for F_s=32khz sample rate
- No external clock output

Table 12-2 Clock Configuration Source

CLK_INP_SEL	
CLK_INP_SEL[1:0]	**Clock Source**
00	Internal Oscillator with Internal Reference
01	IIS SCK Clock
10	Internal Oscillator with Rext
11	XTAL Interface

Table 12-3 Clock PLL M Divisor

CLK_M_DIV	
CLK_M_DIV[1:0]	**M**
00	1
01	2
10	3
11	N/A

Table 12-4 Clock PLL N Divisor

CLK_N_DIV	
CLK_N_DIV[1:0]	**N**
00	PLL_BYPASS
01	8
10	16
11	32

Table 12-5 External Clock Output

EXT Clock	
CLK_OUT[1:0]	
00	NONE – OFF
01	Fosc
10	PLL_REF_CLK
11	MCLK

12.2 DEVICE STATUS REGISTER

Whenever the ISD15C00 receives an SPI command it also returns its current status via MISO. The details of the status byte are shown below. For commands that are not reading digital data from the device this status byte is sent via MISO for every byte of data sent to the ISD15C00.

Table 12-6 Status Register Description

Status Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PD	DBUF_RDY	INT	RM_FUL	-	VM_BSY	CBUF_FUL	CMD_BSY

The individual bits of the status register refer to the following conditions:

- **PD** – If this bit is high then the device is powered down. The DBUF_RDY bit will be low, but all device output pins will be high impedance. When PD is high only the READ_STATUS, READ_INT and PWR_UP commands are accepted. If any other command is sent, it is ignored

and no interrupt for an error is generated.

- **DBUF_RDY** – in PD this bit is low indicating the device can only accept a PWR_UP (power up) command. When PD is low this bit reflects the state of the RDY/BSY pin.
- **INT** – an interrupt has been generated. The interrupt is cleared by the READ_INT command. Interrupt type can be determined by the bits of the Interrupt Status Byte.
- **RM_FUL** – Recording Memory is full. This bit will be set if a record command fills the memory. This bit is reset by an ERASE_MSG@, ERASE_MEM, or CHIP_ERASE operation.
- **VM_BSY** – indicates the device is processing a voice macro. The device will not respond to a new audio command until this bit returns low.
- **CBUF_FUL** – indicates that the command buffer is full. No more commands can be queued for execution until this bit returns low.
- **CMD_BSY** – indicates the device is processing a command. Device will not respond to a new command until this bit returns low. If CMD_BSY=1 and CBUF_FUL=0 and VM_BSY=0, a new command will go into the command buffer and execute when the current command finishes. If CMD_BSY=1 and CBUF_FUL=1 or VM_BSY=1 any new audio command will be ignored and generate a command error. For erasing commands like ERASE_MSG@, ERASE_MEM and CHIP_ERASE, the user has to poll this bit to see if the erasing is done.

Whenever the ISD15C00 generates an interrupt the Interrupt Status register holds flags that indicate what type of interrupt was generated. These flags will remain set until a READ_INT command clears them and the interrupt pin.

Table 12-7 Interrupt Status Register Description

Interrupt Status Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PK_INT	MPT_ERR	WR_FIN	CMD_ERR	OVF_ERR	CMD_FIN	ADDR_ERR	FULL_ERR

The individual bits of the status register refer to the following conditions:

INT – an interrupt has been generated. The interrupt is cleared by the READ_INT command.

- **PK_INT** – Indicates a peak detection interrupt has occurred. Input peak detector can be configured to generate an interrupt when signal level exceeds a certain threshold.
- **MPT_ERR** – Indicates a memory protection error. Digital access attempted for protected memory.
- **WR_FIN** – indicates a digital write command has finished writing to the flash memory.
- **CMD_ERR** – an invalid command was sent to the device. Command was ignored because the command buffer was full, a voice macro was active or the device was not ready to respond to an erase command.
- **OVF_ERR** – This error is generated if host illegally tries to read or write data while RDY/BSYB pin is low. It is also generated if a digital read or write attempts to read or write past the end of memory.
- **CMD_FIN** – This bit indicates an interrupt was generated because a command finished executing. A CMD_FIN interrupt will be generated each time an audio play, record or voice macro finishes.
- **ADDR_ERR** – Indicates an address error. This bit will be set to one if a PLAY_MSG@ command is sent at a non-valid header, a REC_MSG@ is sent at a non-blank memory location or an ERASE_MSG command is sent to a sector that is not the beginning of message.
- **FULL_ERR** – Record Block is full. This bit will be set and an interrupt generated if a record command fills the memory.

12.3 DEVICE CONFIGURATION REGISTERS

The configuration of the ISD15100 is achieved by forty-eight configuration registers, CFG0-CFG2F as detailed below.

Please note that registers 0x19~0x1F have no default value, and user should configure these registers in both POI VM and PU VM to customized value or suggested initial value to avoid undesired consequences. See register 0x19 ~ 0x1F configuration for details. [3]

Table 12-8 CFG0 Register

CFG0 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SR[2:0]			CMP[4:0]				
011			00100				

Default 0x64:

- 4-bit ADPCM
- Ratio to Fs = 4

ISD provides a powerful software tool, Voice Prompt Editor, to help the user build their project and ease the configuration of the ISD15100.

Configuration register CFG0 controls the sample rate and compression algorithm during message record operations. It can also override sample rate setting for playback by setting bit 0 of CFG1 high. SR[2:0]=CFG0[7:5] controls the sample rate and CMP[4:0]=CFG0[4:0] controls the compression. An explanation of these follows below.

[3] Note: Register 0x1C and 0x1E are excluded because register 0x1C is read-only and register 0x1E doesn't exist.

Table 12-9 CFG0 Register Compression Type.

Compression Type	Bit rate (bits/sample)	CMP[4:0]	
		(Dec)	(Hex)
ADPCM	2	2	0x02
ADPCM	3	3	0x03
ADPCM	4	4	0x04
ADPCM	5	5	0x05
µ-Law	6	16	0x10
µ-Law	7	17	0x11
µ-Law	8	18	0x12
Dµ-Law	6	20	0x14
Dµ-Law	7	21	0x15
Dµ-Law	8	22	0x16
PCM	8	24	0x18
PCM	10	25	0x19
PCM	12	27	0x1B

Table 12-10 CFG0 Sample Rate Control

Ratio to Fs	Sample Rate (kHz) (for Fs=32kHz)	Code SR[2:0]	CFG0[7:0]	
			(Dec)	(Hex)
8	4	0	0	0x00
6	5.333	1	32	0x20
5	6.4	2	64	0x40
4	8	3	96	0x60
2.5	12.8	4	128	0x80
2	16	5	160	0xA0
1	32	6	192	0xC0

The current operational mode of the ISD15100 can also be queried by setting CFG1[4] and reading CFG0. Under this condition, rather than reading back the configuration register, the result will be current audio path sample rate and compression scheme.

Table 12-11 CFG1 Register

CFG1 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
FIFO Over-run	FIFO Under-run	-	CFG0_READ	LAT_ADC	NRMP	SRSIL	SRCFG

Default 0x00:

- Sample rate is set by the recorded audio header.
- Whenever a change in sample rate is detected between two consecutive messages, a period of silence is automatically inserted.
- If an audio playback finishes at a non-zero level the input to the signal path will be ramped to zero.
- The output from the ADC and AGC are NOT latched.
- A read of CFG0 will read the setting of the CFG0 register rather than the current operating mode of compression and sample rate.

Configuration register CFG1 controls how compressed audio is treated by the compression block:

- **SRCFG** – Forces the sample rate to be set by the CFG0 register by setting this bit to one, overriding any sample rate contained in the recorded audio header.
- **SRSIL** – Under normal circumstances, whenever a change in sample rate is detected between two consecutive messages a period of silence is automatically inserted. This is to prevent any transients in the signal path occurring as filter coefficients are changed. To turn off this silence insertion set this bit to one.
- **NRMP** – Under normal conditions, if an audio playback finishes at a non-zero level the input to the signal path will be ramped to zero. This prevents a DC offset appearing on the output. To turn this feature off, for instance if a small audio sample is being looped, set this bit to one.
- **LAT_ADC** – When this bit is high the output from the ADC and AGC are latched. It is used to ensure that the data from read-only registers CFGE, CFG10, CFG11, CFG12 and CFG13 are synchronized to the SPI clock. If LAT_ADC is low then these registers are updated under control of the internal clock and spurious read back is possible.
- **CFG0_READ** – When this bit is set, a read of CFG0 will result in the current operation mode of compression and sample rate rather than the setting of the CFG register. A write to CFG0 will still result in setting the register, but the contents of the register cannot be read back until CFG0_READ is set to zero.
- **FIFO Under-run** – This is a read only register, that when high indicates that the audio FIFO has under-run, that is audio data was not present when required by the signal path. This is a normal condition at the end of a play command when compression is active. It can be used during a SPI_DAC operation to check whether data sent to ISD15100 was corrupted. This signal is latched and is reset by writing a 1 followed by a 0 to CFG1[7], the FIFO Over-run bit.
- **FIFO Over-run** – When read, a high indicates that the audio FIFO has over-run, that is audio data from the signal path could not be processed fast enough to keep audio integrity and data was lost. This is a normal condition at the end of a record command when compression has finished. It can be used during a SPI_ADC operation to check whether data received from the ISD15100 was corrupted. This signal is latched and is reset by writing a 1 followed by a 0 to the register.

Table 12-12 CFG2 Register

CFG2 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
I^2S_IN	DECODE	SPI_IN	I^2S_OUT	DAC_OUT	PWM_OUT	ENCODE	SPI_OUT

Default 0x00:

- All digital paths are disabled.

Configuration register CFG2 controls how digital audio signal path is configured:

The I15100 Voice Prompt Editor provides a graphic view of the path configuration to help the user get a better understanding of the audio signal path and largely ease the path setting.

- **SPI_OUT** – Output signal data to SPI. SPI_OUT and ENCODE cannot be both on at the same time. If DECODE is selected, the signal path is bypassed and ISD15100 is ready for SPI playback operation. If DECODE is not set then the signal source is the audio path and a SPI ADC operation is selected. Use the SPI_PCM_READ command to read the audio data out the SPI interface.
- **ENCODE** – Used in conjunction with a record operation. When selected, signal data is routed to the Audio compressor for compression. If SPI_IN is also selected, the signal path is bypassed and becomes ready for an SPI record operation using the SPI_PCM_WRITE command.
- **PWM_OUT** – Output signal to PWM.
- **DAC_OUT** – Output signal to AUXOUT/AUDOUT
- **I^2S_OUT** – Output signal data to I^2S interface
- **SPI_IN** – Input data from SPI. SPI_IN and DECODE cannot be both on at the same time. If ENCODE is set, then an SPI record operation is selected. If not audio data is sent to the signal path for a SPI DAC operation. Use the SPI_PCM_WRITE command to send audio data to the ISD15100 from the SPI interface.
- **DECODE** – Used in conjunction with a play operation. When selected the signal path picks up data from the compressor and plays it to the corresponding outputs selected.
- **I^2S_IN** – Input data from I^2S. I^2S_IN and ADC_IN cannot be both on at the same time.

Table 12-13 CFG3 Register

CFG3 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLC[7:0]							

Default 0x00:

- 0 dB attenuation to the output signal volume

Configuration register CFG3 sets the output signal volume. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-14 CFG4 Register

CFG4 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				OFF_COMP	AGC_EN		ADC_IN

Default 0x00:

- Disable the ADC input to the digital signal path.
- Disable the Automatic Gain Control (AGC) for the ADC input.
- Disable offset compensation on the ADC input.

Configuration register CFG4 controls the digital signal path functions:

- **ADC_IN** – Enables the ADC input to the digital signal path.
- **AGC_EN** – This bit enables the Automatic Gain Control (AGC) for the ADC input.
- **OFF_COMP** – This bit enables offset compensation on the ADC input. When enabled any DC offset on the ADC input, whether from external sources or internal non-idealities is reduced to zero. Offset compensation is recommended for correct AGC performance on small input signals.

Table 12-15 CFG5 Register

CFG5 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PU_DAC	PU_ADC	PU_OP_SUM	PU_IP_SUM	PU_AUXIN	AUXIN_GAIN[1:0]		PU_ANAIN

Default 0x00:

- All blocks in the analog signal path are powered off.

Configuration register CFG5 controls the power up state of blocks in the analog signal path along with the gain of the AUXIN input:

- **PU_ANAIN** – Powers up the ANAIN input buffer.
- **AUXIN_GAIN**- Sets the gain of the AUXIN input buffer.
- **PU_AUXIN** – Powers up the AUXIN input buffer.
- **PU_IP_SUM** – Powers up the input summation amplifier (SUM1).
- **PU_OP_SUM** – Powers up the output summation amplifier (SUM2).
- **PU_ADC** – Powers up the analog-to-digital converter (ADC).
- **PU_DAC** – Powers up the digital-to-analog converter (DAC).

Table 12-16 AUXIN Gain Configuration

AUXIN_GAIN	
AUXIN_GAIN[1:0]	**Gain (dB)**
00	0
01	3
10	6
11	9

Table 12-17 CFG6 Register

CFG6 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AUX_SEL[1:0]		AUD_SEL[1:0]		-	PU_AUDOUT_I	PU_AUDOUT_V	PU_AUXOUT

Default 0x00:

- Input source to the AUDOUT buffer: ANAIN.
- Input source to the AUXOUT buffer: ANAIN.

Configuration register CFG6 controls the analog signal path functions:

- **PU_AUXOUT** – Powers up the AUXOUT output buffer.
- **PU_AUDOUT_V** – Powers up the AUDOUT output buffer, as a voltage output.
- **PU_AUDOUT_I** – Powers up the AUDOUT output buffer, as a current output.
- **AUD_SEL** – Selects the input source to the AUDOUT buffer.
- **AUX_SEL** – Selects the input source to the AUXOUT buffer.

Table 12-18 AUDOUT Source Selection.

AUD_SEL	
AUD_SEL[1:0]	**Source**
00	ANAIN
01	AUXIN
10	SUM2
11	DAC

Table 12-19 AUXOUT Source Selection

AUX_SEL	
AUX_SEL[1:0]	**Source**
00	ANAIN
01	AUXIN
10	SUM2
11	DAC

Table 12-20 CFG7 Register

CFG7 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	MIC_EN	AUD_IOUT_RMPDN	AUD_IOUT_RMPUP	OUT_SUM[1:0]		ADC_SEL[1:0]	

Default 0x00:

- Input source to the analog-to-digital converter (ADC): ANAIN.
- Input source to the SUM2 mixer: ANAIN.
- Disable the ramp up/down function on the current driver.
- ANAIN and ANAOUT are used as single ended MIC inputs, instead of differential MIC inputs.

Configuration register CFG7 controls the analog signal path functions:

- **ADC_SEL** – Selects the input source to the analog-to-digital converter (ADC).
- **OUT_SUM_SEL** – Selects the configuration of the SUM2 mixer.
- **AUD_IOUT_RMPUP** – Enables the ramp up function on the current driver. After powering up the current driver, a slow ramp is generated as an input to the current driver to prevent sudden transients on the output. This bit enables the ramp up function to ramp current from zero to center level.
- **AUD_IOUT_RMPDN** – Before powering down the current driver, this bit should be set to prevent fast transients. Setting this bit ramps the current driver zero current.
- **MIC_EN** – Setting this bit to 1 in conjunction with powering down the ANAIN input amplifier (**PU_ANAIN=0),** allows the use of pins ANAIN and ANAOUT as differential MIC inputs. In this mode, the ANAIN and ANAOUT pins become MIC+ and MIC- and allow a differential input to be applied to the ADC. The maximum level for this input is 1Vpp measured differentially. This configuration is designed to be used in conjunction with the AGC to amplify microphone signals while achieving good common mode rejection of supply noise. No mixing with AUXIN is possible in this mode.

Table 12-21 ADC Input Source Selection

ADC_SEL	
ADC_SEL[1:0]	**Source**
00	ANAIN
01	AUXIN
10	SUM1
11	N/A

Table 12-22 SUM2 Input Source Selection

OUT_SUM_SEL	
OUT_SUM_SEL[1:0]	**Source**
00	ANAIN
01	SUM1
10	AUXIN
11	N/A

Table 12-23 CFG8 Register

CFG8 Configuration Register				
Bit 7 - 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	MUTE_ADC_IN	MUTE_SUM2_MUX	MUTE_AUXOUT	MUTE_AUDOUT

Default 0x00:

- NOT mute on analog signal path.

Configuration register CFG8 controls the analog signal path functions:

- **MUTE_AUDOUT** –Mutes AUDOUT output.
- **MUTE_AUXOUT** –Mutes AUXOUT output.
- **MUTE_SUM2_MUX** –Mutes the SUM2_MUX input to the SUM2 summation block.
- **MUTE_ADC_IN** –Mutes the input to the ADC.

Bits 4-7 are unused and have no effect on the signal path.

Table 12-24 CFG9 Register

CFG9 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PWMF[3:0]				I^2S_L_IN	I^2S_R_IN	I^2S_L_OUT	I^2S_R_OUT

Default 0x00:

- Disable I^2S function.
- PWM nominal frequency is 256 kHz when master sample rate is 32 kHz.

Configuration register CFG9 controls the functionality of the I^2S audio interface:

- **I^2S_L_IN** – Enables I^2S input from the left (WS=0) channel to the signal path.
- **I^2S_R_IN** – Enables I^2S input from the right (WS=1) channel to the signal path.
- **I^2S_L_OUT** – Enables signal path output to the left (WS=0) I^2S channel.
- **I^2S_R_OUT** – Enables signal path output to the right (WS=1) I^2S channel.
- In addition to this basic functionality these bits are decoded to determine the whether mixing or feed-through occurs in the I^2S path. See I^2S section for details.
- **PWMF[3:0]** – Adjusts the nominal frequency of the PWM driver. This frequency is 1MHz/PWMF for all settings except 0, where frequency = 256kHz. Numbers are relative to a 32kHz master sample rate.

Table 12-25 I^2S Selection

I^2S Channel Selection	
CFG9[3:0]	**Description**
0000	No I^2S input or output selected
1111	Stereo Feed-through, left channel record.
10XX	Left channel in; can output to both/either
01XX	Right channel in can output to both/either.
1100, 1101, 1110	Left+Right mixed for record or either channel output.

Table 12-26 CFGB Register

CFGB Configuration Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC_MAXG[1:0]		AGC_REL[2:0]			AGC_ATK[2:0]		

Default 0x00:

- The attack rate of the gain of the AGC is 2.0 us per gain step.
- The release rate of the gain of the AGC is 0.063 ms per gain step.
- Maximum gain that the AGC will apply to the input signal is 28 dB.

Configuration register CFGB controls the functionality of the AGC:

The AGC aims to keep the recording volume constant, regardless of the input signal level. The AGC ramps down its gain when the recording volume attacks (volume increases); the AGC ramps up its gain when the recording volume releases (volume decreases).

- **AGC_ATK[2:0]** – Determines the attack rate of the gain of the AGC. This is the rate at which gain is reduced when the AGC output is larger than the target range. Attack time is the time it takes for the AGC gain to ramp down.
- **AGC_REL[2:0]** – Determines the release rate of the gain of the AGC. This is the rate at which gain is increased when the AGC output is below target range. Release time is the time it takes for the AGC gain to ramp up.
- **AGC_MAXG[1:0]** – Sets the maximum gain that the AGC will apply to the input signal.

Table 12-27 AGC Gain Attack and Release Configuration

AGC_ATK	
AGC_ATK[2:0]	**Step Time (us)**
0	2.0
1	3.9
2	7.8
3	15.6
4	31.3
5	62.5
6	125.0
7	250.0

AGC_REL	
AGC_REL[2:0]	**Step Time (ms)**
0	0.063
1	0.125
2	0.250
3	0.500
4	1.000
5	2.000
6	4.000
7	8.000

Table 12-28 AGC Maximum Gain

AGC Maximum Gain	
AGC_MAXG[1:0]	**Gain (dB)**
00	28
01	34
10	40
11	47

Table 12-29 CFGC Register

CFGC Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AGC_PKREL[1:0]		AGC_NG[2:0]			AGC_HOLD[2:0]		

Default 0x00:

- 0 ms delay before the AGC gain beginning to ramp up.
- The level of the noise gate for AGC gain control is -54 dBFS
- Release time of the input peak detector is 4 us.

Configuration register CFGC controls the functionality of the AGC:

- **AGC_HOLD[2:0]** – Determines the amount of time that the AGC gain is held constant after AGC output leaves target signal range. Hold time is the time delay before the AGC gain beginning to ramp up.
- **AGC_NG[2:0]** – Determines the level of the noise gate for AGC gain control. When the peak detector level falls below the noise gate no gain changes are applied. Level is referred to a full scale digital input which is 1Vpp at 0dB analog gain.
- **AGC_PKREL[1:0]** – Sets the release time of the input peak detector.

Table 12-30 AGC Gain hold and noise gate Configuration

AGC Hold time	AGC Noise Gate

AGC_HOLD [2:0]	Hold Time (ms)
0	0
1	4
2	16
3	32
4	128
5	256
6	512
7	1024

AGC_NG [2:0]	Gate Level (dBFS)	Gate Level (mVp)
0	-54	1.0
1	-51	1.4
2	-48	2.0
3	-45	2.8
4	-42	4.0
5	-39	5.6
6	-36	7.9
7	-33	11.2

Table 12-31 AGC Maximum Gain

AGC Peak Detector Release	
AGC_PKREL[1:0]	Step Time (us)
00	4
01	16
10	62.5
11	125

Table 12-32 CFGD Register

CFGD Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AGC_IG_EN	AGC_IG[6:0]						

Default 0x00:

- Disable the AGC initial gain setting. Initial gain the AGC is 0 dB.

Configuration register CFGD controls the functionality of the AGC:

- **AGC_IG[6:0]** – Allows the initial gain of the AGC to be set. This gain is applied anytime AGC_IG_EN=1 and AGC_EN=0.
- **AGC_IG_EN** – Enables the AGC initial gain setting feature. If AGC_IG_EN=0 then initial gain of the AGC is 0dB. If AGC is activated (AGC_EN=1) then gain will adjust according to the AGC algorithm. *Note: When AGC is disabled (AGC_EN=0) the last gain will continue to be applied to the ADC input. To reset the ADC gain back to 0dB user must write AGC_IG=8, AGC_IE_EN=1.

Table 12-33 AGC Initial Gain

AGC Initial Gain		
AGC_IG[6:0]	**Gain**	**Gain (dB)**
0	0	
1	0.016	-36
8	1	0
n	(n * n)/64	20*log(n*n/64)
120	225	47
127	252	48

Table 12-34 CFGE Register

CFGE Configuration Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	AGC_G[6:0]						

Configuration register CFGE is a read only register to query the AGC gain:

- **AGC_G[6:0]** – Is the current gain applied to the ADC input. This gain is (AGC_G * AGC_G)/64.

Table 12-35 CFGF Register

CFGF Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PK_DET_IE	PK_DET_LEV[6:0]						

Default 0x00:

- Disable the peak detection interrupt.

Configuration register CFGF controls the functionality of the peak detection interrupt:

- **PK_DET_LEV[6:0]** – Threshold level for the peak detection interrupt. When peak detector exceeds this limit an interrupt is generated.
- **PK_DET_IE** – Enables the peak detection interrupt.

Table 12-36 Peak Detector Interrupt Level

Peak Detector Interrupt Level		
PK_DET_LEV[6:0]	**Level (dBFS)**	**Level (mVp)**
0	-54.3	1
1	-48.2	1.9
8	-35.1	8.8
n	20log((n*64+63)/32767)	(n*64+63)/32767*500
120	-12.5	118
127	-12	125

Table 12-37 CFG10 Register

CFG10 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PK_DET_RD[7:0]							

Table 12-38 CFG11 Register

CFG11 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PK_DET_RD[15:8]							

Configuration register CFG10 and CFG11 are a read only registers to query the peak detector:

- **PK_DET_RD[15:0]** – Current value of the peak detector. For reliable read-back the ADC_LAT bit should first be set high to latch this value.

Table 12-39 CFG12 Register

CFG12 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADC_VAL[7:0]							

Table 12-40 CFG13 Register

CFG13 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADC_VAL[15:8]							

Configuration register CFG12 and CFG13 are a read only registers to query current output of the ADC converter:

- **ADC_VAL[15:0]** – Current value of the ADC converter. For reliable read-back the ADC_LAT bit should first be set high to latch this value.

Table 12-41 CFG14 Register

CFG14 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLB[7:0]							

Default 0x00:

- 0 dB attenuation to the volume control coming from the decompression block.

Configuration register CFG14 controls the volume level coming from the decompression block. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-42 CFG15 Register

CFG15 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VOLA[7:0]							

Default 0x00:

- 0 dB attenuation to the volume control coming from the I^2S or ADC.

Configuration register CFG15 controls the volume level coming from the I^2S or ADC input. Setting 0 has 0dB attenuation. Each subsequent step provides 0.25dB of attenuation.

Table 12-43 CFG16 Register.

CFG16 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AGC_GAIN[-1:-3]			INC	DEC	FAST_DEC	HOLD	NOISE

This is a read-only register that provides information on the performance of the AGC:

- **NOISE** – High if noise gate is active.
- **HOLD -** High if AGC gain hold is active.
- **FAST_DEC** – High if peak signal level is >90% causing a fast decrement of gain.
- **DEC** – High if peak signal level is > 81.25%FS causing a decrement of gain.
- **INC**- High if peak signal level is less than 80%FS causing gain to increment unless HOLD or NOISE is active.
- **AGC_GAIN[-1:-3]** – Additional bits of resolution of AGC_GAIN setting of CFGE.

Table 12-44 CFG17 Register

CFG17 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PLL_LOCK	RB_SPI	I²S_MM	I²S_ATT	DECODE	COMP_ACTIVE	UPDATE	IMM

Default 0x01:

- Turn off double buffering of configuration. Configuration is updated after each register byte is written.
- Disable the 3dB attenuation when left and right channel are mixed.
- I²S slave mode: ISD15100 accepts SCK and WS from a bus master.
- Monitor the RDY/BSYB handshake through the hardware pin.

Configuration register CFG17 controls how the configuration registers are applied:

- **IMM** – This bit set to one turns off double buffering of configuration. Thus configuration is updated after each register byte is written. Set to zero, configuration register setting is not made active until a one is written to the update bit.
- **UPDATE** – When a one is written to this bit and IMM bit is zero, configuration registers CFG0-CFG2F become active. In this way a path can be set up and applied at the same instant to prevent disturbance on the analog path. (Write Only)
- **COMP_ACTIVE –** Indicates that compression or decompression is active. (Read only).
- **DECODE** – Indicates that compressor is in decode mode. (Read Only)
- **I²S_MM** – Enables I²S master mode. With this bit set to one, the device generates I²S SCK and WS at 32fs.
- **I²S_ATT** – Enables 3dB of attenuation when left and right channels are mixed.
- **RB_SPI** – This bit is set if users wish to monitor the RDY/BSYB handshake through SPI status rather than the hardware pin. When set it ensures that when conducting DIG_WRITE, SPI_PCM_WRITE and SPI_SND_DEC commands that the RDY bit of the status register is latched on SPI byte boundaries for correct read back.
- **PLL_LOCK** – Indicates that the PLL is locked. If this bit is zero it indicates the PLL is attempting to lock on the input clock. (Read Only)

Table 12-45 CFG18 Register

CFG18 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ANA_ EN	MUTE_ SPK-	BTL_MO DE	SPK- _IN_SEL	PU_SPK -	MUTE_ SPK+	SPK+_IN_ SEL	PU_SPK +

Default 0x00:

- PWM is selected by default.

CFG18 controls the configuration of the two pins SPK+ and SPK-:

- **PU_SPK+** – Powers up buffer SPK+.
- **SPK+_IN_SEL** –
    - When BTL_MODE is set, SPK+_IN_SEL selects the source for the BTL output. When SPK+_IN_SEL is cleared, the source is AUDOUT MUX; when set, the source is the AUXOUT MUX. When BTL_MODE is cleared (separate outputs), SPK+_IN_SEL selects the source for SPK+ output only.
- **MUTE_SPK+ –** Mutes SPK+ output.
- **PU_SPK-** – Powers up buffer SPK-.
- **SPK-_IN_SEL** –
    - When BTL_MODE/ANA_EN is set, SPK-_IN_SEL is “don’t care”. When BTL_MODE is cleared, SPK-_IN_SEL selects the signal source for the SPK- pin. When SPK-_IN_SEL is cleared, the source is the AUDOUT MUX; when set, the source is the AUXOUT MUX.
- **BTL_MODE –**
    - When set, the speaker driver operates in the BTL (differential) mode for driving a speaker. When cleared, each speaker driver pins operates independently. The signal source can be the output of the AUXOUT MUX or the AUDOUT MUX.
- **MUTE_SPK- –** Mutes SPK- output.
- **ANA_EN** –
    - When set, the speaker driver operates in the analog mode. When cleared it operates in the digital mode (PWM). When operating in the digital mode, all remaining bits in CFG18 are “don’t care” and have no effect upon the operation. In the digital mode of operation, speaker driver is controlled by PWM_OUT (CFG2[2]).

The figure below shows an example of BTL setting from the AUX_MUX.

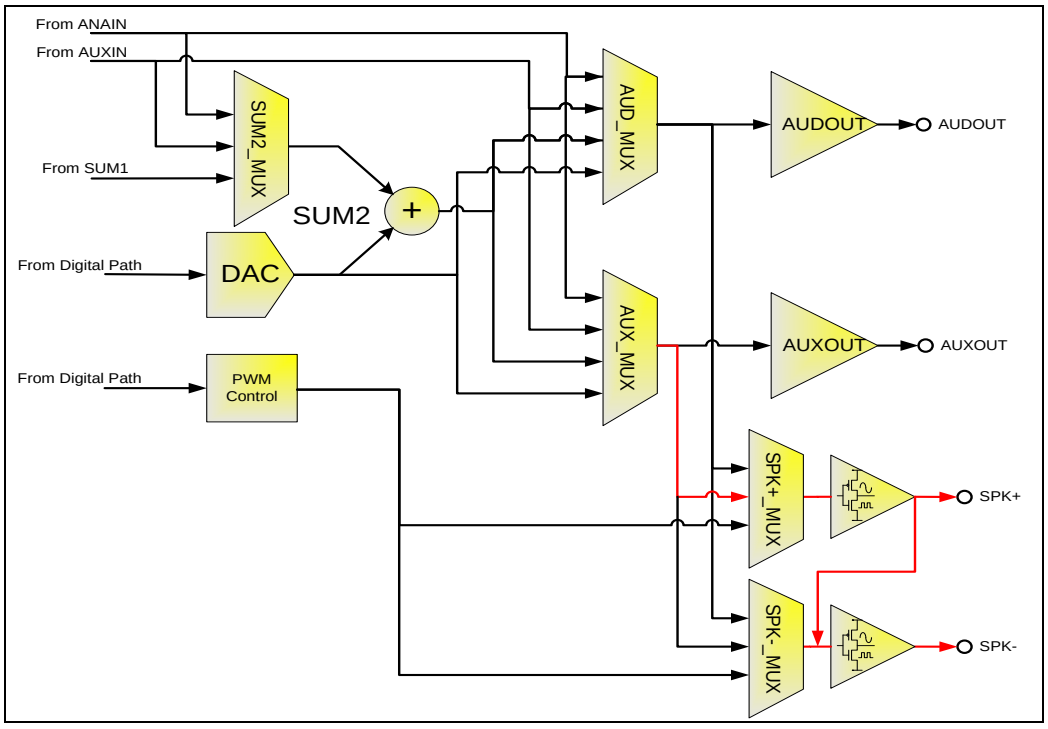


Figure 12-1 BTL from the AUX_MUX (the red line)

Table 12-46 CFG19 Register

CFG19 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 DOUT	GPIO6 DOUT	GPIO5 DOUT	GPIO4 DOUT	GPIO3 DOUT	GPIO2 DOUT	GPIO1 DOUT	GPIO0 DOUT

Default: N/A

- Suggested initial configuration value: 0x00.[4]

This register sets the value to output to GPIO when OE is 1.

[4] Note: This register should be configured in both POI VM and PU VM to customized value or suggested initial configuration value.

Table 12-47 CFG1A Register

CFG1A Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 OE	GPIO6 OE	GPIO5 OE	GPIO4 OE	GPIO3 OE	GPIO2 OE	GPIO1 OE	GPIO0 OE

Default: N/A

- Suggested initial configuration value: 0x00, set to input (output disabled).[3]

This register sets Output-Enable to GPIO

- 1: output enabled.
- 0: output disabled.

Table 12-48 CFG1B Register

CFG1B Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 PE	GPIO6 PE	GPIO5 PE	GPIO4 PE	GPIO3 PE	GPIO2 PE	GPIO1 PE	GPIO0 PE

Default: N/A

- Suggested initial configuration value: 0xFF, pull up/down enabled.[3]

This register sets Pull-up/down-Enable to GPIO

- 1: pull up/down enabled.
- 0: pull up/down disabled.

Table 12-49 CFG1C Register (Read Only)

CFG1C Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 DIN	GPIO6 DIN	GPIO5 DIN	GPIO4 DIN	GPIO3 DIN	GPIO2 DIN	GPIO1 DIN	GPIO0 DIN

This register monitors the GPIO input value.

Table 12-50 CFG1D Register

CFG1D Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7 PS	GPIO6 PS	GPIO5 PS	GPIO4 PS	GPIO3 PS	GPIO2 PS	GPIO1 PS	GPIO0 PS

Default: N/A

- Suggested initial configuration value: 0xFF, set to pull-up.[3]

This register selects Pull-up or pull-down when PE is 1.

- 1: pull up
- 0: pull down

Table 12-51 CFG1F Register

CFG1F Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO7/ SDI AF	GPIO6/ SCK AF	GPIO5/ WS AF	GPIO4/ SDO AF				

Default: N/A

- Suggested initial configuration value: 0x00.[3]

This register sets the alternate function of I2S.

- 1: set to GPIO
- 0: set to I2S

Table 12-52 CFG20 Register

CFG20 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R0[7:0] for PlayVP@Rn							

Table 12-53 CFG21 Register

CFG21 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R0[15:8] for PlayVP@Rn							

Table 12-54 CFG22 Register

CFG22 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R1[7:0] for PlayVP@Rn							

Table 12-55 CFG23 Register

CFG23 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R1[15:8] for PlayVP@Rn							

Table 12-56 CFG24 Register

CFG24 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R2[7:0] for PlayVP@Rn							

Table 12-57 CFG25 Register

CFG25 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R2[15:8] for PlayVP@Rn							

Table 12-58 CFG26 Register

CFG26 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R3[7:0] for PlayVP@Rn							

Table 12-59 CFG27 Register

CFG27 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R3[15:8] for PlayVP@Rn							

Table 12-60 CFG28 Register

CFG28 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R4[7:0] for PlayVP@Rn							

Table 12-61 CFG29 Register

CFG29 Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R4[15:8] for PlayVP@Rn							

Table 12-62 CFG2A Register

CFG2A Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R5[7:0] for PlayVP@Rn							

Table 12-63 CFG2B Register

CFG2B Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R5[15:8] for PlayVP@Rn							

Table 12-64 CFG2C Register

CFG2C Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R6[7:0] for PlayVP@Rn							

Table 12-65 CFG2D Register

CFG2D Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R6[15:8] for PlayVP@Rn							

Table 12-66 CFG2E Register

CFG2E Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R7[7:0] for PlayVP@Rn							

Table 12-67 CFG2F Register

CFG2F Configuration Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
R7[15:8] for PlayVP@Rn							

12.4 DEVICE IDENTIFICATION REGISTERS.

By sending the command READ_ID the device responds with a four byte identification. The first byte reports the 15C00 family version. The following three bytes are a JEDEC compliant code indicating the memory type. The first byte is the manufacturer code which is 0xEF for Winbond. The following byte is for memory type which is 0x30. The last byte is memory size according to the following table:

Table 12-68 JDEC Memory Size ID Byte

Capacity	Value
4Mb	13
8Mb	14
16Mb	15
32Mb	16
64Mb	17

13 SPI COMMANDS

The ISD15C00 provides SPI commands including: (1) 13 audio play and record commands, (2) 5 device status commands, (3) 4 digital commands, and (4) 6 device configuration commands.

The following section contains a list of all SPI commands and their function.

Table 13-1 SPI Commands

Instructions	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4 … Byte n	Description
PLAY_VP	0xA6	Index[15:8]	Index[7:0]			Play Voice Prompt Index
PLAY_VP@Rn	0xAE	n = 0 …7				Play Voice Prompt; Index @ Rn
EXE_VM	0xB0	Index[15:8]	Index[7:0]			Execute voice macro Index
REC_MSG	0x38					Record message
REC_MSG@	0x3A	A[23:16]	A[15:8]	A[7:0]		Record message starting at address A.
PLAY_MSG@	0x3C	A[23:16]	A[15:8]	A[7:0]	Off[15:8], Off[7:0]	Play message starting at address A offset by OFF sectors.
PLAY_SIL	0xA8	LEN[7:0]				Play silence for LEN*32ms
STOP	0x2A					STOP current playback or record operation.
ERASE_MSG@	0x3E	A[23:16]	A[15:8]	A[7:0]		Erase message starting at address A.
SPI_PCM_WRITE	0xAA	D0[7:0]	D0[15:8]	D1[7:0]	D1[15:8] …Dn[7:0] Dn[15:8]	Send 16 bit PCM audio data [low-byte, high-byte] to I15C00 via SPI interface.
SPI_PCM_READ	0xAC	D0[7:0]	D0[15:8]	D1[7:0]	D1[15:8] …Dn[7:0] Dn[15:8]	Receive 16 bit PCM audio data [low-byte, high-byte] from I15C00 via SPI interface.
SPI_SND_DEC	0xC0	D0[7:0]	D1[7:0]	D2[7:0]	D3[7:0] …Dn[7:0]	Send compressed audio data to I15C00 via SPI interface for decoding.
SPI_RCV_ENC	0xC2	D0[7:0]	D1[7:0]	D2[7:0]	D3[7:0] …Dn[7:0]	Receive compressed (encoded) audio data from I15C00 via SPI interface.
READ_STATUS	0x40	XX	XX	XX	…	Query status of I15C00.
READ_INT	0x46	XX	XX	XX	…	Query status and clear interrupt flags of I15C00.
RD_MSG_ADD	0x42	XX	XX	XX	XX, XX	Query message address details of audio record. Returns start address A and current sector length LEN.
RD_MSG_LEN	0x44	XX	XX			Query current sector length LEN of current playback or record operation.
READ_ID	0x48	XX	XX	XX	XX	Read device ID of 15C00.

Instructions	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4 … Byte n	Description
DIG_READ	0xA2	A[23:16]	A[15:8]	A[7:0]	XX, … XX	Read digital data from address A.[5]
DIG_WRITE	0xA0	A[23:16]	A[15:8]	A[7:0],	D0[7:0], … Dn[7:0]	Write digital data from address A.[4]
ERASE_MEM	0x24	SA[23:16]	SA[15:8]	SA[7:0]	EA[23:16], EA[15:8], EA[7:0]	Erase sectors of memory from sector containing SA to sector containing EA.
CHIP_ERASE	0x26	0x01				Initiate a mass erase of memory.
PWR_UP	0x10					Power up I15C00
PWR_DN	0x12					Power down I15C00
SET_CLK_CFG	0xB4	CFG_CLK[7:0]				Set clock configuration register.
RD_CLK_CFG	0xB6	XX				Read clock configuration register.
WR_CFG_REG	0xB8	REG[7:0]	D0[7:0], ...Dn[7:0]			Write data D0..Dn to configuration register(s) starting at configuration register REG.
RD_CFG_REG	0xBA	REG[7:0]	XX, ...XX			Read configuration register(s) starting at configuration register REG.

Each command will be accepted if certain conditions are met as in the following table, or a CMD_ERR interrupt will be generated and the command ignored.

Table 13-2 Commands vs. Status

Instructions	Op Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PD	DBUF_RDY	INT	RM_FUL	-	VM_BSY	CBUF_FUL	CMD_BSY
PLAY_VP	0xA6	0	***1***	x	x	-	0	0	x
PLAY_VP@Rn	0xAE	0	***1***	x	x	-	0	0	x
EXE_VM	0xB0	0	***1***	x	x	-	0	0	0
REC_MSG	0x38	0	***1***	x	0	-	0	0	x
REC_MSG@	0x3A	0	***1***	x	0	-	0	0	x
PLAY_MSG@	0x3C	0	***1***	x	x	-	0	0	x
PLAY_SIL	0xA8	0	***1***	x	x	-	0	0	x
STOP	0x2A	0	***1***	x	x	-	x	x	x
ERASE_MSG@	0x3E	0	***1***	x	x	-	0	0	0
SPI_PCM_WRITE	0xAA	0	***1***	x	x	-	x	x	x
SPI_PCM_READ	0xAC	0	***1***	x	x	-	x	x	x
SPI_SND_DEC	0xC0	0	***1***	x	x	-	0	0	0

[5] Note: For Digital Read/Write operations, ISD15C00 can only support up to 64Mbits. For all other SPI operations, this limitation does not apply.

Instructions	Op Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PD	DBUF_RDY	INT	RM_FUL	-	VM_BSY	CBUF_FUL	CMD_BSY
SPI_RCV_ENC	0xC2	0	***1***	x	x	-	0	0	0
READ_STATUS	0x40	x	x	x	x	-	x	x	x
READ_INT	0x46	x	x	x	x	-	x	x	x
RD_MSG_ADD	0x42	0	***1***	x	x	-	x	x	x
RD_MSG_LEN	0x44	0	***1***	x	x	-	x	x	x
READ_ID	0x48	0	***1***	x	x	-	x	x	x
DIG_READ	0xA2	0	***1***	x	x	-	x	x	x
DIG_WRITE	0xA0	0	***1***	x	x	-	x	x	x
ERASE_MEM	0x24	0	***1***	x	x	-	0	0	0
CHIP_ERASE	0x26	0	***1***	x	x	-	0	0	0
PWR_UP	0x10	***1***	0	x	x	-	x	x	x
PWR_DN	0x12	0	***1***	x	x	-	x	x	x
SET_CLK_CFG	0xB4	0	***1***	x	x	-	0	0	0
RD_CLK_CFG	0xB6	0	***1***	x	x	-	x	x	x
WR_CFG_REG	0xB8	0	***1***	x	x	-	x	x	x
RD_CFG_REG	0xBA	0	***1***	x	x	-	x	x	x

13.1 AUDIO PLAY AND RECORD COMMANDS

This section describes the 13 audio commands that can be sent to the device.

13.1.1 Play Voice Prompt

PLAY_VP				
Byte Sequence:	Host controller	0xA6	*Index*[15:8]	Index[7:0]
	ISD15C00	Status Byte	Status Byte	Status Byte
Description:	Play Voice Prompt *Index*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command initiates a play of a pre-recorded voice-prompt. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. After completion of playback, the device will generate an interrupt. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once playback is finished a CMD_FIN interrupt will be generated.

13.1.2 Play Voice Prompt @Rn, n = 0 ~ 7

PLAY_VP@Rn				
Byte Sequence:	Host controller	0xAE	*n = 0 ~ 7*	
	ISD15C00	Status Byte	Status Byte	
Description:	Play Voice Prompt, *Index@Rn*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command is same as PlayVP except that the 16bit index is stored in Rn, n = 0 ~ 7.

- R0[7:0] = CFG20, R0[15:8] = CFG21
- R1[7:0] = CFG22, R1[15:8] = CFG23
- R2[7:0] = CFG24, R2[15:8] = CFG25
- R3[7:0] = CFG26, R3[15:8] = CFG27
- R4[7:0] = CFG28, R4[15:8] = CFG29
- R5[7:0] = CFG2A, R5[15:8] = CFG2B
- R6[7:0] = CFG2C, R6[15:8] = CFG2D
- R7[7:0] = CFG2E, R7[15:8] = CFG2F

13.1.3 Execute Voice Macro

EXE_VM				
Byte Sequence:	Host controller	0xB0	*Index*[15:8]	Index[7:0]
	ISD15C00	Status Byte	Status Byte	Status Byte
Description:	Play voice macro *Index*			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback is finished.			

This command initiates the execution of a pre-recorded voice group. After completion of the voice macro the device will generate a CMD_FIN interrupt. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once voice macro execution is finished a CMD_FIN interrupt will be generated.

13.1.4 Record Message

REC_MSG				
Byte Sequence:	Host controller	0x38		
	ISD15C00	Status Byte		
Description:	Initiates a managed record at first available location in memory.			

Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when recording complete. FULL_ERR when device fills available memory.

This command initiates a record operation. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. If device is or becomes full, an interrupt is generated and the FULL_ERR bit of the interrupt status register is set. Recording is terminated by issuing a STOP command. After the operation is complete the begin address of the message can be read, along with the number of sectors recorded, with the READ_MSG_ADDR command.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory becomes full while recording a FULL_ERR interrupt will be generated. If device was full before the record was sent then a FULL_ERR interrupt will be generated and READ_MSG_ADDR will return a length of zero. When a record is terminated by a stop command a CMD_FIN interrupt will be generated once the recording process is complete.

13.1.5 Record Message at Address

REC_MSG@					
Byte Sequence:	Host controller	0x3A	A[23:16]	A[15:8]	A[7:0]
	ISD15C00	Status Byte	Status Byte	Status Byte	Status Byte
Description:	Initiate a managed record starting at sector address A/4096				
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when recording complete. FULL_ERR when device fills available memory. ADDR_ERR if invalid address sent.				

This command initiates a- record operation starting at a specified address. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. If device is or becomes full, an interrupt is generated and the FULL_ERR bit of the interrupt status register is set. Recording is terminated by issuing a STOP command. After the operation is complete the begin address of the message can be read, along with the number of sectors recorded out with the READ_MSG_ADDR command.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. If memory becomes full while recording a FULL_ERR interrupt will be generated. If device was full before the record was sent then a FULL_ERR interrupt will be generated and READ_MSG_ADDR will return a length of zero. If the address sent is not a blank sector then an ADDR_ERR interrupt is generated. When a record is terminated by a stop command a CMD_FIN interrupt will be generated once the recording process is complete.

13.1.6 Play Message at Address

PLAY_MSG@							
Byte Sequence:	Host controller	0x3C	A[23:16]	A[15:8]	A[7:0]	OFF[15:8]	OFF[7:0]
	ISD15C00	Status Byte	Status Byte	Status Byte	Status Byte	Status Byte	Status Byte
Description:	Initiate a managed record starting at sector address A/4096 + OFF						

Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when playback complete. ADDR_ERR if invalid address sent.

This command initiates a play of a recorded message starting at a specified address, with a specified sector offset. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. If an address is sent that is not a valid message an error interrupt is generated with the ADDR_ERR bit set. Playback can be terminated by issuing a STOP command. After completion of playback, the device will generate an interrupt. This command can be used to randomly access a message at any 4K sector boundary by sending the appropriate offset. The bottom 12 bits of the start address are ignored as messages must begin at a 4Kbyte sector boundary. If command is sent with less than five bytes of data the command is ignored.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once playback is finished a CMD_FIN interrupt will be generated. If the address sent is not a beginning of message sector then an ADDR_ERR interrupt will be generated. If the offset is greater than the message length then an ADDR_ERR interrupt will be generated.

13.1.7 Play Silence

PLAY_SIL				
Byte Sequence:	Host controller	0xA8	*LEN*[7:0]	
	ISD15C00	Status Byte 0	Status Byte 0	
Description:	Play silence for LEN*32ms			
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when silence playback complete.			

This command plays a period of silence to the signal path. Before execution of command a valid signal path must be set up and the device must have space in the audio command buffer. After completion, the device will generate an interrupt. The length of silence played is determined by the data byte, LEN, sent. Silence is played in 32ms increments (at signal path sampling frequency of 32kHz), total silence played is LEN*32ms.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0 and CBUF_FUL=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If command is terminated after the command byte is sent no interrupt will be generated. Once silence play is finished a CMD_FIN interrupt will be generated.

13.1.8 Stop Command

STOP				
Byte Sequence:	Host controller	0x2A		
	ISD15C00	Status Byte		
Description:	Stop current audio command and flush command buffer.			
Interrupt Generation:	Command itself does not generate interrupt, only those commands that it is stopping.			

This command stops any current audio command active in the ISD15C00. If a PLAY_MSG@, PLAY_VP, EXE_VM or PLAY_SIL command is active playback is stopped immediately. If a REC_MSG command is active recording is stopped at the next available byte boundary. The STOP command flushes the audio command buffer, that is any command queued in the buffer when a STOP is issued will not be executed. When device has finished the active command a CMD_FIN interrupt will be generated. STOP will not stop an ERASE_MSG or ERASE_MEM operation. If there is no active command then STOP will have no effect.

13.1.9 Erase Message at Address

ERASE_MSG@					
Byte Sequence:	Host controller	0x3E	A[23:16]	A[15:8]	A[7:0]
	ISD15C00	Status Byte	Status Byte	Status Byte	Status Byte
Description:	Erase message starting at sector address A/4096				
Interrupt Generation:	CMD_ERR if not accepted. CMD_FIN when erase complete. ADDR_ERR if invalid address sent.				

This command erases the message starting at the specified address. The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If address sent is not a beginning of message sector an ADDR_ERR interrupt is generated. Upon completion of command CMD_FIN interrupt is generated. While the device is erasing no other commands will execute. If a PLAY or REC is sent it is queued in the command buffer and will not execute until the erase is finished. If a DIG_RD or DIG_WR command is sent to the device, RDY/BSYB pin will hold off any data transfer until the ERASE_MSG@ has completed.

13.1.10 SPI Write PCM Data

SPI_PCM_WRITE							
Byte Sequence:	Host controller	0Xaa	D0[7:0]	D0[15:8]	….	Dn[7:0]	Dn[15:8]
	ISD15C00	Status Byte					
Description:	Write audio data via SPI interface.						
Interrupt Generation:	OVF_ERR if RDY/BSY violated.						

This command allows the user to send audio data, in 16bit PCM format, down the SPI interface for feed-through or recording. Before execution of command a valid signal path must be set up.

If recording data (SPI record), then: (1) signal path must be set up for SPI input to the compressor. (2) A valid record command is then sent (3) followed by the SPI_PCM_WRITE command. Multiple SPI_PCM_WRITE commands can be issued to write data to the ISD15C00. (4) To finish recording a STOP command is sent and device will respond with a CMD_FIN interrupt. If a memory overflow occurs during the operation a FULL_ERR interrupt will be generated and no more data will be accepted. RDY/BSYB pin will handshake dataflow if device cannot compress and write data at the rate sent down the SPI interface.

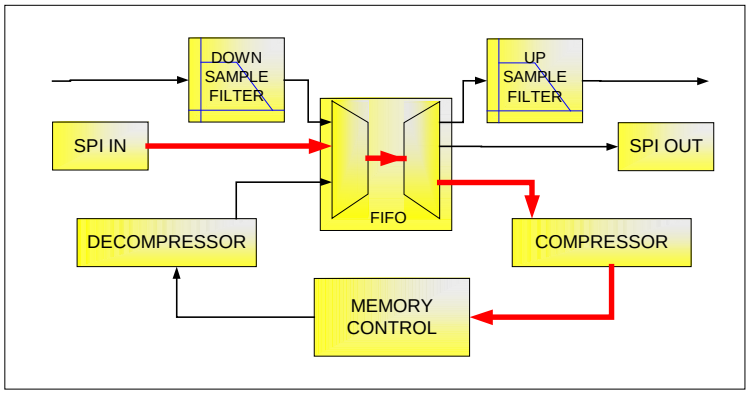


Figure 13-1 SPI Record

If sending audio data to the analog outputs (SPI feed-through), then: (1) the path must be set up for SPI input to the signal path. (2) A SPI_PCM_WRITE command is then sent. Multiple SPI_PCM_WRITE commands can be issued to write data to the ISD15C00. (3) To finish sending audio data a STOP command is sent and device will respond with a CMD_FIN interrupt. RDY/BSYB pin will handshake dataflow to the sample rate set by the audio configuration register. If host cannot keep up with data rate audio will be corrupt. Once audio data is sent, raise SSB high and device will continue to play zero samples out the signal path until reconfigured or more data is sent.

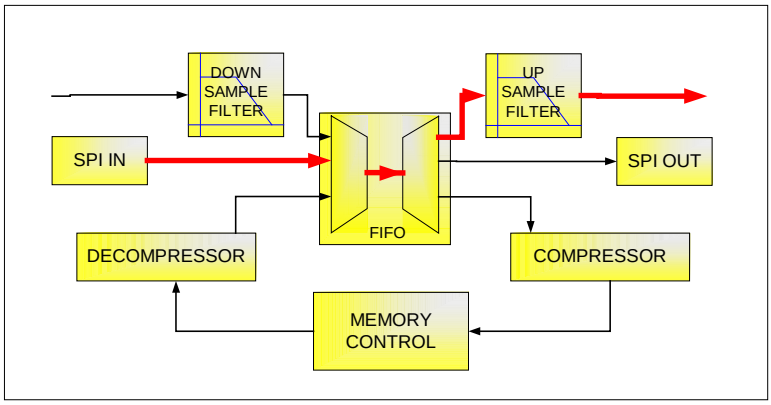


Figure 13-2 SPI Feed-through

The RDY/BSYB pin will go low whenever the internal FIFO is full. If no path or record operation is set up then RDY/BSYB pin will not return high until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated.

13.1.11 SPI Read PCM Data

SPI_PCM_READ							
Byte Sequence:	Host controller	0xAC					
	ISD15C00	Status Byte	D0[7:0]	D0[15:8]	….	Dn[7:0]	Dn[15:8]
Description:	Read audio data via SPI interface.						

Interrupt Generation:	OVF_ERR if RDY/BSY violated.

This command allows the user to receive audio data, in 16bit PCM format, from the SPI interface for feed-through or playback. Before execution of command a valid signal path must be set up.

If receiving audio data from memory (SPI playback), then: (1) signal path must be set up for SPI output from the compressor. (2) A valid play command is then sent; valid play command includes PlayMsg@, PlayVP, and ExeVM. (3) Followed by the SPI_PCM_READ command. Multiple SPI_PCM_READ commands can be sent. (4) To finish receiving data a STOP command is sent and device will generate a CMD_FIN interrupt.

When the end of message is reached a CMD_FIN interrupt will be generated and zero will be sent as data. If the valid play command in step (2) is ExeVM, then a CMD_FIN interrupt will be generated at the end of voice macro.

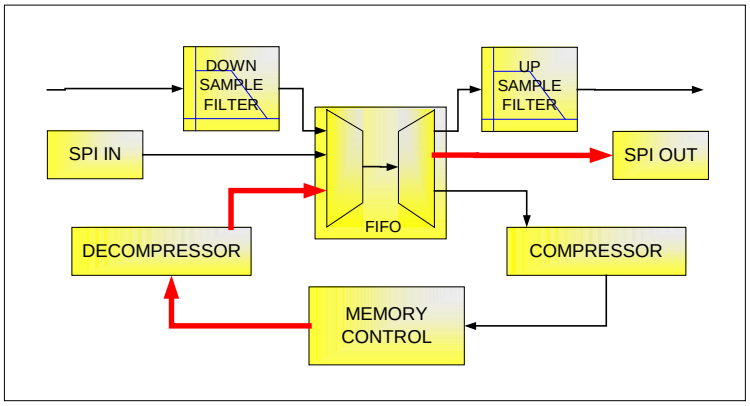


Figure 13-3 SPI Playback

If reading audio data from the analog inputs (feed-through SPI) then: (1) the path must be set up for SPI output from the signal path. (2) A SPI_PCM_READ command is then sent. Multiple SPI_PCM_READ commands can be sent. (3) To finish receiving data a STOP command is sent and device will generate a CMD_FIN interrupt. RDY/BSYB pin will handshake dataflow to the sample rate set by the audio configuration register. If host cannot keep up with data rate, audio will be corrupt.

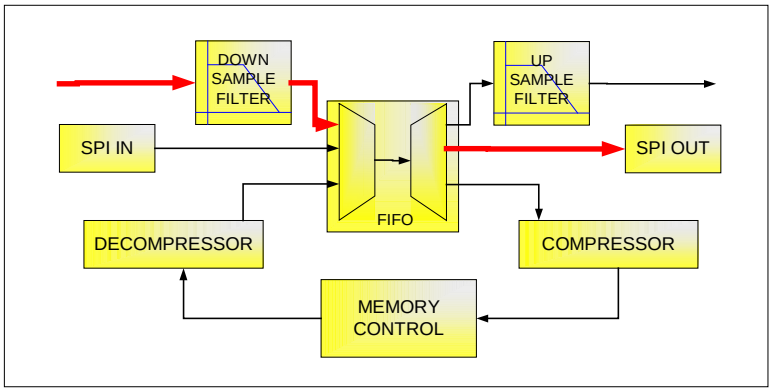


Figure 13-4 Feed-through SPI

The RDY/BSYB pin will go low whenever the internal FIFO is empty. If no path or playback operation is set up then RDY/BSYB pin will be low until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated.

13.1.12 SPI Send Compressed Data to Decode

SPI_SND_DEC						
Byte Sequence:	Host controller	0xC0	D0[7:0]	D1[7:0]	….	Dn[7:0]
	ISD15C00	Status Byte				
Description:	Write compressed audio data via SPI interface.					
Interrupt Generation:	OVF_ERR if RDY/BSYB violated.					

This command allows the user to send compressed audio data, in a byte formatted bit stream, down the SPI interface to the de-compressor and signal path. Before execution of command (1) a valid signal path must be set up. Valid paths are similar to a standard playback. (2) Multiple SPI_SND_DEC commands can be issued to send data to the ISD15C00. (3) To finish decoding a STOP command is sent and device will respond with a CMD_FIN interrupt. RDY/BSYB pin will handshake dataflow if device cannot accept any further data for decompression. If host cannot keep up with data rate audio output will be corrupted.

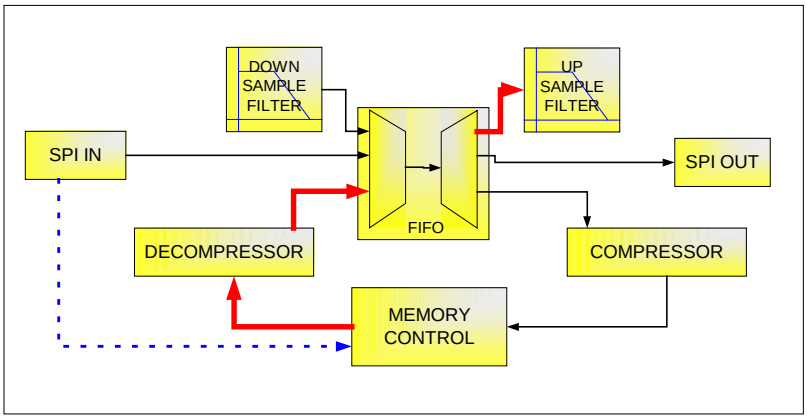


Figure 13-5 SPI Send Compressed Data to Decode

The RDY/BSYB pin will go low whenever the internal FIFO is full. If no path set up to accept audio data then RDY/BSYB pin will not return high until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated. The SPI_SND_DEC command is accepted if no current play or record operation is active. If command is not accepted a CMD_ERR interrupt will be generated. It is possible to perform digital memory operations between SPI_SND_DEC operations, however care must be taken to maintain the required data rate to avoid audio corruption.

13.1.13 SPI Receive Encoded Data

SPI_RCV_ENC

Byte Sequence:	Host controller	0xC2				
	ISD15C00	Status Byte	D0[7:0]	D1[7:0]	….	Dn[7:0]
Description:	Read compressed audio data via SPI interface.					
Interrupt Generation:	OVF_ERR if RDY/BSYB violated.					

This command allows the user to receive compressed audio data, in a byte formatted bit stream, from the SPI interface for use or storage outside the ISD15C00. Before execution of command (1) a valid recording signal path must be set up such that compressor is active. (2) Multiple SPI_RCV_ENC commands can be sent to receive compressed data from the ISD15C00. (3) To finish receiving data a STOP command is sent and device will generate a CMD_FIN interrupt.

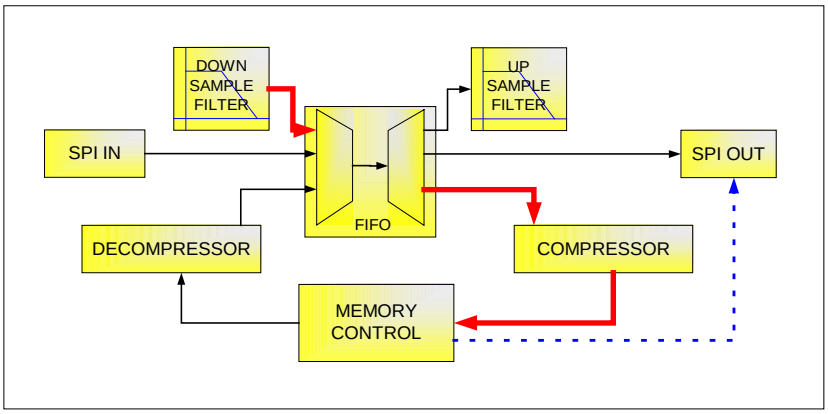


Figure 13-6 SPI Received Encoded Data

RDY/BSYB pin will handshake dataflow to the sample rate and compression bit rate set by the audio configuration register. If host cannot keep up with data rate compressed audio will be corrupt.

The RDY/BSYB pin will go low whenever the internal FIFO is empty. If no path is set up then RDY/BSYB pin will be low until command is terminated. If RDY/BSYB is ignored then an OVF_ERR interrupt is generated. The SPI_RCV_ENC command is accepted if no current play or record operation is active. If command is not accepted a CMD_ERR interrupt will be generated. It is possible to perform digital memory operations between SPI_RCV_ENC operations, however care must be taken to maintain the required data rate to avoid audio corruption.

13.2 DEVICE STATUS COMMANDS.

This section describes the 5 status commands that can be sent to the device.

13.2.1 Read Status

Powered up:

READ_STATUS			
Byte Sequence:	Host controller	0x40	0xXX
	ISD15C00	Status Byte	Interrupt Status Byte
Description:	Query device status.		

Powered down:

READ_STATUS			
Byte Sequence:	Host controller	0x40	0xXX
	ISD15C00	Status Byte 80h	00h
Description:	Query device status.		

This command queries the ISD15C00 device status. For details of device status see Section 12.2. If device is powered up, the two status bytes will be repeated for each two dummy bytes sent to the SPI interface. If device is powered down, only one status byte 80h shows up to the SPI interface at the same time the command is sent. This command is always accepted.

13.2.2 Read Interrupt

READ_INT				
Byte Sequence:	Host controller	0x46	0xXX	
	ISD15C00	Status Byte	Interrupt Status Byte	
Description:	Query device status and clear interrupt flags.			

This command queries the ISD15C00 device status and clears any pending interrupts. After this command the hardware interrupt line will return inactive. The INT bit of the status register along with any status error bits will return inactive.

This command is accepted whenever device is powered up.

13.2.3 Read Recorded Message Address Details

RD_MSG_ADD							
Byte Sequence:	Host controller	0x42	X	X	X	X	X
	ISD15C00	STATUS0	A[23:16]	A[15:8]	A[7:0]	LEN[15:8]	LEN[7:0]
Description:	Reports the start sector address A/4096 of current message and length, LEN, in 4kByte sectors						

This interrogates the status of the last or current audio record command. It returns the start address so that the user can address a message for playback and also returns the number of sectors that the message has used. It should be issued immediately after a record is initiated to correctly get retrieve the message start address and current length of message. After a STOP command or overflow condition, data is valid for final message length after CMD_BSY has returned low and before a subsequent audio command is issued.

13.2.4 Read Message Length

RD_MSG_LEN				
Byte Sequence:	Host controller	0x44	0xXX	0xXX
	ISD15C00	Status Byte	LEN[15:8]	LEN[7:0]
Description:	Read number of sectors played by current PLAY command.			

This command returns the number of sectors played by the current PLAY_MSG@ command, or recorded by the current REC_MSG command. This command is used to determine the offset position of the currently playing/recording message. It can be used to resume the playback of a message at a particular sector. For instance, if a PLAY_MSG(SA, 0) command was sent to start playback of a message from SA then a STOP was sent during playback of the third sector of the message, then RD_MSG_LEN would return LEN=3. A subsequent PLAY_MSG(SA,2) command would restart the playback from the beginning of the sector where playback was stopped, that is send PLAY_MSG(SA, LEN-1). Now, if a STOP was issued after an additional three sectors of playback (message is now playing the sixth sector), RD_MSG_LEN would return LEN=6.

13.2.5 Read I15C00 ID

READ_ID						
Byte Sequence:	Host controller	0x48	0xXX	0xXX	0xXX	0xXX
	ISD15C00	Status Byte	PART_ID	MAN_ID	MEM_TYPE	DEV_ID
Description:	Return memory ID of external memory					

This command queries the ISD15C00 to returns four bytes to indicate the I15C00 family member and the manufacturer, size and type of external memory of the device. The four bytes returned are:

PART_ID – Identifies which 15C00 family member.

MAN_ID – Manufacturer ID, which is 0xEF for Winbond.

MEM_TYPE – Memory type, which is 0x30.

DEV_ID – Device ID indicates the memory size as the table below.

Capacity	Value
4Mb	13
8Mb	14
16Mb	15
32Mb	16
64Mb	17

13.3 DIGITAL MEMORY COMMANDS.

This section describes the 4 digital data commands that can be sent to the device. Digital commands are ones that read, write or erase data directly in the flash memory through a separate interface than the audio data command interface. Digital memory commands other than erase, can occur simultaneously with audio memory commands.

13.3.1 Digital Read

DIG_READ								
	Host controller	0xA2	A[23:16]	A[15:8]	A[7:0]	0xXX	…	0xXX

Byte Sequence:	ISD15C00	Status	Status	Status	Status	D0	…	Dn
Description:	Initiates a digital read of memory from address A[23:0].							
Interrupt Generation:	ADDR_ERR if memory protected or RDY/BSYB violated. OVF_ERR if read past end of array.							

This command initiates a read of flash memory from address A[23:0]. Following the three address bytes, data can be read out of memory in a sequential manner. The RDY/BSYB pin is used to control flow of data. If RDY/BSYB pin goes low, transfer must be paused until RDY/BSYB pin returns high. The user should check RDY/BSYB pin before every byte is sent/read including the command and address bytes. As many bytes of data as required can be read, command is terminated by raising SSB high, finishing the SPI transaction. If an attempt is made to read past the end of memory, status byte will be read back.

The command will always be accepted and RDY/BSYB pin will go low until any active digital memory command is complete. If a digital read is attempted in read protected memory, status byte will be read back and an ADDR_ERR interrupt will be generated. If a read past the end of memory is attempted an OVF_ERR interrupt will be generated. If RDY/BSYB is violated then zero data will be read back and an ADDR_ERR interrupt will be generated.

Please note that for ISD15C00 Digital Read operation can only support up to 64M bits. User should avoid trying to read memory beyond 64Mbit boundary.

13.3.2 Digital Write

DIG_WRITE								
Byte Sequence:	Host controller	0xA0	A[23:16]	A[15:8]	A[7:0]	D0	…	Dn
	ISD15C00	Status	Status	Status	Status	Status	…	Status
Description:	Initiates a digital write to memory from address A[23:0].							
Interrupt Generation:	ADDR_ERR if memory protected or RDY/BSYB violated. OVF_ERR if write past end of array.							

This command initiates a write to flash memory from address A[23:0]. Following the three address bytes, data can be written to memory in a sequential manner. The RDY/BSYB pin is used to control flow of data. If RDY/BSYB pin goes low, transfer must be paused until RDY/BSYB pin returns high. The user should check RDY/BSYB pin before every byte is sent including the command and address bytes. As many bytes of data as required can be written, command is terminated by raising SSB high, finishing the SPI transaction.

The command will always be accepted and RDY/BSYB pin will go low until any active digital memory command is complete. If a digital write is attempted in write protected memory, data will be ignored and an ADDR_ERR interrupt will be generated. If a write is attempted past the end of memory an OVF_ERR interrupt will be generated. If RDY/BSYB is violated then data will ignored and an ADDR_ERR interrupt will be generated. Once the SPI transaction has ended the ISD15C00 will finish the flash write operation. When this operation is complete the ISD15C00 will generate a WR_FIN interrupt. While device is actively writing to flash memory the CMD_BSY bit will be active.

Please note that for ISD15C00 Digital Write operation can only support up to 64M bits. User should avoid trying to write memory beyond 64Mbit boundary.

13.3.3 Erase Memory

ERASE_MEM

Byte Sequence:	Host controller	0x24	SA[23:16]	SA[15:8]	SA[7:0]	EA[23:16]	EA[15:8]	EA[7:0]
	ISD15C00	Status	Status	Status	Status	Status	Status	Status
Description:	Erases memory from sector containing SA to sector containing EA.							
Interrupt Generation:	ADDR_ERR if memory protected. CMD_ERR if device is busy. CMD_FIN when erase operation complete.							

This erases memory from the sector containing start address SA to the sector containing end address EA. The minimum erase block of external memory is a 4kByte sector.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory is write protected an ADDR_ERR interrupt is generated. Upon completion of erase a CMD_FIN interrupt is generated.

While the device is erasing no other commands will execute. If a PLAY or REC is sent it is queued in the command buffer and will not execute until the erase is finished. If a DIG_RD or DIG_WR command is sent to the device, RDY/BSYB pin will hold off any data transfer until the ERASE_MEM has completed.

When ERASE_MEM is in progress, the Status bit 0 CMD_BSY goes high. Users could poll the status to see if the erasing is done.

13.3.4 Chip Erase

CHIP_ERASE			
Byte Sequence:	Host controller	0x26	0x01
	ISD15C00	Status Byte	Status Byte
Description:	Initiate a mass erase of memory.		
Interrupt Generation:	CMD_ERR if device is busy and cannot accept command. CMD_FIN when erase operation complete.		

This erases the entire contents of the external memory.

The command will be accepted if status bits PD=0, DBUF_RDY=1, VM_BSY=0, CBUF_FUL=0 and CMD_BSY=0. If any of these conditions are not met then a CMD_ERR interrupt will be generated and the command ignored. If memory is mass erase protected an ADDR_ERR interrupt is generated. Upon completion of erase a CMD_FIN interrupt is generated.

While the device is erasing no other commands will execute. If a PLAY or REC is sent it is queued in the command buffer and will not execute until the erase is finished. If a DIG_RD or DIG_WR command is sent to the device, RDY/BSYB pin will hold off any data transfer until the CHIP_ERASE has completed.

When CHIP_ERASE is in progress, the Status bit 0 CMD_BSY goes high. Users could poll the status to see if the erasing is done.

13.4 Device Configuration Commands

This section describes 6 commands used to configure the ISD15C00. These commands are used to:

Set up the clocking regime of the device including clock source and setting the master sample rate.

Configure the audio signal path.

Configure the compression and sample rate for message recording.

The signal path, compression and sample rate configuration are controlled by forty-eight bytes of configuration register. These forty-eight bytes can be written individually or in a continuous sequential manner. These configuration registers are double buffered such that a new configuration can be loaded and only set active when the user desires.

13.4.1 PWR_UP – Power up

PWR_UP				
Byte Sequence:	Host controller	0x10		
	ISD15C00	Status		…
Description:	Powers up device and initiates the power up sequence.			

This command powers up the device. If device already powered up this command has no effect. If powered down, then the internal power up sequence is initiated. If the PU voice macro is present this is executed, otherwise the device defaults to power up the internal oscillator. When power up is complete the PD bit of the status register will go low and the RDY bit high. Until this event no other commands will be accepted by the ISD15C00.

A formal power-up procedure is as follows:

- Send PWR_UP command.
- Poll Status until bit-6 DBUF_RDY goes high, which means ready.
- Poll Status until bit-2 VM_BSY goes low, which means voice macro 1 finishes.

13.4.2 PWR_DN – Power Down

PWR_DN				
Byte Sequence:	Host controller	0x12		
	ISD15C00	Status		…
Description:	Powers down the device after any active commands finish			

This command powers down the device. If the device is currently executing a command the device will powers down when the command finishes. If sent while recording without a STOP command sent first then device will record until full then power down. If playing or executing a voice macro, device will power down after playback is finished. The PWR_DN command will not generate an interrupt. PWR_DN has executed when PD bit of status goes high.

13.4.3 SET_CLK_CFG – Set Clock Configuration Register

SET_CLK_CFG				
Byte Sequence:	Host controller	0xB4	CFG_CLK[7:0]	
	ISD15C00	Status Byte	Status Byte	

Description:	Loads clock configuration register.

This sets the clock configuration register. The part reconfigures the clock and PLL configuration and waits for stable clock conditions before accepting new commands. When the configuration is changed, CMD_BSY will go high until clock configuration is complete. No new commands should be sent until the device status shows device not busy. This command does not generate an interrupt.

13.4.4 RD_CLK_CFG – Read Clock Configuration Register

This reads the clock configuration register.

RD_CLK_CFG				
Byte Sequence:	Host controller	0xB6	0xXX	
	ISD15C00	Status Byte	CFG_CLK[7:0]	
Description:	Reads clock configuration register.			

13.4.5 WR_CFG_REG – Write Configuration Register

WR_CFG_REG						
Byte Sequence:	Host controller	0xB8	REG[7:0]	D0	…	Dn
	ISD15C00	STATUS0			…	
Description:	Loads configuration register CFG[REG] with D0. Data bytes 1..n can be sent to load CFG[REG+1] with D1 to CFG[REG+n] with Dn.					

This command loads configuration registers starting at the address specified. If multiple data bytes are sent, additional configuration registers are loaded. See Section 12.3 for details on configuration registers. There are forty-eight configuration registers in the ISD15C00, REG0 – REG2F.

13.4.6 RD_CFG_REG – Read Configuration Register

RD_CFG_REG						
Byte Sequence:	Host controller	0xBA	REG[7:0]	X	…	X
	ISD15C00	STATUS0		D0	…	Dn
Description:	Reads configuration register CFG[REG] and outputs to SPI as D0. Data bytes 1..n can be read sequentially from CFG[REG+1] to CFG[REG+n].					

This command reads the configuration register starting at the address specified. If multiple data bytes are sent, additional configuration registers are read.

See Section 12.3 for details on configuration registers.

14 ELECTRICAL CHARACTERISTICS

14.1 ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS) [1]

CONDITIONS	VALUES
Junction temperature	130^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pins	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Power supply voltage to ground potential	-0.3V to +5.0V

[1] *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

14.2 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) [1]	+2.7V to +3.6V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 3.6V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] $V_{DD} = V_{CCA} = V_{CCD} = V_{CCPWM}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSPWM}$

14.3 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.7		3.6	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1mA
INTB Output Low Voltage	V_{OH1}			0.4	V	
Record Current	I_{DD_Record}			40	mA	V_{DD}= 3.6V, No load, Sampling freq = 16 kHz
Playback Current	$I_{DD\_Playback}$			30	mA	
Standby Current	I_{SB}		1	10	µA	V_{DD}= 3.6V
Input Leakage Current	I_{IL}			±1	µA	Force V_{DD}

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated

14.4 AC PARAMETERS

14.4.1 Internal Oscillator

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Internal Oscillator with internal reference	F_{INT}	-10%	2.048 MHz	+10 %	MHz	Vdd = 3V. At room temperature
Internal Oscillator with external resistor [1]	F_{Ext}	-5%	2.048 MHz	+5%	MHz	With 1% precision resistor, 80k-ohm. Vdd = 3V. At room temperature

Notes:
[1] Characterization data shows that frequency deviation is +/- 5% across temperature and voltage ranges.

14.4.2 Inputs

ANAIN & MICIN

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
ANAIN Input Voltage	V_{ANAIN}		10-1000		mV	Peak-to-Peak[2]
ANAIN Feed Back Resistance	$R_{ANA(FB)}$	40		100	KΩ	
MICIN Input Voltage	V_{MICIN}		5-500		mV	Peak-to-Peak[2]

Notes: [1] Conditions V_{DD}=3V, T_{AB}=25°C unless otherwise stated
[2] Depends on Gain Setting

AUXIN

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
AUXIN Input Voltage	V_{AUXIN}		1000		mV	Peak-to-Peak[2]
Gain from AUXIN to AUXOUT/ANAOUT	$A_{AUXIN\ GAIN}$		0 to 9		dB	4 Gain Steps of 3db each
AUXIN Gain Accuracy	$A_{AUXIN\ (GA)}$	-0.5		+0.5	dB	
AUXIN Input Resistance	R_{AUXIN}		20-40		KΩ	Depending on AUXIN Gain Setting

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated.
[2] With 0db Gain setting.

14.4.3 Outputs

AUXOUT

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SINAD, AUXIN to AUXOUT	$SINAD_{AUXIN\_AUXOUT}$		80		dB	Load 5K[2][3]
SINAD, ANAIN to AUXOUT	$SINAD_{ANAIN\_AUXOUT}$		80		dB	Load 5K[2][3]
PSRR	$PSRR_{AUXOUT}$		-40		dB	[4]
DC Bias	V_{BIAS_AUXOUT}			1.2	V	
Minimum Load Impedance	$R_{L(AUXOUT)}$	5			KΩ	
Maximum Load Capacitance	$C_{L(AUXOUT)}$			0.1	nF	

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
[3] All measurements are C-message weighted.
[4] Measured with 1KHz, 100 mVpp sine wave applied to V_{CCA} pins.

SS

AUDOUT

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SINAD, AUXIN to AUDOUT[5]	$SINAD_{AUXIN\_AUDOUT}$		80		dB	Load 5K[2][3]
SINAD, ANAIN to AUDOUT[5]	$SINAD_{ANAIN\_AUDOUT}$		80		dB	Load 5K[2][3]
PSRR[5]	$PSRR_{AUDOUT}$		-40		dB	[4]
DC Bias[5]	V_{BIAS_AUDOUT}			1.2	V	
Minimum Load Impedance[5]	$R_{L(AUDOUT)}$	5			KΩ	
Maximum Load Capacitance[5]	$C_{L(AUDOUT)}$			0.1	nF	
Output Current [6]	I_{AUDOUT}	0	3	6	mA	[2][6]

Notes: [1] Conditions V_{cc}=3V, T_A=25°C unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
[3] All measurements are C-message weighted.
[4] Measured with 1Khz, 100 mVpp sine wave applied to V_{CCA} pins.
[5] Configured as AUDOUT(Voltage Output).
[6] Configured as AUDOUT(Current Output).

SPEAKER OUTPUTS

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SNR, AUXIN to SPK+/SPK-	SNR_{AUXIN_SPK}		60		dB	Load 150Ω [2][3]
SNR, ANAIN to SPK+/SPK-	SNR_{ANAIN_SPK}		60		dB	Load 150Ω [2][3]
Output Power	P_{OUT_SPK} VCC=3.0			360	mW	Load 8Ω [2]
			62.5		mW	Load 8Ω[4] [5]
THD, AUXIN to SPK+/SPK-	THD %		<1%			Load 8Ω [2]
Minimum Load Impedance	$R_{L(SPK)}$	4	8		Ω	

Notes:
[1] Conditions V_{CC}=3V, T_A=25°C unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0dB gain setting to PWM output.
[3] All measurements are C-message weighted.
[4] Full scale 1K sine wave as input, playback from memory with 0dB gain setting to BTL output.
[5] 2 Vpp 1KHz signal applied at AUXIN/ANAIN with 0dB gain setting to BTL output.

SPEAKER OUTPUT POWER

Conditions: V_{CCD} = 3.3V, 16KHz sample rate, 12bit PCM, T_A = +25°C, 1kHz signal

PARAMETER	SYMBOL	MODE	MIN	TYP[1]	MAX	UNITS	CONDITIONS
Output Power	P_{OUT_SPK}	Class-D PWM		350		mW	@ 3.3V, Load 8Ω, 0.4% THD
				420		mW	@ 3.6V, Load 8Ω, 0.4% THD
				520		mW	@ 3.3V, Load 4Ω, 0.8% THD
				620		mW	@ 3.3V, Load 4Ω, 0.8% THD
		Class-AB BTL		63		mW	Load 8Ω, 0.1% THD[1]
				125		mW	Load 4Ω, 0.1% THD[1]

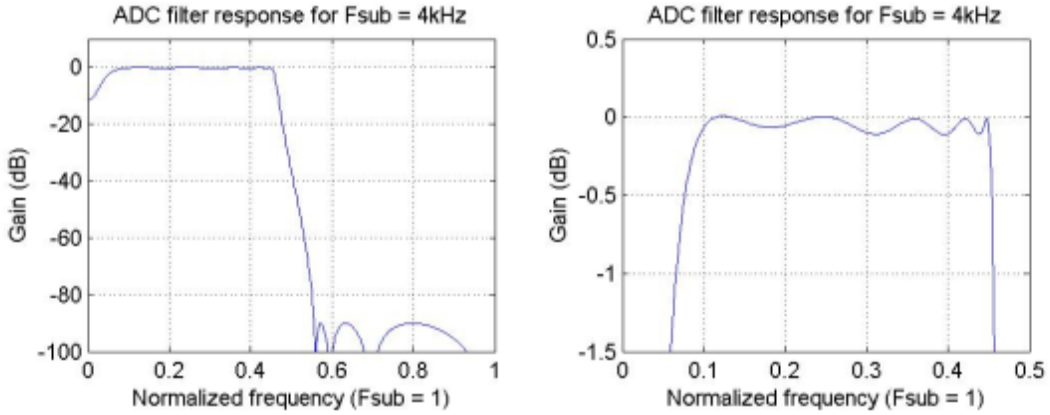
Notes:
[1] CLASS AB BTL is fixed referenced from bandgap, independent from V_{CCA}.

14.4.4 ADC and DAC Frequency Responses

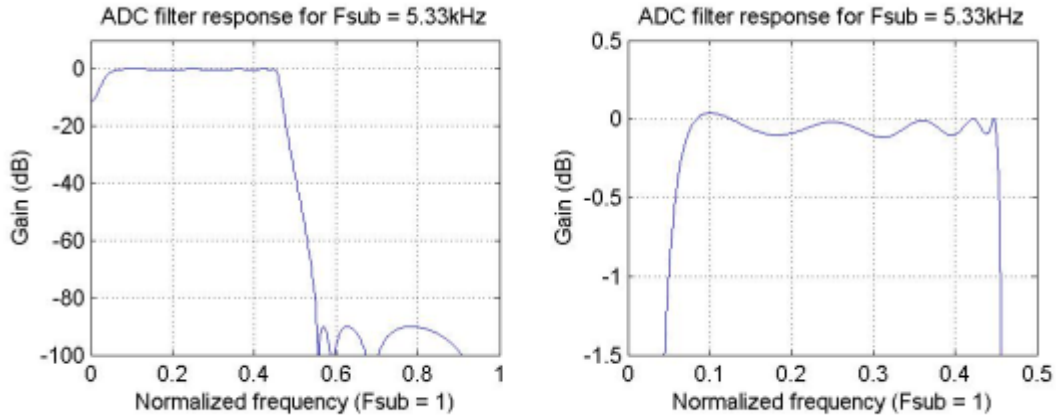
The following graphs show the frequency responses of the record path for analog or digital audio inputs. The data presented is for a master sample rate Fs=32kHz. For other values of Fs, Fsub scales accordingly.

There is a built-in high-pass filter with cutoff 200Hz following the ADC filter. The graphs below show a combined effect.

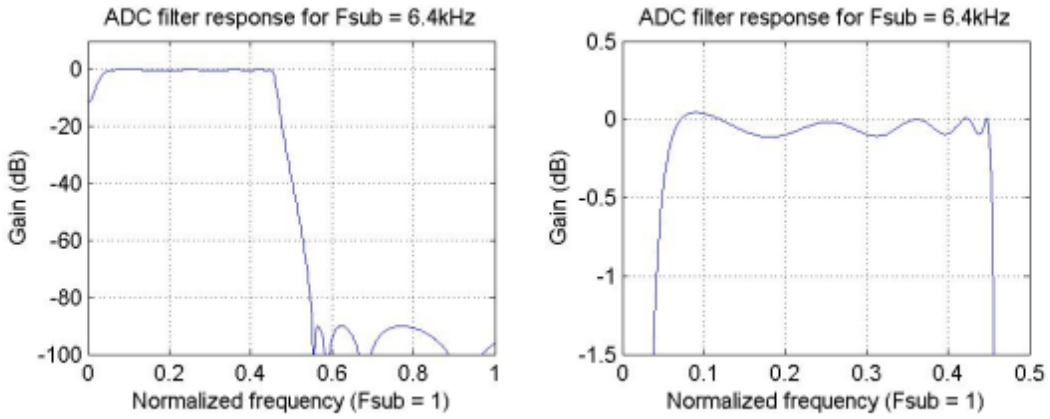
Record Frequency Response Fs = 32kHz, Fsub = 4kHz



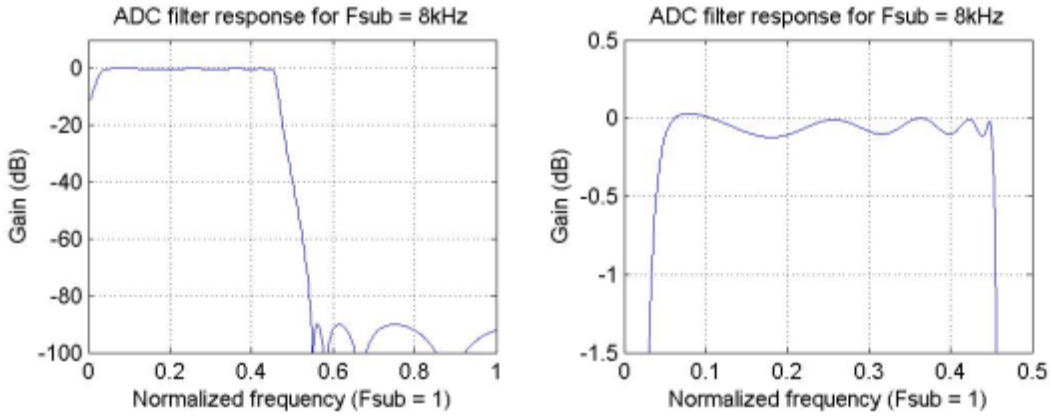
Record Frequency Response Fs = 32kHz, Fsub = 5.33kHz



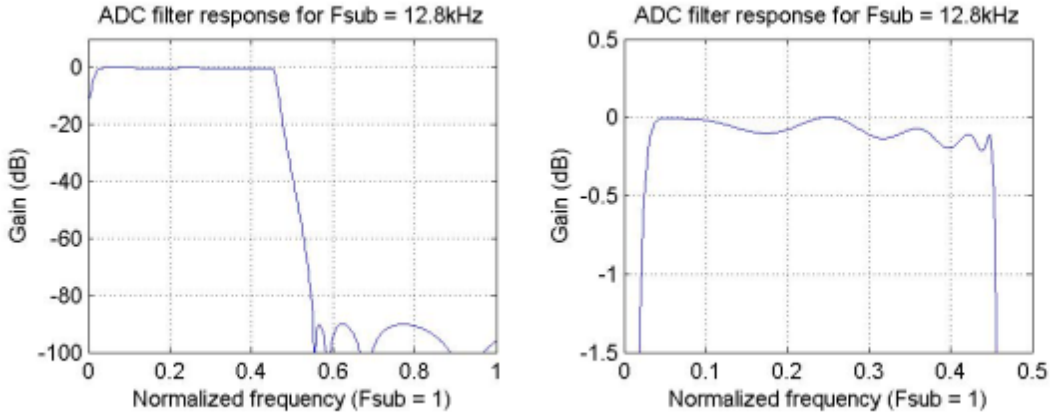
Record Frequency Response Fs = 32kHz, Fsub = 6.4kHz



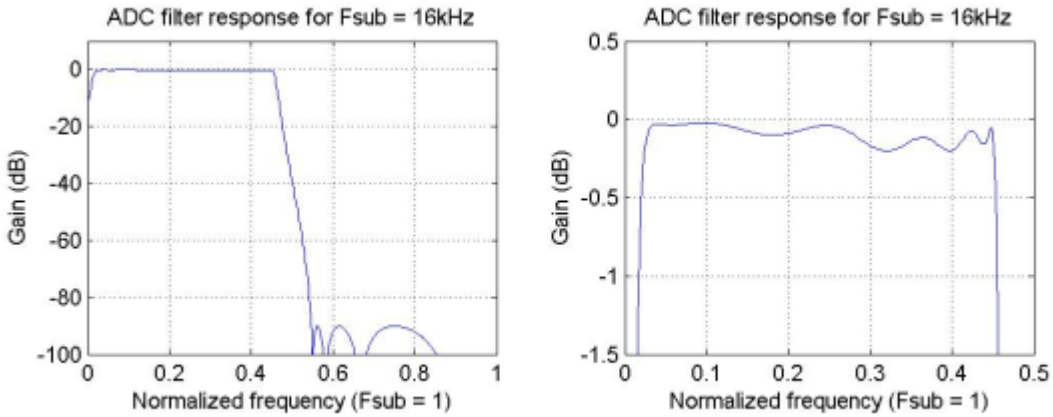
Record Frequency Response Fs = 32kHz, Fsub = 8kHz



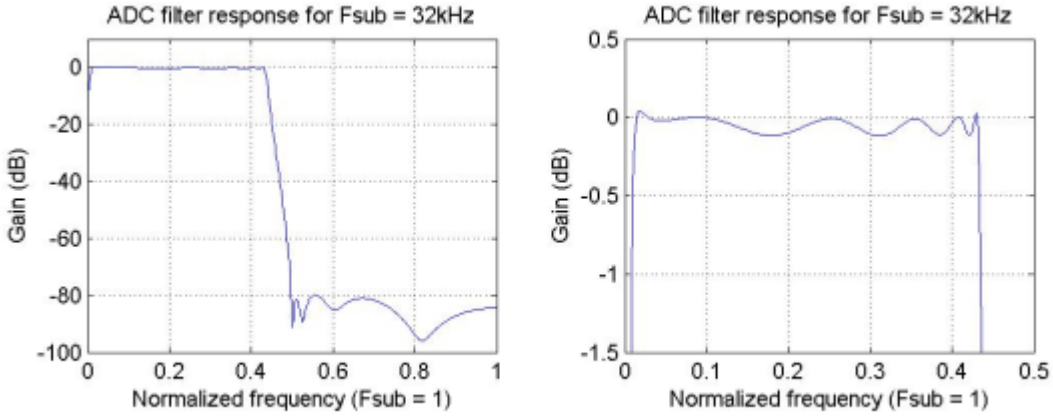
Record Frequency Response Fs = 32kHz, Fsub = 12.8kHz



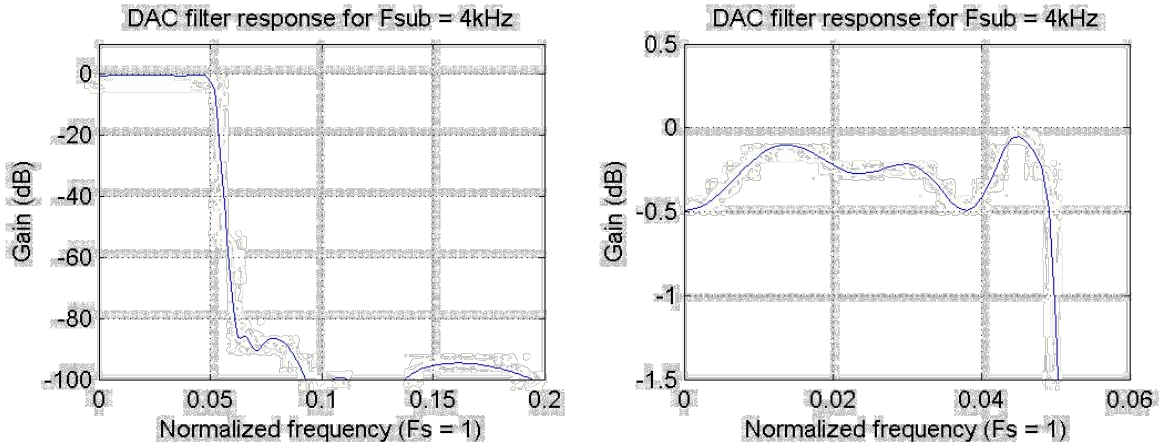
Record Frequency Response Fs = 32kHz, Fsub = 16kHz



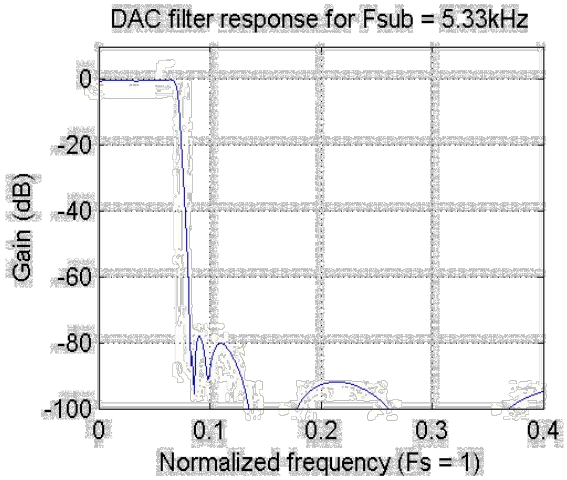
Record Frequency Response Fs = 32kHz, Fsub = 32kHz

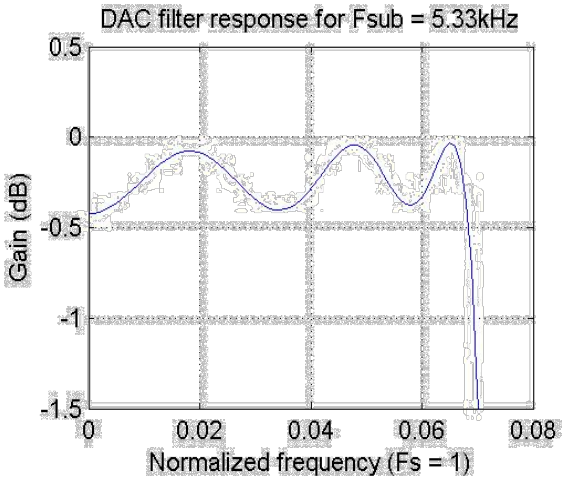


Playback Frequency Response Fs = 32kHz, Fsub = 4kHz

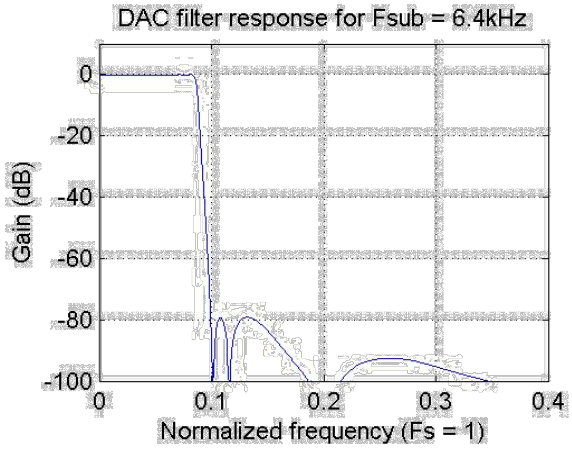


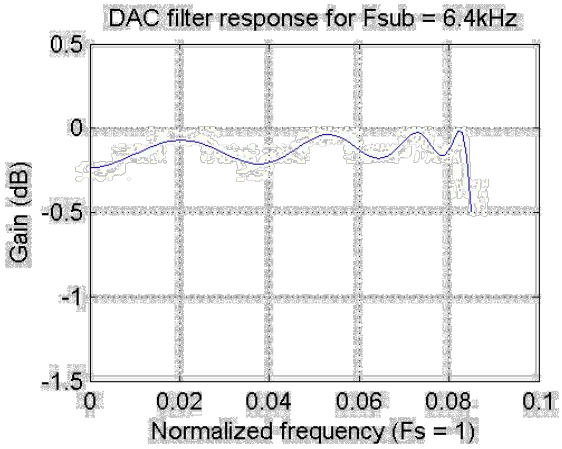
Playback Frequency Response Fs = 32kHz, Fsub = 5.33kHz



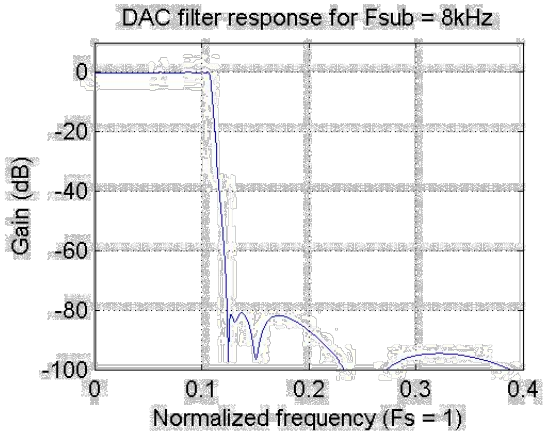


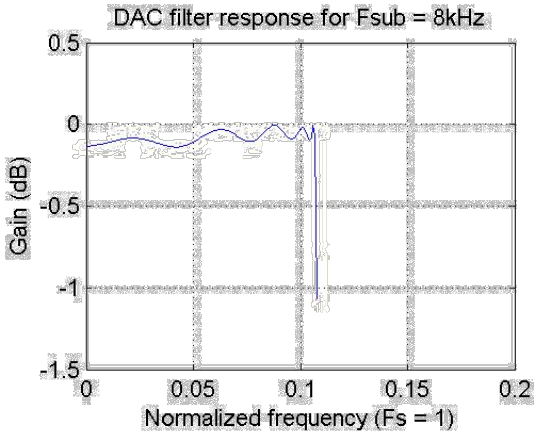
Playback Frequency Response Fs = 32kHz, Fsub = 6.4kHz



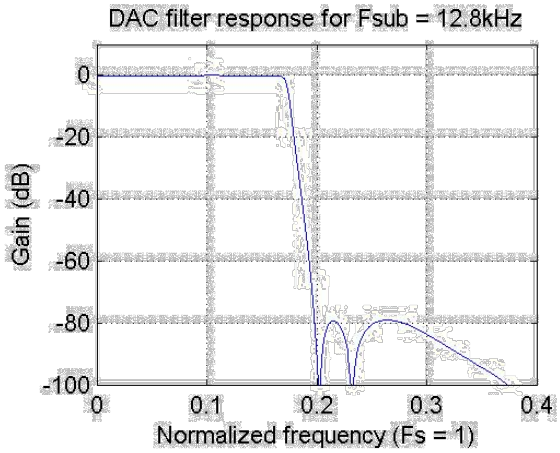


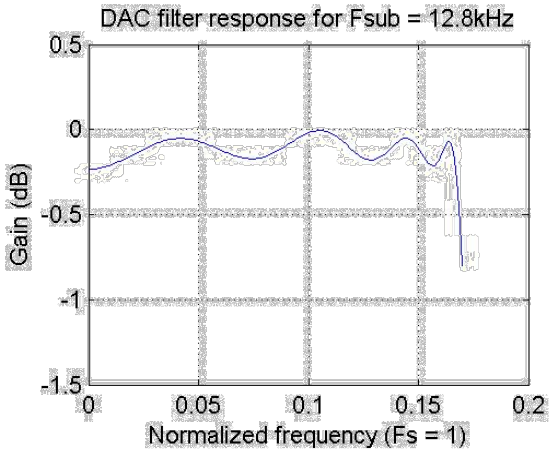
Playback Frequency Response Fs = 32kHz, Fsub = 8kHz



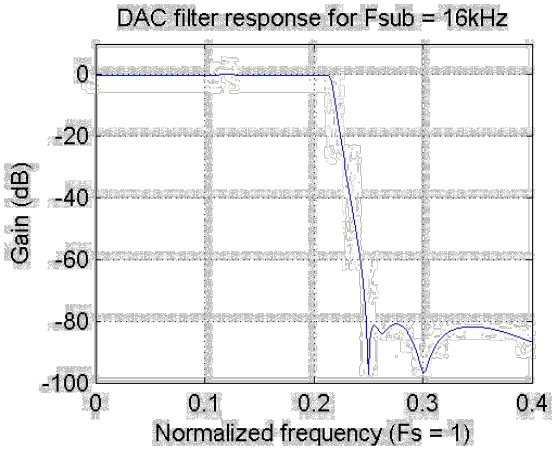


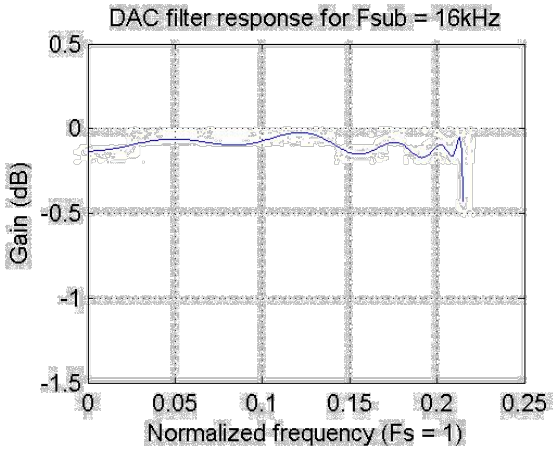
Playback Frequency Response Fs = 32kHz, Fsub = 12.8kHz



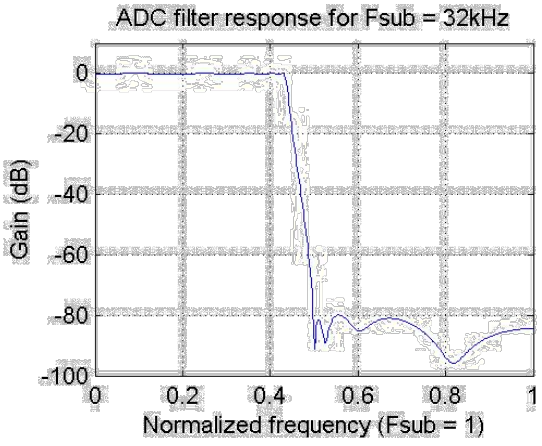


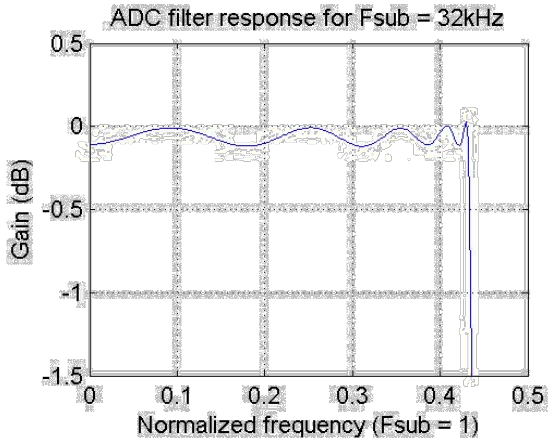
Playback Frequency Response Fs = 32kHz, Fsub = 16kHz





Playback Frequency Response Fs = 32kHz, Fsub = 32kHz





14.4.5 SPI Timing

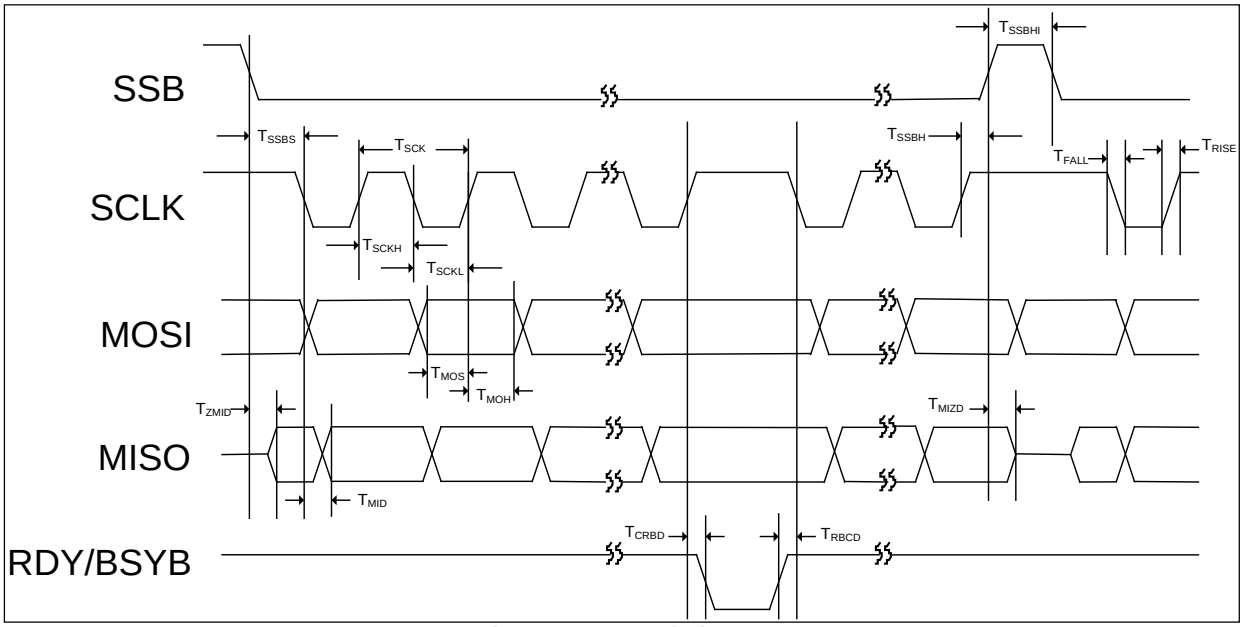


Figure 0-1 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

14.4.6 I²S Timing

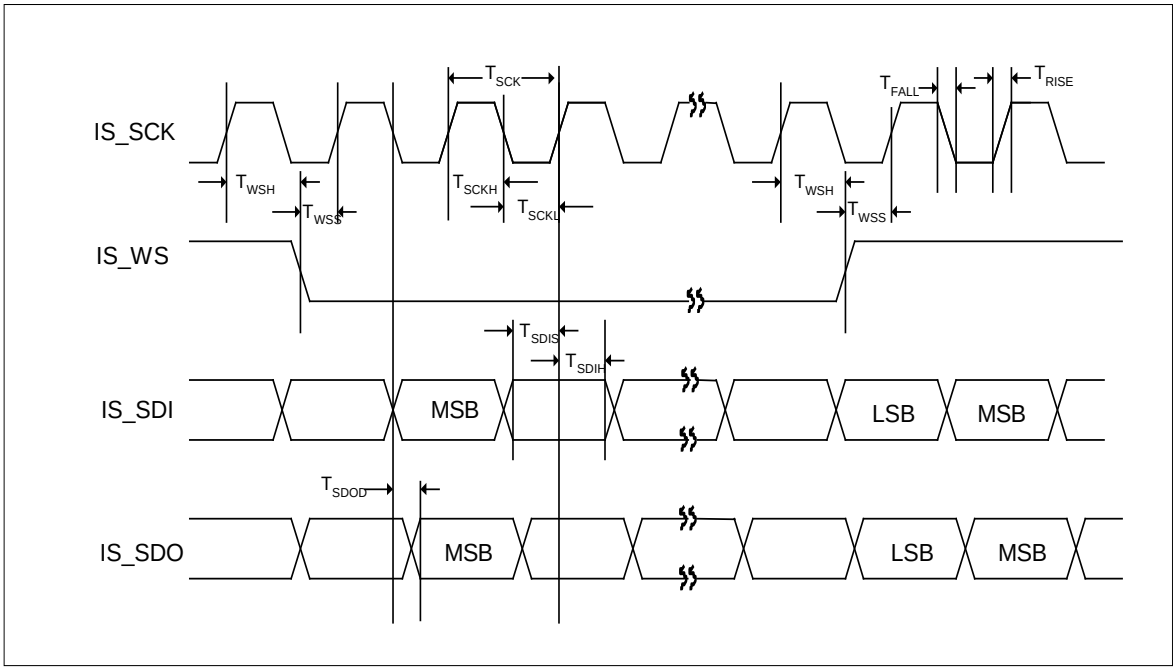


Figure 0-2 I²S Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	IS_SCK Cycle Time	60	---	---	ns
T_{SCKH}	IS_SCK High Pulse Width	25	---	---	ns
T_{SCKL}	IS_SCK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{WSS}	WS to IS_SCK Rising Edge Setup Time	20	---	---	ns
T_{WSH}	IS_SCK Rising Edge to IS_WS Hold Time	20	---	---	ns
T_{SDIS}	IS_SDI to IS_SCK Rising Edge Setup Time	15	---	---	ns
T_{SDIH}	IS_SCK Rising Edge to IS_SDI Hold Time	15	---	---	ns
T_{SDOD}	Delay Time from IS_SCLK Falling Edge to IS_SDO	---	---	12	ns

15 APPLICATION DIAGRAM

The following applications example is for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

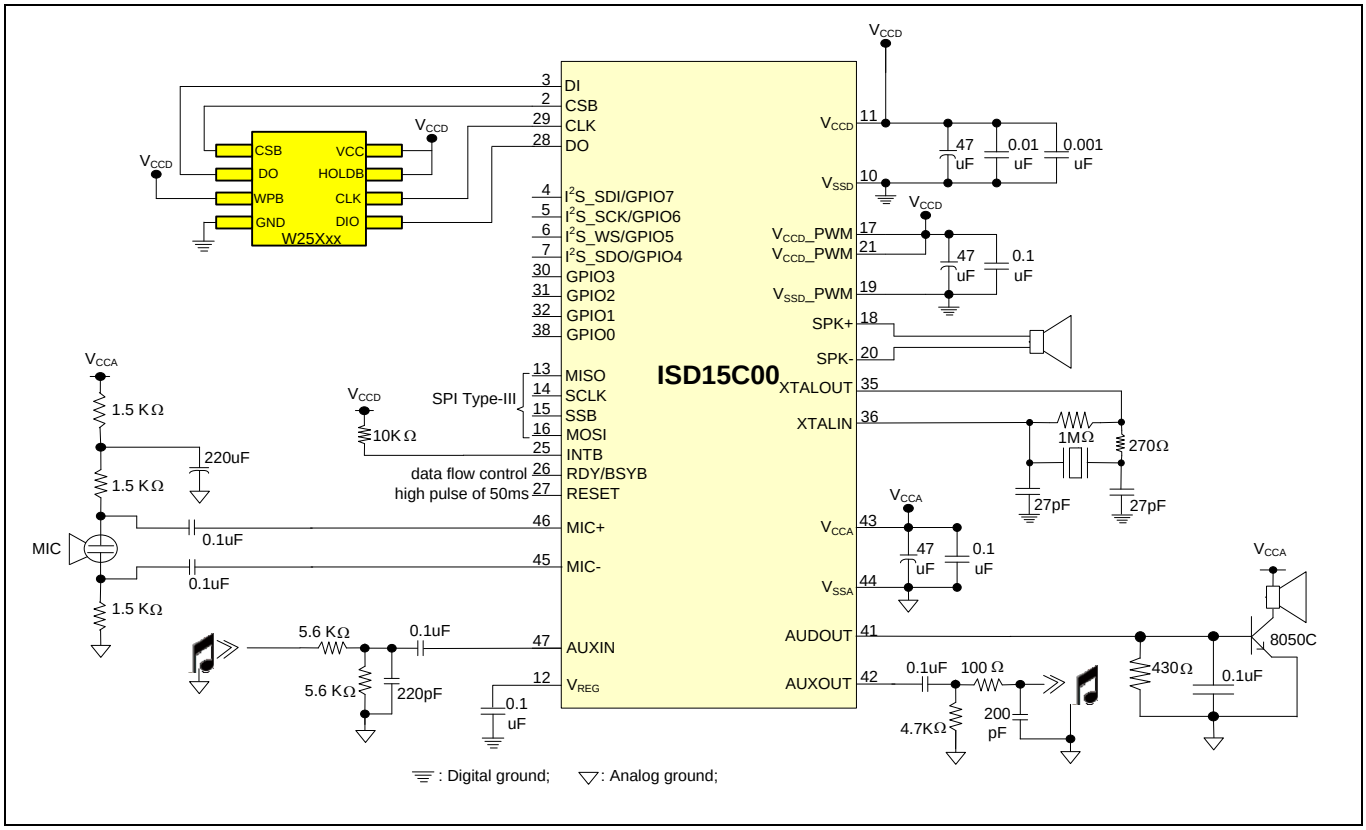
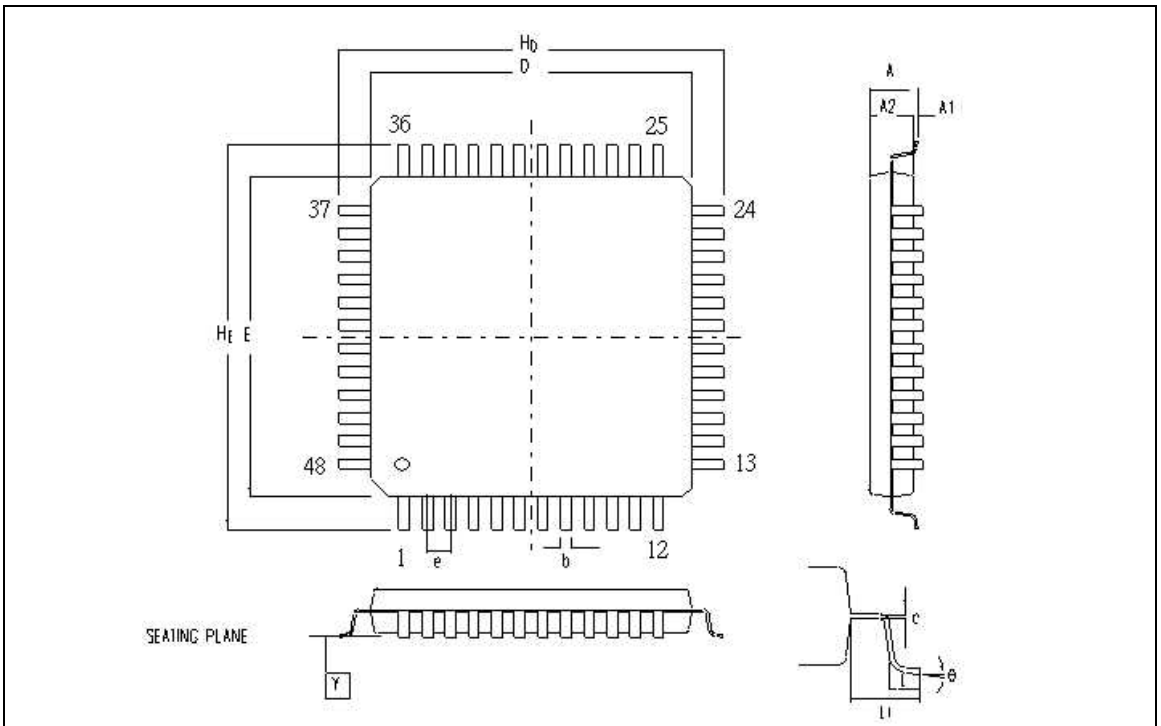


Figure 15-1 ISD15C00 Application Diagram

16 PACKAGE SPECIFICATION

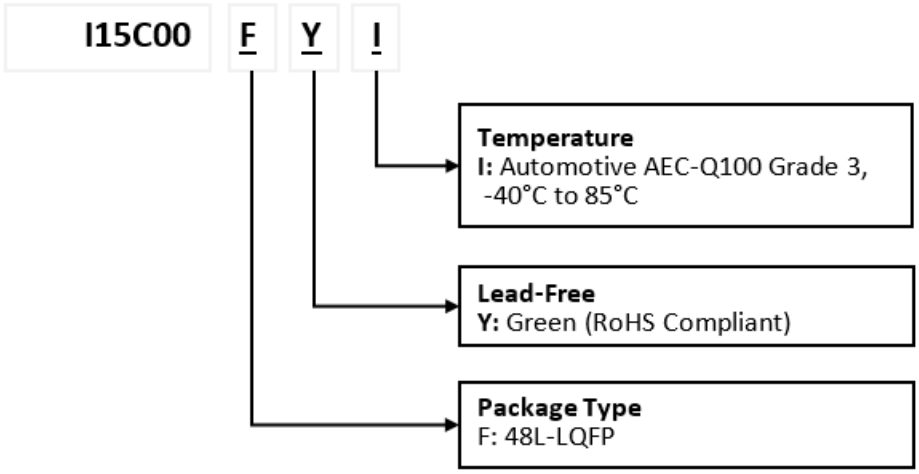
16.1 48 LEAD LQFP(7X7X1.4MM FOOTPRINT 2.0MM)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

17 ORDERING INFORMATION



Part Number	Duration	Package	Temperature	Notes
I15C00FYI	Ext. Flash 128Mbit / 64 Minutes	48L-LQFP	Automotive AEC-Q100 Grade 3 -40°C to 85°C	

18 REVISION HISTORY

Version	Date	Description
1.0	July 1, 2010	Update crystal configuration.
1.1	Dec 13, 2010	Fix the typo of internal memory to external memory.
1.3	May 6, 2011	Add Absolute Maximum Ratings.
1.4	Aug 30, 2011	Update register 0x19 ~ 0x1F description. Update output power description.
1.5	Mar 26, 2020	Update Document Format
1.6	Jun 15, 2021	Update Ordering Information Update output power Remove buzzer description

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