NAU88L25B
Ultra-Low Power Audio CODEC Ground-Referenced Headphone Amplifier with Headset Detection

GENERAL DESCRIPTION

The NAU88L25B is an ultra-low power high performance audio codec designed for smartphone, tablet PC, laptops, and other portable devices that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital mixer, two high quality DACs, one high quality ADC, one mono differential analog microphone input, two analog single-ended microphone inputs, and one stereo class G headphone amplifier with automatic headset detection. An integrated headset switch allows three different types of headsets to be configured, without changing hardware.

The advanced on-chip signal processing engine that includes dynamic range compressor (DRC) and programmable bi-quad filter, can maximize audio quality and eliminate any undesirable frequency components.

The NAU88L25B also has powerful headset detection that supports jack insertion / ejection, microphone detection, distinct key / short key / long key / key release detection features as well as an integrated frequency locked loop (FLL) to support various clocks.

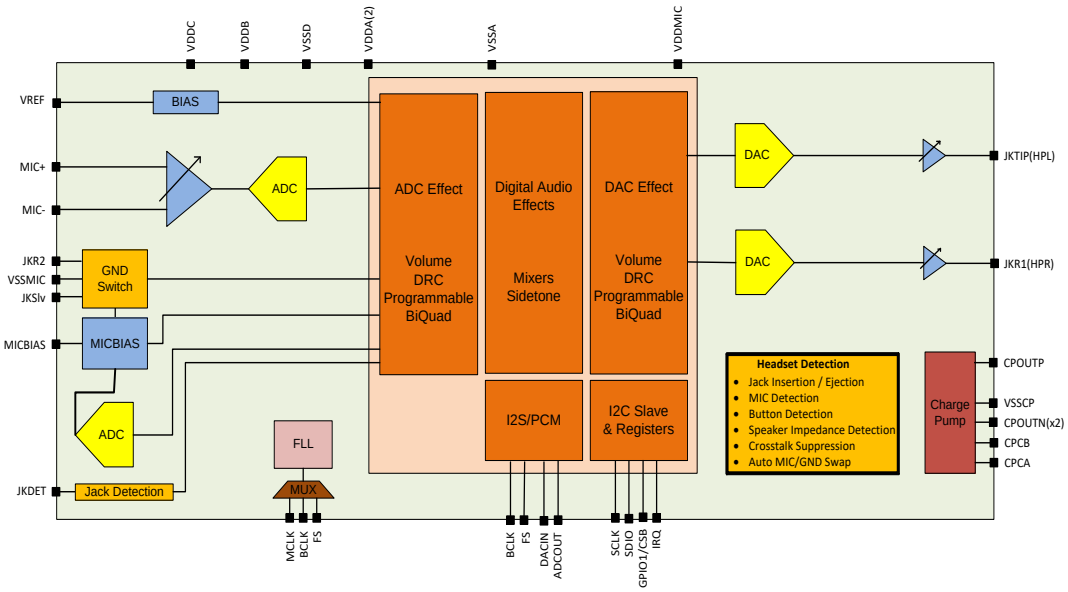
FEATURES

- DAC with auto attenuate: 124dB SNR; without auto mute: 113dB SNR, (A-weighted) @ 0dB gain, 1.8V and -89dB THD @ 20mW and RL= 32Ω, DAC playback to headphone output mode
- ADC: 101dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -91dB THD, 1.8V, MIC gain 0dB, OSR 128x
- 1 Digital I2S/PCM I/O port
- Dynamic Range Compressor (DRC)
- Programmable Biquad filter
- 1 Headset Mic, 1 Differential Analog Mic input, Line-input, or two single-ended Mic input
- Class G Headphone Amplifier (28mW @ 32Ω, 1% THD+N)
- Sampling rate from 8K to 192 KHz
- Headset Detection & Auto Headset switch for MIC and Ground
- Jack Insertion and Ejection Detection
- Distinct Keys Detection
- Package: 32 Pin QFN package, and Optional 42 Balls WLCSP with 0.4mm Pitch

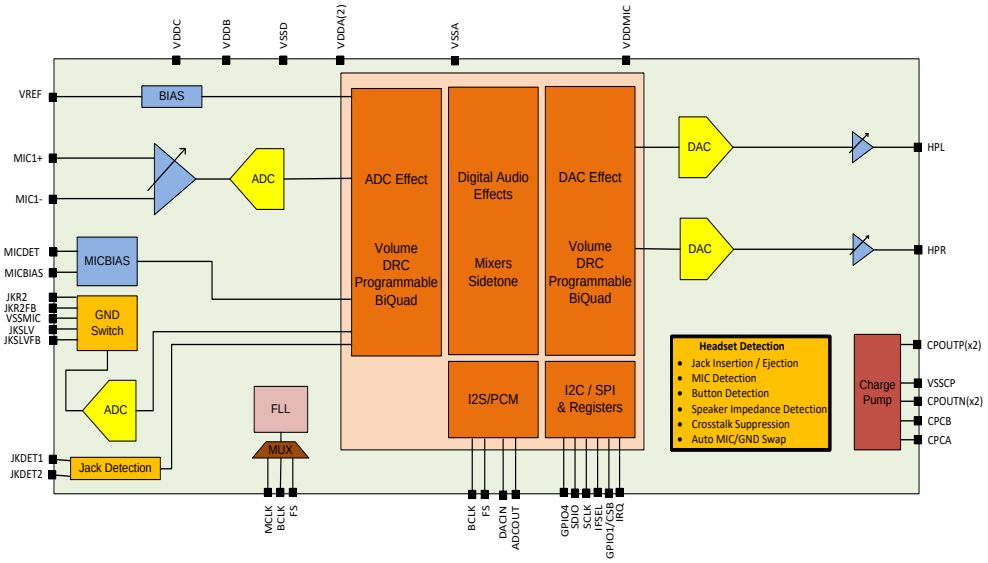
Applications

- Gaming Controller
- Ultra-Portable Laptop
- Mobile Device
- Wireless Headset
- Smart Remote Controller

Block Diagram: QFN32



Block Diagram: WLCSP42 Balls



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1 General Description

1.1 Overview

The NAU88L25B is an Ultra-Low-Power High-Performance Audio CODEC Ground-Referenced Headphone Amplifier with Advanced Headset Detection. The single-chip solution with microphone and ground detection and switching capabilities is designed for smartphones, tablets, Personal Computers (PCs), and other portable devices that support both analog and digital audio functions. The NAU88L25B is a cost-optimized solution for audio jack applications that benefit from enhanced audio quality and more integrated detection and suppression functions. Additionally, when used in combination with the Nuvoton NuMicro® NUC123, an ARM® Cortex MO-based microprocessor, the NAU88L25B Audio CODEC provides an easy-to-implement design solution for USB headphones.

The differential input architecture offers an improved Power-Supply Rejection Ratio (PSRR) and higher ground noise immunity. The highly-integrated NAU88L25B features one I2S/PCM Interface, one digital mixer, two high-quality audio Digital-to-Analog Converters (DACs), one high-quality audio Analog-to-Digital Converter (ADC), one monophonic differential analog microphone input, two analog single-ended microphone inputs, and one stereophonic Class G headphone amplifier with automatic headset detection. After automatically detecting which type of headset is in use—Stereo headphone, Nokia-type headsets, or Apple-type headsets—the NAU88L25B switches internal connections to support the appropriate format.

The advanced on-chip Digital Signal Processing (DSP) engine includes a Dynamic Range Compressor (DRC), and Programmable Bi-Quad Filters for various types of filters to optimize audio quality and eliminate undesirable frequency components.The NAU88L25B Audio CODEC provides comprehensive headset detection features that support jack insertion/ejection, microphone detection, distinct key / short key / long key / key release detection and Crosstalk detection/suppression. The chip also provides an integrated Frequency Locked Loop (FLL) to support various clocks.

1.2 Features

- Two Digital-to-Analog-Converters (DACs) with auto-attenuate:
  - 124 dB Signal-to-Noise Ratio (SNR) with auto mute;
  - 113 dB SNR, (A-weighted) @ 0 dB gain;
  - 1.8 V and -89 dB Total Harmonic Distortion (THD) @ 20 mW and R_L= 32 Ω,
  - DAC playback to Headphone Output Mode
- One Analog-to-Digital Converter (ADC):
  - 101 dB SNR (A-weighted) @ 0 dB Mircophone gain;
  - 1.8 V, Fs = 48 kHz and -91 dB THD, 1.8 V, MIC gain 0 dB,
  - Over Sampling Rate (OSR) 128x
- One Digital Integrated Interchip Serial Interface/Pulse Code Modulation Interface (I2S/PCM) Input/Output (I/O) port
- Dynamic Range Compressor (DRC)
- Three Programmable Bi-Quad Filters (1-ADC. 2-DAC)
- One Headset Microphone Input:
  - One Differential Analog Microphone input, Line-input, or
  - Two single-ended Microphone inputs
- One Class G Headphone Amplifier (28 mW @ 32 Ω, 1% THD+N)
- Sampling Rate selectable from 8 K to 192 KHz

- Headset Microphone and Ground Detection and Switching
- Jack Insertion and Ejection Detection
- Automatic headset format detection for three types of headsets:
  - Stereo headphone
  - Nokia-type headset
  - Apple-type headset
- Distinct Keys Detection
- Operating Conditions:
  - Voltage:
    - Digital Core 1.2 V
    - Analog Supply and Digital I/O Supply and FLL operation
    - Microphone Bias Supply 3 V
  - Temperature Range: Industrial: -40° C to 85° C
- Packages, Green:
  - Quad Flat No-Lead Package: QFN 32-Lead with 0.5 mm Pitch
  - Wafer Level Chip Scale Package: WLCSP 42 Balls with 0.4 mm Pitch

1.3 Applications

The Nuvoton NAU88L25B Audio CODEC is designed for smartphones, tablets, PCs, and other portable devices that support both analog and digital audio functions. After automatically detecting which type of headset is in use—Stereo headphone, Nokia-type headsets, or Apple-type headsets—the NAU88L25B switches internal connections to support the appropriate format. When used in combination with the NUC123 microprocessor, the NAU88L25B Audio CODEC provides an easy-to-implement design solution for USB headphones.

The NAU88L25B is cost-optimized for a wide variey of audio jack applications that benefit from enhanced audio quality and more integrated detection and suppression functions. To facilitate easy application and product development, Nuvoton provides reference Audio CODEC drivers for use with Windows® and Android® operating systems.

Typical applications include:

- Gaming Controllers
- Ultra-Portable Laptops
- Mobile Devices
- Wireless Headsets
- Smart Remote Controllers
- USB Headphones (in combination with the NUC123 microprocessor)

1.3.1 USB Headphones

Nuvoton provides a reference applicaton schematic in **Figure 1** to assist in the quick and cost-effective development of a USB Type C Headphone when the NAU88L25B Audio CODEC is used in combination with the NUC123 microprocessor. Appropriate firmware is also available to reduce product development effort and time-to-market.

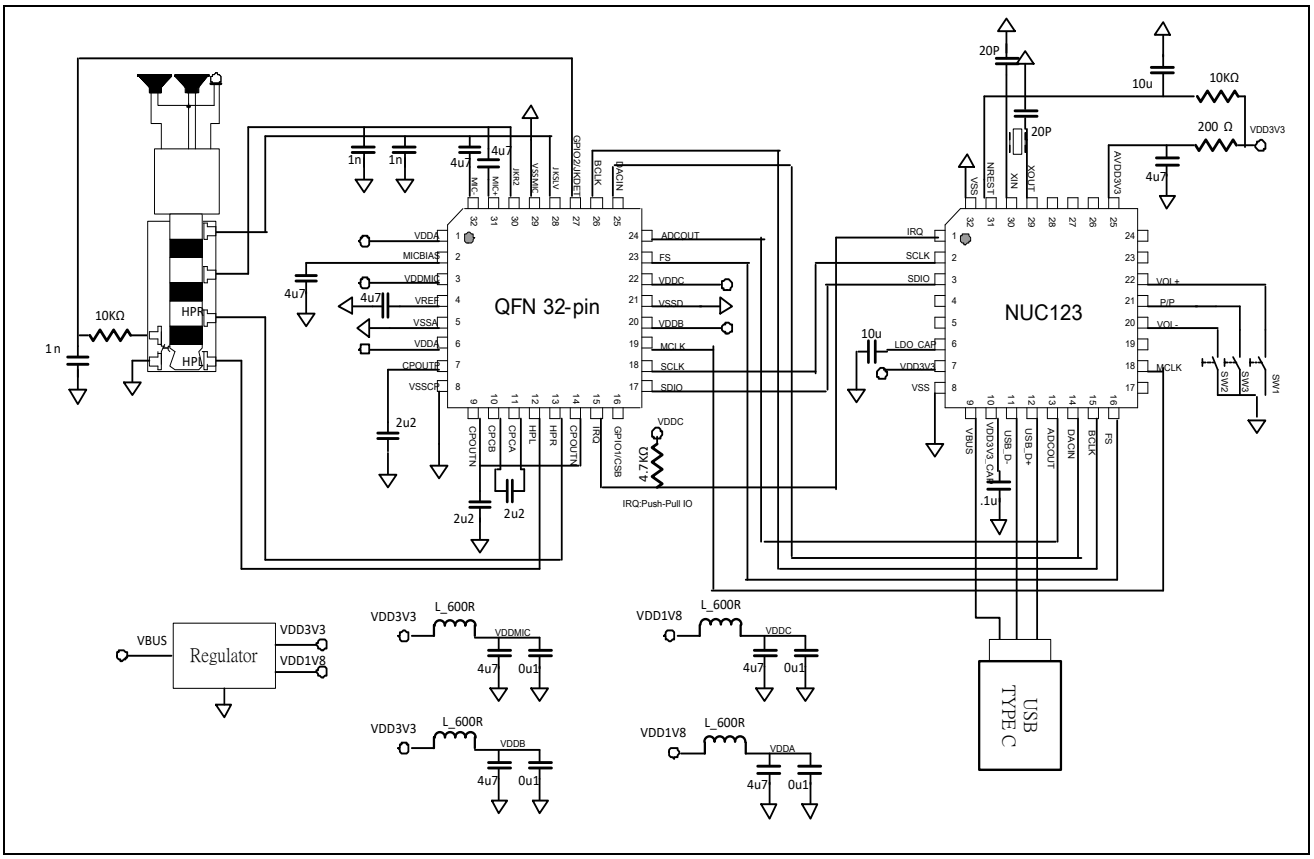


Figure 1 USB Headphone Reference Application Schematic

Note: This reference application schematic illustrates design implementation with the 32-Lead QFN package but the design also supports use of the 42-Ball WLCSP package of the NAU88L25B Audio CODEC.

1.3.2 Audio Jack Applications

The NAU88L25B CODEC is ideally suited to a variety of 3.5 mm Audio Jack applications, using either the **32-Lead QFN package** or the **42-Ball WLCSP** package, as shown in the two reference schematics in **Figure 2** and **Figure 3.**

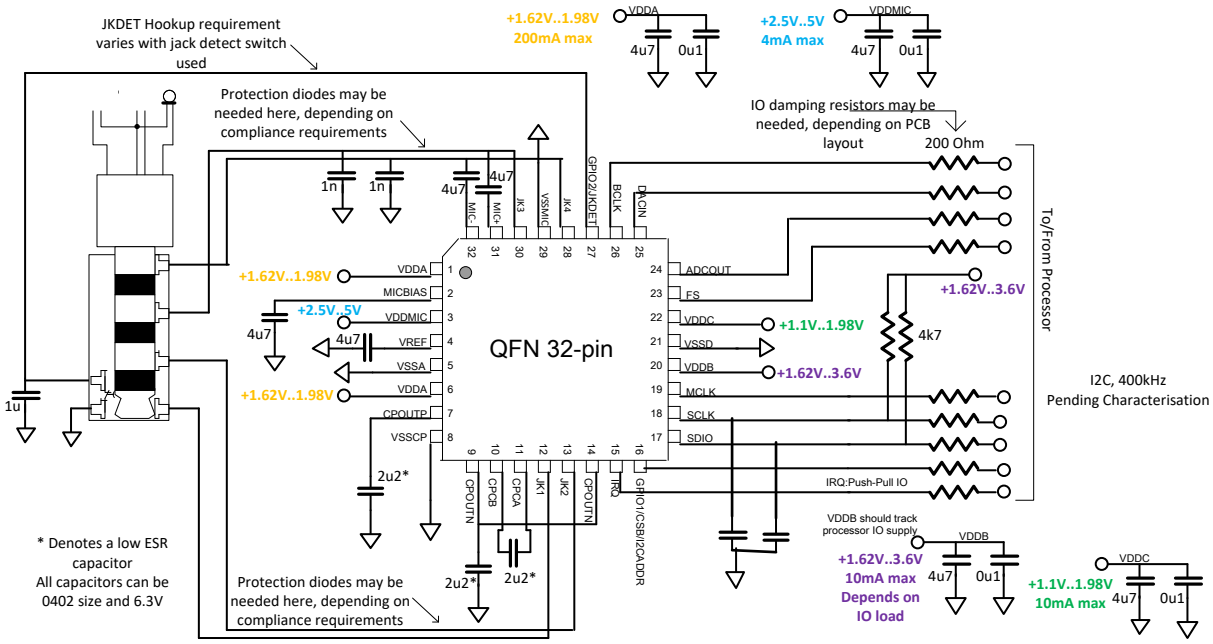


Figure 2 Audio Jack Reference Schematic 32-Lead QFN

Note: MIC+ with JKSLV, and MIC- with JKR2 constitute an alternative connection.

SCLK and SDIO can add a low pass filter to filter out glitch, the coner freuquency is about 8MHz to 33MHz

The **42-Ball WLCSP package** is shown in the sample reference schematic in **Figure 3.**

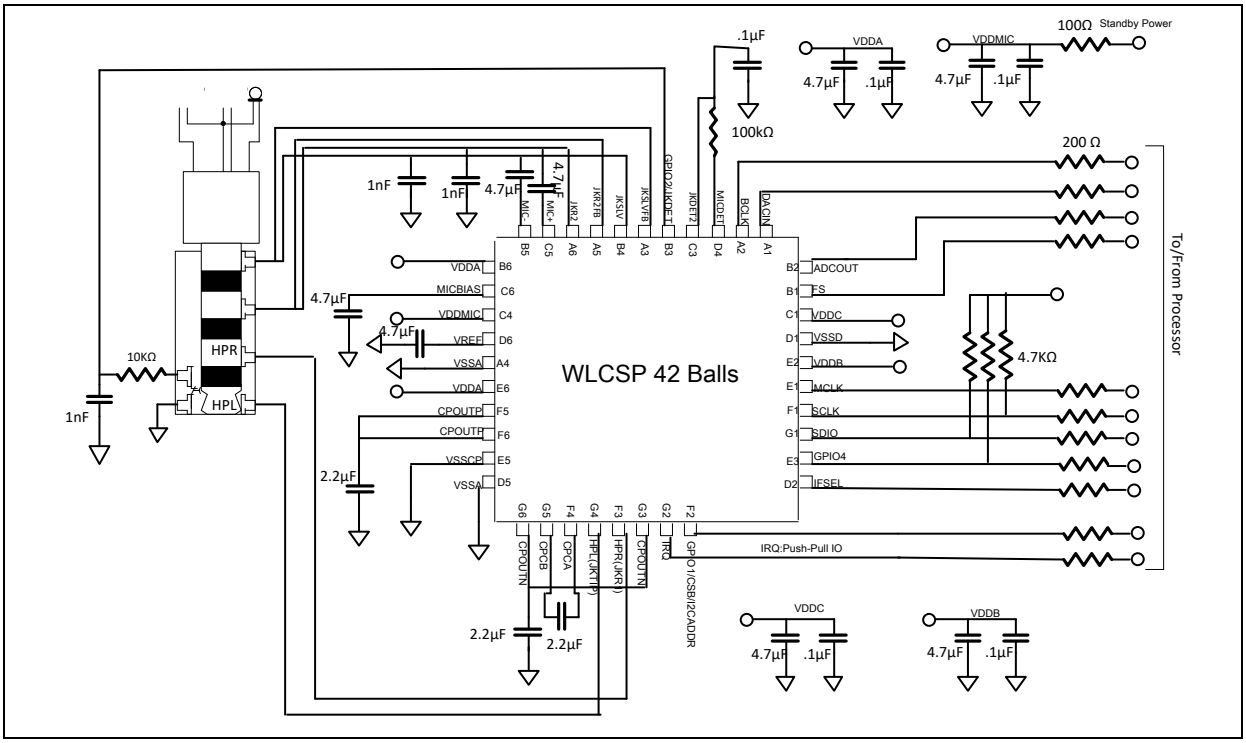


Figure 3 Audio Jack Reference Schematic 42-Ball WLCSP

Notes: Two pin combinations constitute altrnative connections: MIC+ with JKSLV, and MIC- with JKR2. JKR2 and JKR2FB are connected together on the jack connector side; the same applies to JKSLV and JKSLVFB. If microphone doesn't use, the JKSLVFB (A3) and JKR2FB (A5) connect to ground of jack connector, and JKSLV (B4) and JKR2 (A6) no connection.

A 100 KOhm resistor is recommended between MICDET and JKDET2 to reduce the current.

2 Pin Configurations

2.1 Pin Diagrams

The NAU88L25B Audio CODEC is available in a QFN 32-Lead package and in a WLCSP 42-Ball package, as shown in **Figure 4** and **Figure 5**, respectively.

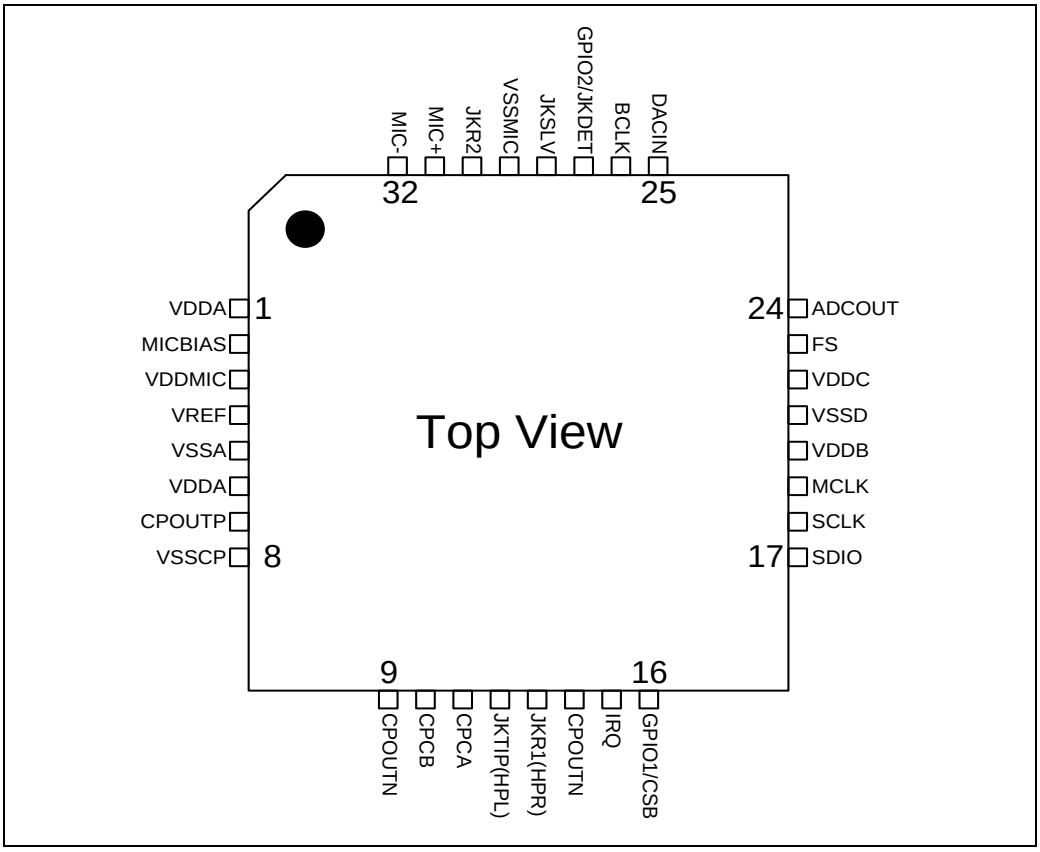


Figure 4 Pin Diagram 32-Lead QFN

Note: The large center pad under the 32-Lead QFN package should be connected to ground on the board to ensure good heat dissipation and mechanical stability.

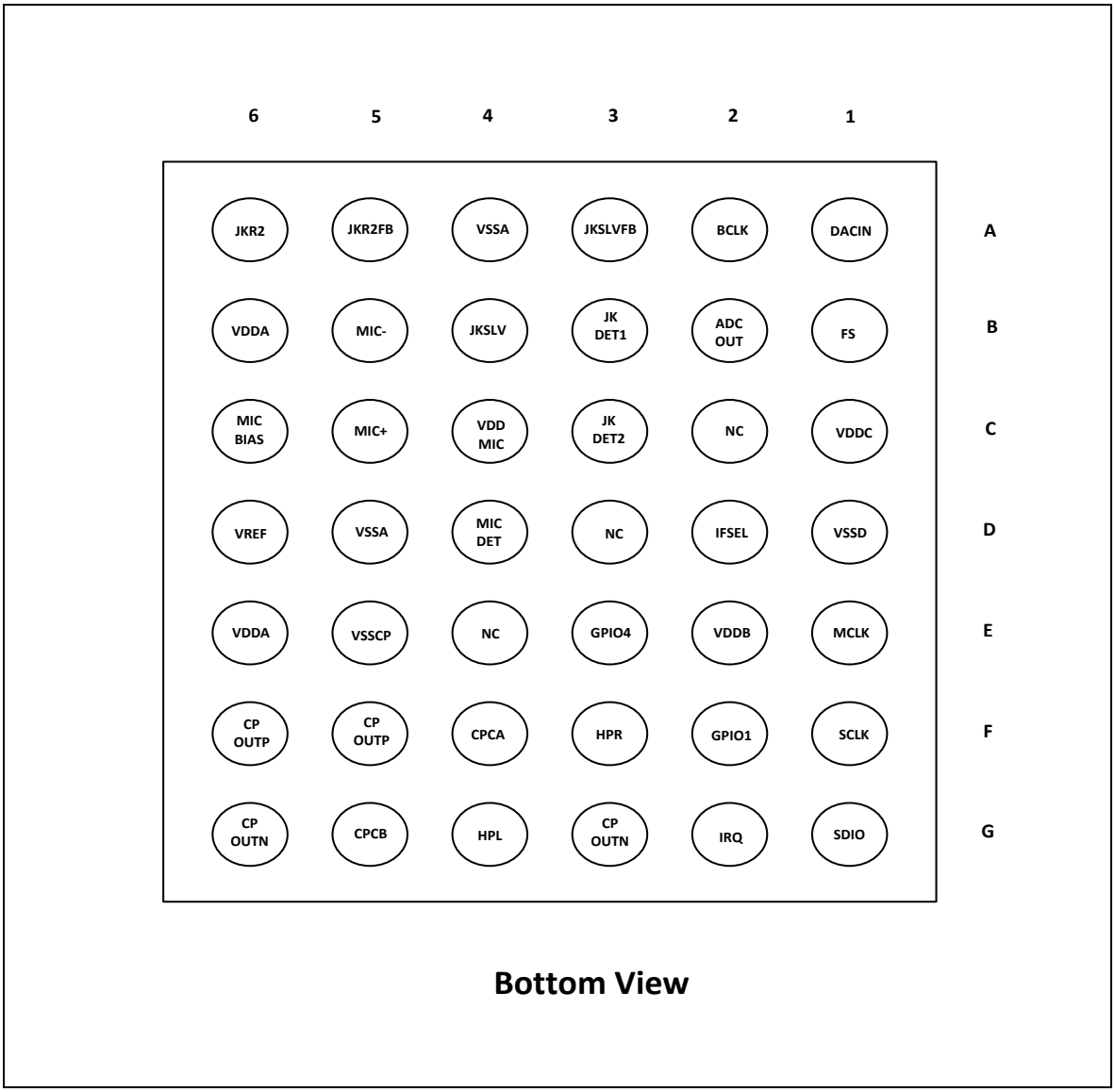


Figure 5 Pin Diagram 42-Ball WLCSP

2.2 Pin Descriptions

Pin Descriptions for the NAU88L25B are shown in **Table 1 and Table 2** by package type.
Note: Analog I/O supply is VDDA*;* Digital I/O supply is VDDB*.*

Table 1 Pin Descriptions for 32-Lead QFN

Pin #	Name	Type	Functionality
1	VDDA	Supply	Analog Supply
2	MICBIAS	Analog Output	Microphone Bias Output
3	VDDMIC	Supply	Microphone Supply
4	VREF	Analog I/O	Internal DAC & ADC Voltage Reference Decoupling I/O
5	VSSA	Ground	Analog Supply Ground
6	VDDA	Supply	Analog Supply
7	CPOUTP	Analog I/O	Charge Pump Positive Voltage
8	VSSCP	Ground	Charge Pump Supply Ground
9	CPOUTN	Analog I/O	Charge Pump Negative Voltage
10	CPCB	Analog I/O	Charge Pump Switching Capacitor Node B
11	CPCA	Analog I/O	Charge Pump Switching Capacitor Node A
12	JKTIP(HPL)	Analog Output	Jack Tip; Headphone Left Channel Output
13	JKR1(HPR)	Analog Output	Jack Ring 1; Headphone Right Channel Output
14	CPOUTN	Analog I/O	Charge Pump Negative Voltage
15	IRQ	Digital Output	Programmable Interrupt Output
16	GPIO1	Digital I/O	General Purpose I/O/I2C Address
17	SDIO	Digital I/O	Serial Data for I2C
18	SCLK	Digital Input	Serial Data Clock for I2C
19	MCLK	Digital Input	CODEC Master Clock Input
20	VDDB	Supply	Digital IO Supply
21	VSSD	Ground	Digital IO Ground
22	VDDC	Supply	Digital Core Supply
23	FS	Digital I/O	Frame Sync Input or Output for I2S or PCM Data
24	ADCOUT	Digital Output	Serial Audio Data Output for I2S or PCM Data
25	DACIN	Digital Input	Serial Audio Data Input for I2S or PCM Data
26	BCLK	Digital I/O	Serial Data Bit Clock Input or Output for I2S or PCM Data
27	JKDET	Analog Input	Jack Detect Input
28	JKSLV	Analog I/O	Jack Sleeve; Headset Jack Pin 4
29	VSSMIC	Ground	Analog Supply Ground
30	JKR2	Analog I/O	Jack Ring 2; Headset Jack Pin 3
31	MIC+	Analog Input	PGA MIC+ Analog Input
32	MIC-	Analog Input	PGA MIC- Analog Input

Table 2 Pin Descriptions 42-Ball WLCSP

Pin #	Name	Type	Functionality
A1	DACIN	Digital Input	Serial Audio Data Input for I2S or PCM Data
A2	BCLK	Digital I/O	Serial Data Bit Clock Input or Output for I2S or PCM Data
A3	JKSLVFB	Analog I	Jack Sleeve Feedback Sense Input
A4	VSSA	Ground	Analog Supply Ground
A5	JKR2FB	Analog I	JackRing 2 Feedback Sense Input
A6	JKR2	Analog I/O	JackRing 2 Jack Terminal
B1	FS	Digital I/O	Frame Sync Input or Output for I2S or PCM Data
B2	ADCOUT	Digital Output	Serial Audio Data Output for I2S or PCM Data
B3	JKDET1	Analog Input	Jack Detect Input
B4	JKSLV	Analog I/O	Jack Sleeve Jack Terminal
B5	MIC-	Analog Input	PGA MIC- Analog Input
B6	VDDA	Supply	Analog Supply
C1	VDDC	Supply	Digital Core Supply
C2	NC	No Connect	This pin should remain not connected
C3	JKDET2	Analog Input	Jack Detect Input
C4	VDDMIC	Supply	Microphone Supply
C5	MIC+	Analog Input	PGA MIC+ Analog Input
C6	MICBIAS	Analog Output	Microphone Bias Output
D1	VSSD	Ground	Analog Supply Ground
D2	IFSEL	Digital Input	I2C/SPI Interface selection
D3	NC	No Connect	This pin should remain not connected
D4	MICDET	Analog I/O	Microphone Signal and SAR ADC Input
D5	VSSA	Ground	Analog Supply Ground
D6	VREF	Analog I/O	Internal DAC & ADC Voltage Reference Decoupling I/O
E1	MCLK	Digital Input	CODEC Master Clock Input
E2	VDDB	Supply	Digital IO Supply
E3	GPIO4	Digital Output	Serial Data Output for SPI Data
E4	NC	No Connect	This pin should remain NOT CONNECTED
E5	VSSCP	Ground	Charge Pump Supply Ground
E6	VDDA	Supply	Analog Supply
F1	SCLK	Digital Input	Serial Data Clock for I2C
F2	GPIO1	Digital I/O	General Purpose Input Output/I2C Address
F3	JKR1(HPR)	Analog Output	Jack Ring 1; Headphone Right Channel Output
F4	CPCA	Analog I/O	Charge Pump Switching Capacitor Node A

Pin #	Name	Type	Functionality
F5	CPOUTP	Analog I/O	Charge Pump Positive Voltage
F6	CPOUTP	Analog I/O	Charge Pump Positive Voltage
G1	SDIO	Digital I/O	Serial Data for I2C
G2	IRQ	Digital Output	Programmable Interrupt Output
G3	CPOUTN	Analog I/O	Charge Pump Negative Voltage
G4	JKTIP(HPL)	Analog Output	Jack Tip; Headphone left channel output
G5	CPCB	Analog I/O	Charge Pump Switching Capacitor Node B
G6	CPOUTN	Analog I/O	Charge Pump Negative Voltage

Note: Analog I/O supply is VDDA; Digital I/O supply is VDDB.

3 Block Diagrams

The major functional blocks of the NAU88L25B Audio CODEC include:

- Two Digital-to-Analog-Converters (DACs)
- One Analog-to-Digital Converter (ADC)
- Dynamic Range Compressor (DRC)
- Programmable Bi-Quad Filters
- One Digital I2S/PCM I/O Interface
- One I2C Slave Interface
- Frequency-Locked Loop (FLL)
- Charge Pump
- Headset Microphone Input and Ground Detection
- Jack Insertion and Ejection Detection

Figure 6 and **Figure 7** provide the block diagrams for the 32-Lead QFN package and the 42-Ball WLCSP packages, respectively.

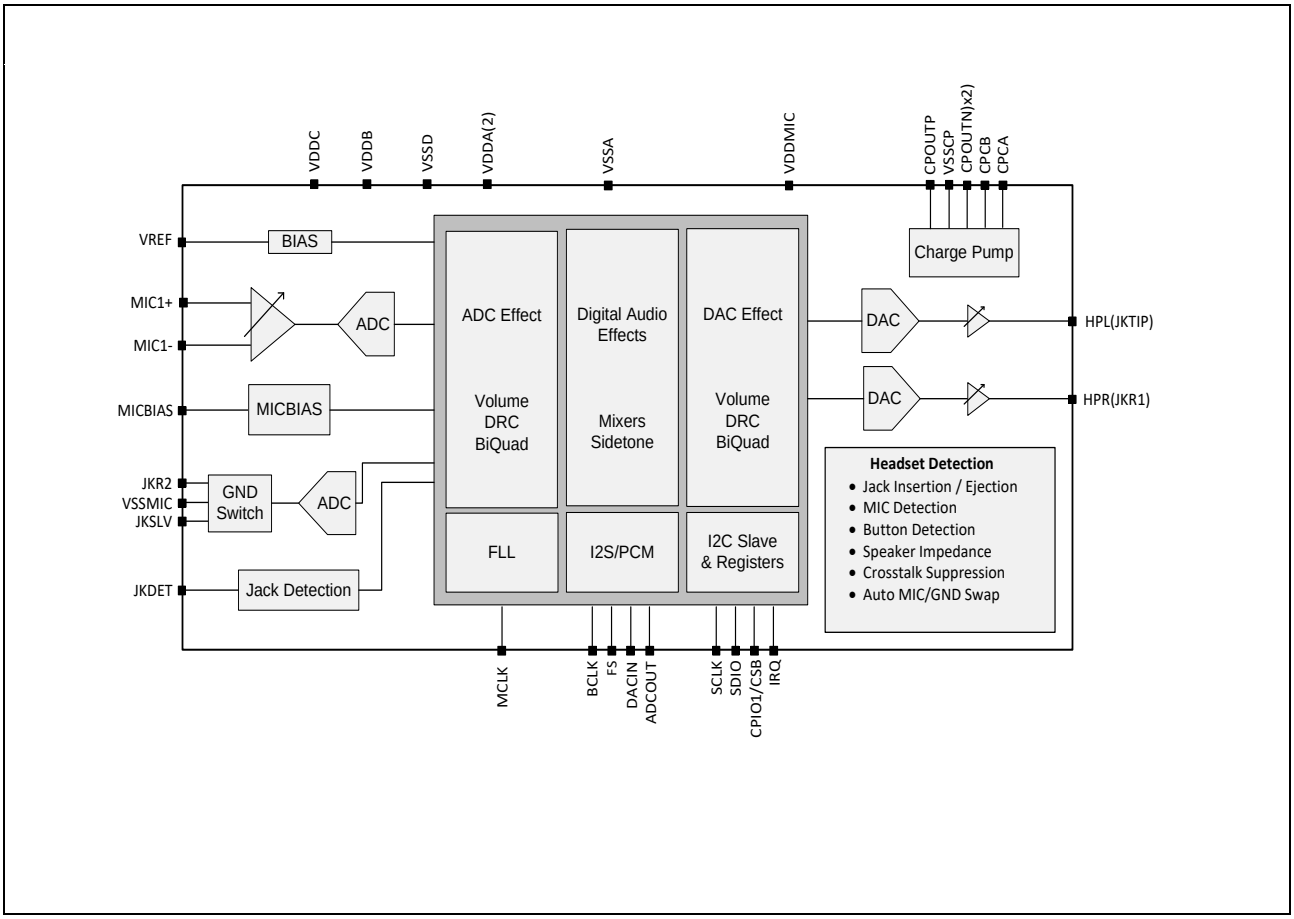


Figure 6 Block Diagram 32-Lead QFN

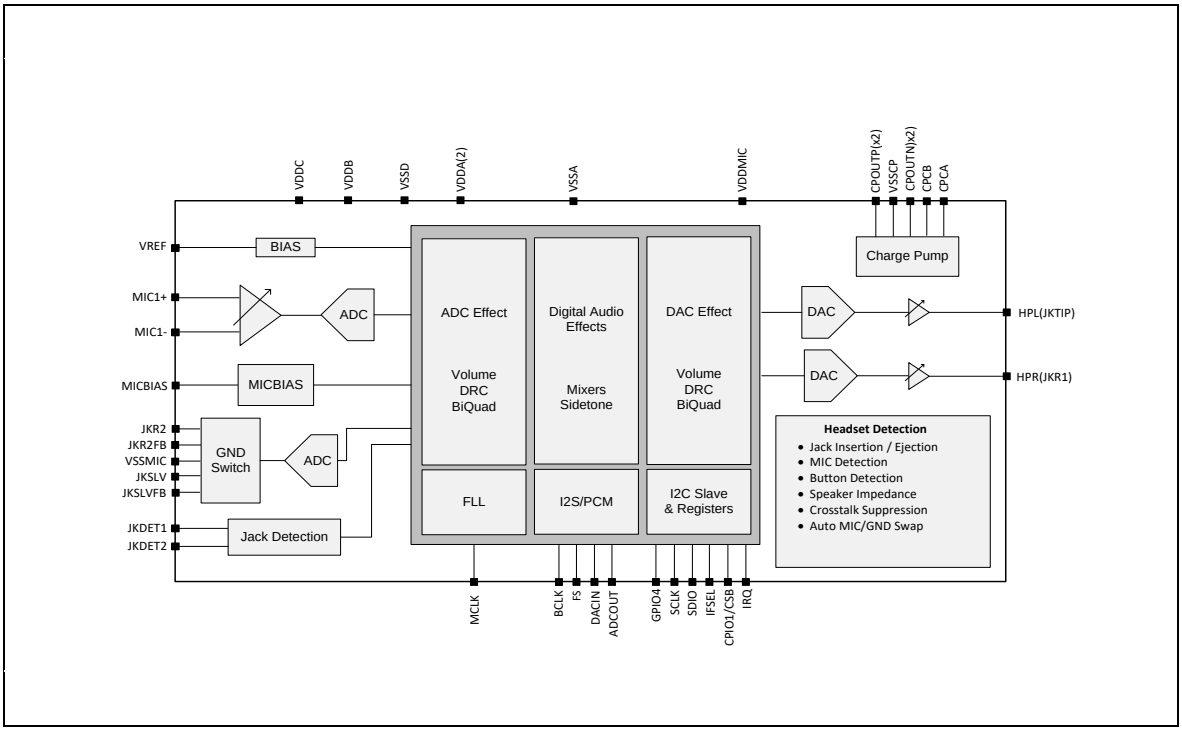


Figure 7 Block Diagram 42-Ball WLCSP

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 3 provides the absolute maximum ratings for the NAU88L25B Audio CODEC.

CAUTION: Do not operate at or near maximum ratings extended periods. Stresses above those listed in **Table 3** may cause permanent damage to the device. Exposure to conditions beyond these ratings may adversely affect the life and reliability of the device and result in failures not covered by warranty.

Table 3 Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C
Analog Supply Range	-0.3	2.2	V
Digital I/O Supply Range	-0.3	6.0	V
Digital Supply Range	-0.3	2.2	V
Input Voltage Digital Range	DGND - 0.3	VDD + 0.3	V
Input Voltage Analog Range	AGND - 0.3	VDD + 0.3	V
Headphone Supply Range	-0.3	2.2	V
Microphone Bias Supply Voltage	-0.3	6.0	V

CAUTION: The following conditions must be met for absolute maximum ratings:
VDDMIC > VDDA -1.2 V; VDDB > VDDC – 0.6 V.

4.2 Operating Conditions

Table 4 provides the recommended operating conditiions for the NAU88L25B.

Table 4 Operating Conditions

Condition		Symbol	Min	Typical	Max	Units
Analog Supply Range		VDDA	1.6	1.8	2.0	V
Digital Supply Range		VDDC	1.1	1.2	1.98	V
Digital Supply Range for FLL Operation and for Fs> 48 KHz		VDDC	1.61	1.8	1.98	V
Digital I/O Supply Range		VDDB	1.6	1.8	3.6	V
Headphone Supply Range		VDDA	1.6	1.8	2.0	V
Microphone Bias Supply Voltage		VDDMIC	2.5	4.2	5.0	V
Temperature Range		TA	-40		+85	°C
QFN Package	Junction to Ambient	η°_{ja}		33.1		°C/W
	Junction to Case	η°_{jc}		3.1		°C/W

CAUTION: The following conditions must be met for absolute maximum ratings:
VDDMIC > VDDA -1.2 V; VDDB > VDDC – 0.6 V.

4.3 Shutdown and Standby Current

Table 5 provides Shutdown and Standby currents.

Conditions: VDDA = VDDB = VDDC = 1.8 V; VDDMIC= 4.2 V. RL(Headphone) = 32 Ω, f = 1 kHz, MCLK=12.88 MHz, unless otherwise specified. Limits apply for TA = 25° C.

Table 5 Shutdown and Standby Current

Parameter	Symbol	Conditions	Typical	Limit	Units
Shutdown Current	ISD	VDDA in Shutdown Mode	0.2	1	µA
		VDDA When VDDC=1.2 V	17.2		
		VDDB	0.2	1	
		VDDC	2	10	
		VDDMIC	0.2	1	
Standby Current	IDD	MCLK off, Jack Insertion, IRQ enabled	5		µA

4.4 ADC Characteristics

Table 6 provides the ADC electrical characteristics for the NAU88L25B Audio CODEC.

Conditions: VDDA = VDDB = VDDC = 1.8 V; VDDMIC= 4.2 V. RL(Headphone) = 32 Ω, f = 1 kHz, MCLK=12.88 MHz, unless otherwise specified. Limits apply for TA = 25° C.

Table 6 ADC Electrical Characteristics

Parameter	Symbol	Conditions	Typical	Limit	Units
ADC Total Harmonic Distortion + Noise	THD+N	MIC Input, MIC_GAIN = 0 dB, VIN = 0.8 Vrms, f = 1 KHz, fs = 48 KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30 dB, Volume = 0 dB, VIN = 28.5 Vrms, fs = 1 k, Digital Gain = 0 dB, Mono Differential Input	-80		dB
Signal-to-Noise Ratio	SNR	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0 dB,fs = 8 KHz, Mono Differential Input	101		dB
		Reference = VOUT(0 dB FS), A-Weighted, MIC Input, MIC Gain = 6 dB,fs = 8 KHz, Mono Differential Input	98		dB
Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 200 mV_{PP} applied to VDDA, f_{RIPPLE} = 217 Hz, Input Referred, MIC_GAIN = 0 dB Differential Input	78		dB

Parameter	Symbol	Conditions	Typical	Limit	Units
Common Mode Rejection Ratio	CMRR	Differential Input 100 Vrms, PGA Gain = 20 dB, frequency sweep from 20 Hz to 20 KHz	64		dB
ADC Full Scale Input Level	FSADC	VDDA= 1.8 V	1		V_{RMS}
Input Impedance			12		KOhm
Frequency Response		f = 20 Hz ~ 20 KHz	+/-0.02		dB
Power Consumption		No Load, No Signal, ADC on, PGA on; fs = 44.1 kHz	5.4		mW

4.5 Headphone Amplifier Characteristics

Table 7 provides the headphone amplifier electrical characteristics for the NAU88L25B.

Conditions: VDDA = VDDB = VDDC = 1.8 V; VDDMIC= 4.2 V. RL(Headphone) = 32 Ω, f = 1 kHz, MCLK=12.88 MHz, unless otherwise specified. Limits apply for TA = 25° C.

Table 7 Headphone Amplifier Electrical Characteristics

Parameter	Symbol	Conditions	Typical	Limit	Units
Output Power 32-Lead QFN Package	PO	Stereo R_L = 16 Ω, DAC Input, CPVDD = 1.8 V, f = 1 kHz, 22 kHz BW, THD+N = 1% w. Headset Switch	35		mW
		Stereo RL = 32 Ω, DAC Input, CPVDD = 1.8 V, f = 1 kHz, 22 kHz BW, THD+N = 1%, w. Headset Switch	28		mW
Output Power 42-Ball WLCSP Package		Stereo R_L = 16Ω, DAC Input, CPVDD = 1.8 V, f = 1 kHz, 22 kHz BW, THD+N = 1%, w. Headset Switch	39.5		mW
		Stereo RL = 32 Ω, DAC Input, CPVDD= 1.8 V, f = 1 kHz, 22 kHz BW, THD+N = 1%, w. Headset Switch	30.5		mW
Total Harmonic Distortion + Noise	THD+N	RL = 32 Ω, f=1 kHz, PO = 20 mW, w. Headset Switch	-89		dB
Signal to Noise Ratio	SNR	VOUT = 1 VRMS, DAC Input, DAC_Gain = 0 dB, HP_Gain = 0 dB, Digital Zero Input, f = 1 kHz, A-Weighted, w. Headset Switch	113		dB
		VOUT = 1 V_{RMS}, DAC Input, DAC_Gain = 0 dB, HP_Gain = 0 dB, Digital Zero Input, f = 1 kHz, A-Weighted, Auto Mute Enabled, w. Headset Switch	124		dB

Parameter	Symbol	Conditions	Typical	Limit	Units
Power Supply Rejection Ratio	PSRR	fRIPPLE = 217 Hz, VRIPPLE = 200 mV_{P_P} Input Referred, HP_GAIN = 0 dB DAC Input, DAC_Gain = 0 dB Ripple Applied to VDDA	81		dB
Channel Crosstalk	X_{TALK}	Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching Off without HCS	88		dB
		Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching On with HCS (**QFN**)	91		dB
		Left Channel to Right Channel, -1 dB FS, Gain = 0 dB, f = 1 kHz, MIC/GND Switching On with HCS (**WLCSP**)	98		dB
Interchannel Level Mismatch		Headphone Right and Left Channel Difference with 0 dB FS Input Sweep from 20 Hz to 20 KHz	+/- 0.1		dB
Frequency Response		F = 20 Hz ~ 20 KHz	+/-0.005		dB
Output Noise	$\mathbf{e}_{OS}$	DAC_Gain = 0 dB, HP_Gain = 0 dB, f_S=48 kHz, OSRDAC = 128, A-Weighted	2.2		μV_{RMS}
Out-of-Band Noise Level		BW= 400 Hz to 500 KHz	-86		dB
Output Offset Voltage	VOS	HP_Gain = 0 dB, DAC_Gain= 0 dB, DAC Input	0.1	±0.5	mV
Power Consunption		No Load, No Signal, Amp on f_S = 48 kHz, Stereo DAC On, Amp On, POUT = 0 mW. R_L = 32 Ω	5.7		mW
Pop-and-Click Noise		Into or out of DAC to Headphone Shutdown, Headphone Impedance & Crosstalk Detection Disabled	.1		mVrms
Ground Switch ON Resistance		ON Resistance between JKR2 and GND or JKSLV and GND (QFN)	.09		Ohm
		ON Resistance between JKR2 and GND or JKSLV and GND (WLCSP)	0.075		Ohm

4.6 Digital I/O Characteristics

Table 8 provides the headphone amplifier electrical characteristics for the NAU88L25B.

Conditions: VDDA = VDDB = VDDC = 1.8 V; VDDMIC= 4.2 V. RL(Headphone) = 32 Ω, f = 1 kHz, MCLK=12.88 MHz, unless otherwise specified. Limits apply for TA = 25° C.

Table 8 Digital I/O Characteristics

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW Level	VIL	VDDB = 1.8 V			0.33* VDDB	V
		VDDB = 3.3 V			0.37**VDDB	
Input HIGH Level	VIH	VDDB = 1.8 V		0.67* VDDB		V
		VDDB = 3.3 V		0.63* VDDB		
Output HIGH Level	VOH	I_{Load}= 1mA	VDDB = 1.8 V	0.9* VDDB		V
			VDDB = 3.3 V	0.95* VDDB		
Output LOW Level	VOL	I_{Load}= 1mA	VDDB = 1.8 V		0.1* VDDB	V
			VDDB =3.3 V		0.05* VDDB	

5 Functional Overview

The Nuvoton NAU88L25B is a new generation of ultra-low power Audio CODEC that has both analog and digital blocks operating at 1.8 V and a digital core that is able to operate at 1.2 V. This CODEC includes new Digital Signal Processing (DSP) functions including Dynamic Range Compression (DRC) and programmable Bi-Quad Filters.

5.1 Power Supply Functions

The NAU88L25B is designed to operate reliably under a wide range of power supply conditions and power-on/power-off sequences. However, ESD protection diodes between the supplies affect the application of the supplies. The ESD protection diodes require the following conditions must be met:

VDDMIC > VDDA-1.2 V and VDDB > VDDC – 0.6 V

The NAU88L25B includes a power on/off reset circuit on-chip. The circuit resets the internal logic control on VDDC and VDDA supply power up. This reset function is also automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55 Vdc for VDDC and 1.0 Vdc for VDDC and VDDA, respectively. Note that these values are much lower than the required voltage for normal operation.

The reset is held On when the power levels for both VDDC and VDDA are below their respective thresholds. When the power levels rise above their thresholds, the reset is released. When the reset is released, the registers are ready for Write operations.

An additional internal RC filter-based circuit helps the circuit respond for fast ramp rates (~10 µs) and generates the desired reset period width (~10 µs at typical corner). This filter is also used to eliminate supply glitches that can generate false reset conditions, typically 50 ns. For reliable operation, it is recommended to write to the register **SOFTWARE_RST REG0X00** at power-up. This will reset all registers to the known default state.

5.1.1 Power Supply Application Notes

Reset threshold values are much lower than the required voltage for normal operation.

All registers should remain in their reset state for at least 6 µs.

VDDA ramp-up time for a guaranteed power- on-reset needs to be less than 50 msec.

When VDDA and/or VDDC are below the power-on-reset threshold, the digital IO pins will go into a tri-state condition.

The VDDA ramp-down time for a guaranteed power-off reset must be less than 125 msec. If the ramp down rate is too slow (no pull down), it is possible to enable the minimum VREF impedance by **BIAS_ADJ.VMIDSEL REG0X66[5:4]** ='11' with **BIAS_ADJ.VMIDEN REG0X66[6]** ='1', before shutdown in order to discharge VDDA quickly.

5.2 Inputs and Outputs

The NAU88L25B provides analog inputs to acquire and process audio microphones signals with high fidelity and flexibility. The input path has two input pins that can be used to capture signals from either single-ended or differential sources. The channel has a fully differential Programmable Gain Amplifier (PGA). The outputs of the PGA connect to the Analog-to-Digital Converter (ADC).

5.2.1 Input/Output Appplication Notes

One stereophonic, ground-referenced Class G headphone output is fed by two Digital-to-Analog Converters (DACs). The headphone amplifier has a gain range of -54 dB to 0 dB. The Class G stereophonic headphone amplifier is powered by Charge Pump output voltages CPOUTP and CPOUTN. In a no-load condition, CPOUTP is equal to VDDA, and CPOUTN is equal to –VDDA.

5.3 Companding

Companding is used in digital communication systems to optimize the Signal-to-Noise Ratio (SNR) with reduced data bit rates using non-linear algorithms. Companding can be useful in both ADC and DAC operations of the NAU88L25B Audio CODEC.

The NAU88L25B supports the two main telecommunications companding standards on both the transmit and receive sides: A-Law and μ-Law. The A-Law algorithm is primarily used in European communication systems and the μ-Law algorithm is primarily used by North America, Japan, and Australia. **Chapter 5.3.1** and **5.3.2** provide the compression equations set by the ITU-T G.711 standard and implemented in the NAU88L25B

Companding converts 14 bits (μ-Law) or 13 bits (A-Law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits, and 4 mantissa bits. This option can be enabled for both of the DACs and the ADC using these registers: **I2S_PCM_CTRL1.DACCM0 REG0X1C[15:14]** and **I2S_PCM_CTRL1.ADCCM0_REG0X1C[13:12]**, respectively. When the Companding Mode is enabled, **I2S_PCM_CTRL1.CMB8_0 REG0X1C[10]** must be enabled for 8-bit operation. This will disable the word length selection in **I2S_PCM_CTRL1.WLEN REG0X1C[3:2]** for this port and allow the companding functions to use an 8-bit word length.

5.3.1 μ-Law Compression

$$F(x) = \frac{\ln(1+\mu\times|x|)}{\ln(1+\mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

5.3.2 A-Law Compression

$$F(x) = \frac{A\times|x|}{(1+\ln(A))}, \qquad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1+\ln(A\times|x|)}{(1+\ln(A))}, \qquad \frac{1}{A} \le x \le 1$$

$$A = 87.6$$

5.4 Signal Conversion and Processing

The NAU88L25B has three high-quality, independent signal converters: one ADC and two DACs. They are high-performance 24-bit sigma-delta converters, suitable for a very wide range of audio applications. The ADC and the DACs have functions that individually support analog mixing and routing. The ADC and DACs blocks also support advanced DSP subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize creation of processing artifacts and to maximize the audio dynamic range supported by the NAU88L25B.

The ADC and DACs digital signal processing can support a four-point Dynamic Range Compressor (DRC), Programmable Bi-Quad Filters configurable for low-pass filters, high-pass filters, Notch filters, Bell filters, low-shelf filters, and high-shelf filters with various gain (aka “Q”) and frequency controls. The two-point DRC can be programmed to limit the maximum output level and/or boost a low output level. The Bi-Quad Filters can configure high-pass filters intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or “wind noise” on a microphone input. Notch filters can also be configured to greatly reduce the noise at a specific frequency band or frequency, such as removing the power supply 60 Hz noise.

5.5 Digital Interfaces

Command and control of the NAU88L25B are accomplished using a 2-wire Serial Control Interface (I2C). This simple, but highly flexible interface is compatible with most commonly used command and control serial data protocols and host drivers. The digital audio I/O data streams transfer separately from the command and control instructions using either I2S or PCM audio data protocols. These interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I2S and PCM devices.

Detailed information for the Control Interfaces is provided in **Chapter 10**. Information about the Digital Audio Interfaces is provided in **Chapter 11**.

6 Input Operation

The NAU88L25B has one low-noise, high-common-mode-rejection-ratio analog microphone differential. The two microphone inputs, MIC+ and MIC-, are followed by a -1 dB to 36 dB Programmable Gain Amplifier (PGA) gain stage with a fixed 12 KOhm input impedance. Inputs are maintained at a DC-bias of approximately half (½) of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of external DC blocking capacitors suitable for the device application. The Audio Microphone Input Path is shown in the block diagram in **Figure 8**.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary, such as in portable digital media devices and cell phones. Differential inputs are also very useful for reducing ground noise in systems in which there are ground voltage differences between various chips and other components. When properly implemented, the differential input architecture offers an improved Power-Supply Rejection Ratio (PSRR) and higher ground noise immunity.

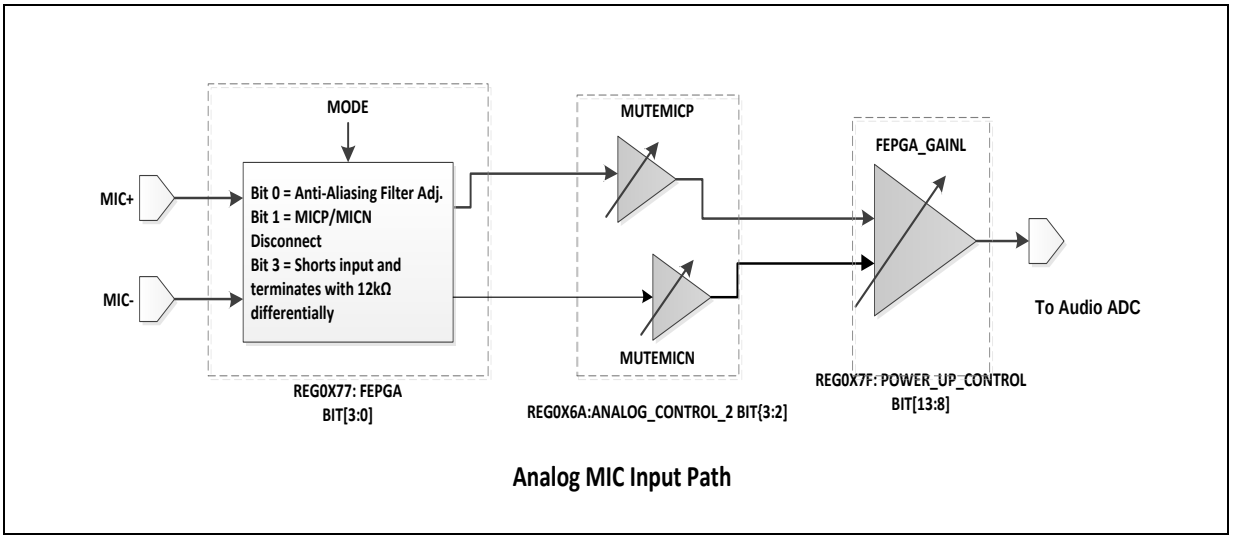


Figure 8 Microphone Input Block Diagram

6.1 Analog Microphone Inputs

The analog microphone inputs are followed by an input stage before being routed to the Front End Programmable Gain Amplifier (FEPGA) stage. The input stage can configure different mode stages by **FEPGA.FEPGA_ MODEL REG77[3:0]**. The microphone inputs are followed by a 1 dB step from -1 dB to 36 dB FEPGA gain stage with a fixed 12 KOhm input impedance. FEPGA can be individually enabled or disabled using **POWER_UP_ CONTROL.PUFEPGA REG0X7F[14].**

The FEPGA can be set for operation in Low-Power Mode or High-Power Mode using **BIAS_ADJ.BIASADJ REG0X66[1:0]** MIC+/- could be muted using either register by **ANALOG_ CONTROL_2.MUTEMICP** or **ANALOG_ CONTROL_2.MUTEMICN REG0X 6A[3:2].** The gain for FEPGA can be set using **POWER_UP_ CONTROL. FEPGA_GAIN REG0X7F[13:8];** set the gain from -1 dB to 36 dB with 1 dB per step.

The **ANALOG_ADC_2.VREFSEFL1** and **ANALOG_ADC_2.VREFSEFL0** registers can be optimized to improve ADC Total Harmonic Distortion. Each input has an input impedance of about 12-kΩ by setting **FEPGA.FEPGA_ MODEL REG77[3:0]** =0X8.

6.1.1 Microphone Input Application Notes

If the application uses single-ended MIC inputs, the input can be precharged to VREF as a single-ended input using **FEPGA.ACDC_CTRL REG0X77[15:14].**

When using a single-ended input, the unused input pin should be AC-coupled to Ground to improve common-mode noise rejection.

If the application has large decoupling capacitors on the inputs, it is possible to pre-charge the capacitors to minimize pops and clicks during startup. For more detail, please refer to register **FEPGA.ACDC_CTRL REG0X77[15:14]**.

6.2 Reference Voltage

The NAU88L25B includes a mid-supply Reference Circuit that produces voltage close to VDDA/2 that is decoupled to VSS through the VREF pin by means of an external bypass capacitor. VREF is used as a reference voltage for the much of the NAU88L25B,so a large capacitance is required to achieve good power supply rejection at low frequency. Typically 4.7 µF is used. The VREF voltage can be enabled by setting **BIAS_ADJ.VMIDEN REG0X66[6]** and the output impedance can be set using **BIAS_ADJ.VMIDSEL_REG0X66[5:4]**. **Figure 9** illustrates the VREF circuitry. **Table 9** identifies the appropriate values for VMIDSEL, based on resisor and impedance choices.

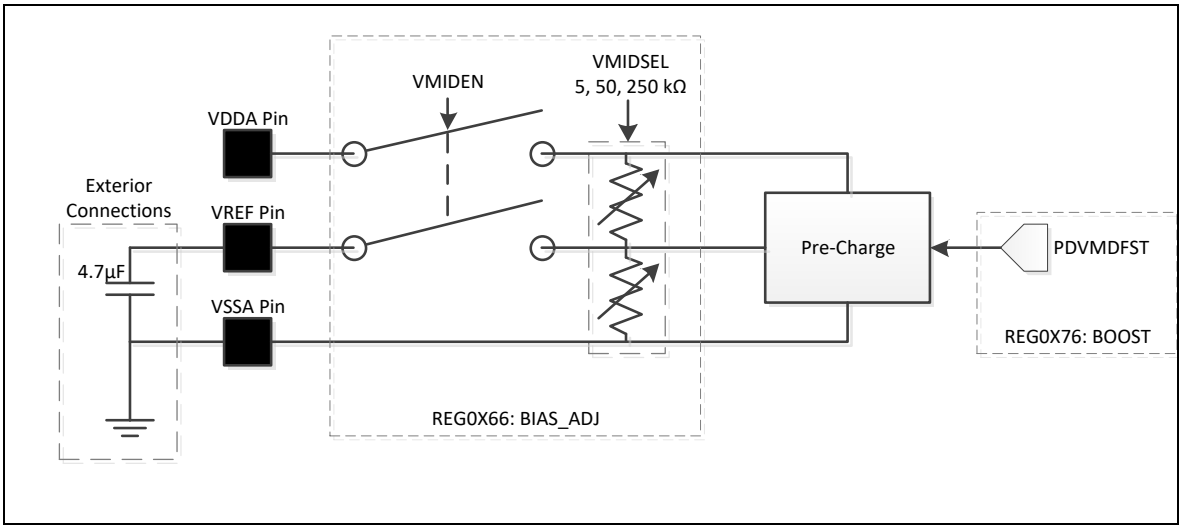


Figure 9 Reference Voltage Circuitry

Note: A pre-charge circuit has been included to reduce the VREF rise time.

Table 9 VREF Impedance Selection

VMIDSEL	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50 KOhm	25 KOhm
10	250 KOhm	125 KOhm
11	5 KOhm	2.5 KOhm

Larger capacitances may be used but that will increase the rise time of VREF and delay the line output signal. A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using **BOOST.PVDMFST REG0X76[13]** to save power or to prevent rapid changes in level due to fluctuations in VDDA. Due to the high impedance of the VREF pin, it is important to use a low leakage capacitor.

6.3 MIC Bias

The NAU88L25B provides one MIC Bias pin (MICBIAS) to power the condenser microphone. The MICBIAS pin can be set by using **MIC_BIAS.POWERUP REG0X74[8]** and the level can be set by using **MIC_BIAS.MICBIASLVL1 REG0X74[2:0]** register. There are internal 2 KOhm resistors for connecting the microphone. This can be enabled enabled using **MIC_BIAS.INT2KB REG0X74[14]** or **MIC_BIAS.INT2KB REG0X74[12]**.

There are two modes available for microphone operation: Low Noise or Low Power. The mode can be enabled by setting **MIC_BIAS.LOWNOISE REG0X74[10]** to '1' for Low-Noise Mode, or to '0' for Low-Power Mode.

6.3.1 MIC Bias Application Notes

If MICBIAS is used in Low-Power Mode **MIC_BIAS.MICBIASLVL1 REG0X74[2:0]** is set to 000 (VDDA) and the capacitor can be 100 nF or 200 nF.

If MICBIAS is used to power analog microphones, it is possible to omit the capacitor, but then the **MIC_BIAS.NOCAP REG0X74[6]** bit must be set High to ensure stability.

If a capacitor is used, **MIC_BIAS.NOCAP REG0X74[6]** must be set LOW to ensure stability. In this case, a capacitor value of 1 µF to 4.7 µF can be used.

Microphones should not draw more than 4 mA from the MICBIAS pin.

7 ADC Digital Block

The NAU88L25B ADC Digital Block uses the output of the 24-bit Analog-to-Digital Converter to perform signal processing to produce a high-quality audio sample stream for the audio path digital interface. **Figure 10** shows the various functions and operations associated with the ADC digital path. This block can be enabled by the **ENA_CTRL.ADCEN REG0X01[8]** register.

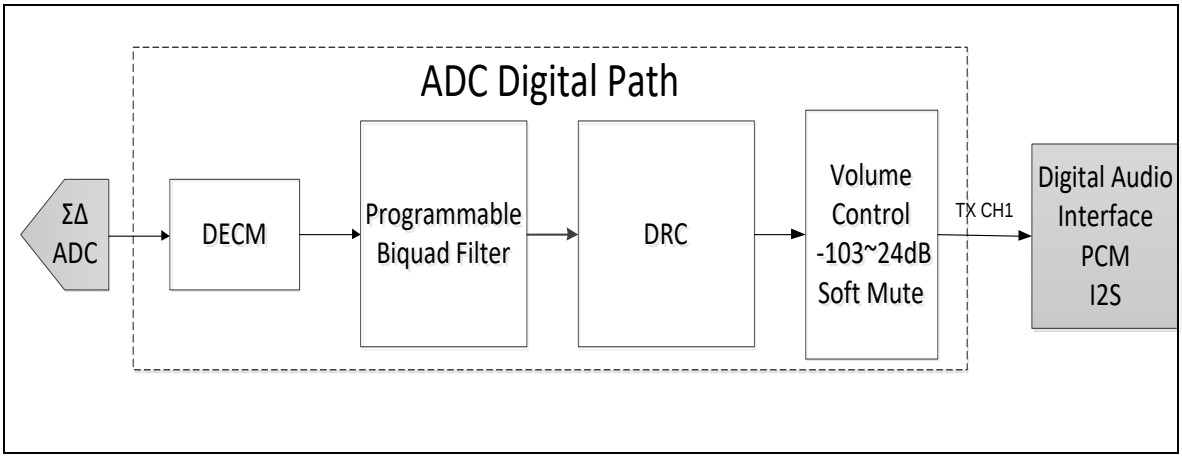


Figure 10 ADC Digital Path

The ADC coding scheme is in twos complement format. The full-scale input level is proportional to VDDA. For example, with a 1.8 V supply voltage, the full-scale level is 1.0 V_{RMS}.

Oversampling is used to improve noise and distortion performance; however this does not affect the final audio sample rate. **ADC_RATE.ADC_RATE REG0X2B[1:0]** can be used to set the ADC Over Sampling Rate from 8 K to 192 KHz.

Independent changeability of the polarity of either ADC output signal on either ADC logic output is often helpful in managing the audio phase of signal processing. This can minimize any audio processing that may otherwise be required as the data is passed to other stages in the system.

7.1 Sigma Delta Modulator and Decimator

The NAU88L25B includes Sigma Delta Modulation with decimation filtering when encoding analog signals into digital signals to reduce aliasing during sample rate conversion or downsampling. This cost-effective methodology improves the accuracy of the signal conversion without introducing complexity to the design.

7.2 ADC Programmable Bi-Quad Filters

The NAU88L25B has 3 dedicated digital Bi-Quad Filters. One is for the ADC path; two are for the DAC path (one for each channel). The Bi-Quad Filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain quotient of this second order quadratic function:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The Bi-Quad Filter coefficients A_1, A_2, B_0, B_1, B_2 are represented in the 3.16 format shown in **Figure 11** and **Figure 12**. The Bi-Quad Filter coefficient registers are listed in**Table 10.**

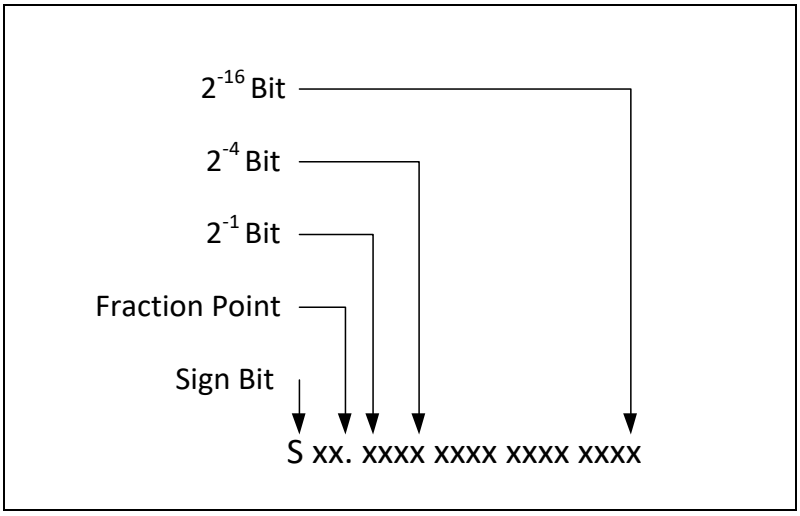


Figure 11 Bi-Quad Filter Coefficient Number Format

Each Bi-Quad Coefficient has 19 bits in Sxx.16 format where:

- S is the sign bit (1 bit),
- xx are integers (2 bits)
- 16 fractional bits (16 bits)

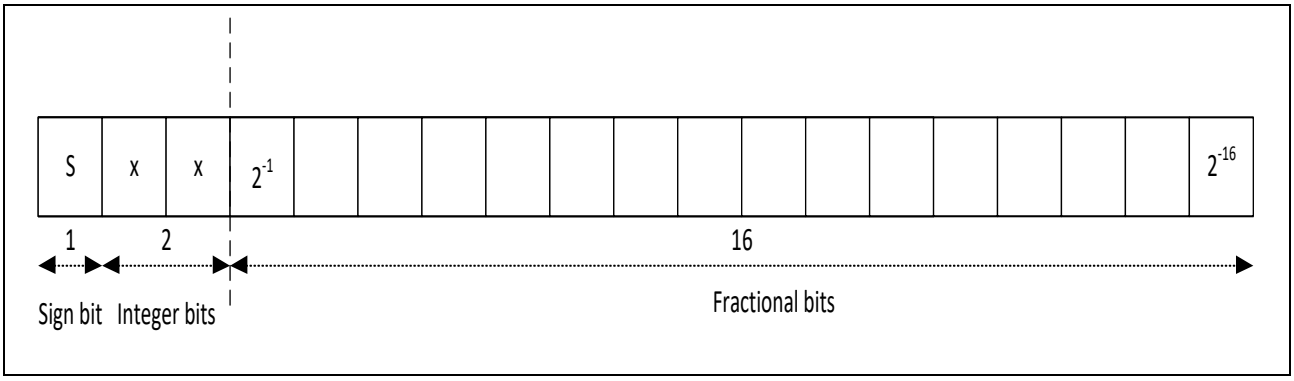


Figure 12 Bi-Quad Filter Coefficient Bit Map

Table 10 Bi-Quad Filter Coefficient Register Locations

Coefficient	Register Locations
A1	**BIQ_COF2.BIQ_A1_H REG0X22[2:0]** and **BIQ_COF1.BIQ_A1_L REG0X21[15:0]**
A2	**BIQ_COF4.BIQ_A2_H REG0X24[2:0]** and **BIQ_COF3.BIQ_A2_L REG0X23[15:0]**
B0	**BIQ_COF6.BIQ_B0_L REG0X26[2:0]** and **BIQ_COF5.BIQ_B0_L REG0X25[15:0]**
B1	**BIQ_COF8.BIQ_B1_L REG0X28[2:0]** and **BIQ_COF7.BIQ_B1_L REG0X27[15:0]**
B2	**BIQ_COF10.BIQ_B2_L REG0X2A[2:0]** and **BIQ_COF9.BIQ_B2_L REG0X29[15:0]**

Note: Values for MCLK, FS, and BCLK are also required for programming the filter. **ENA_CTRL REG0X1** needs to be set to 7FF.

7.2.1 Bi-Quad Filter Application Notes

After the Bi-Quad coefficients are set, the values cannot be cleared by **SOFTWARE_RST REG0X00.** Coefficients can only be cleared by either: (1.) POR (Power ON Reset,) or (2.) Disabling them by choosing **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]** for the ADC (='0') or the DAC ('1') path; **BIQ_COF10.PATH_EN REG0X2A[15]** = '0'; **BIQ_CTRL.BIQ_WRT_EN REG20[4]** = '1'**.**

To enable Write: use **BIQ_CTRL.BIQ_WRT_EN REG0X20[4]** ='1':

- To select the ADC or DACs Bi-Quad Filter function, use **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]** 0b'1 sets both DAC paths with same coefficient; 0b'0 sets ADC path.
- Write **REG0X21** to **REG0X2A** for the coefficients.

After the Bi-Quad coefficients are entered, set **BIQ_CTRL.BIQ_COF_SE REG20X[1]** ='1' to update all the coefficients for the next frame sync clock.

To read back the coefficients, use **BIQ_CTRL.BIQ_WRT_EN REG0X20[4]** ='0':

- Read from **REG0X21** to **REG0X2A.**
- To select the ADC or DACs Bi-Quad Filter, use **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]**.

After programming the coefficients, the Bi-Quad Filter can be enabled by by **BIQ_COF10.PATH_EN REG0X2A[15]**:

- Use **BIQ_CTRL.DAC_PATH_EN REG0X20[3]** for the DAC path
- Use **BIQ_CTRL.ADC_PATH_EN REG0X20[2]** for the ADC path.

Note: The Bi-Quad Filters can be bypassed if they are not used.

When using Bi-Quad filter, the DCR needs to be enabled, too.

7.3 ADC Dynamic Range Compressor

The NAU88L25B includes a Dynamic Range Compressor (DRC) for the ADC channel. The DRC function uses Peak Level Estimation and Static Curve Control.

7.3.1 Level Estimation

The NAU88L25B uses Peak Level Estimation that depends on attack and decay times settings. The values for the peak coefficients are shown in **Table 11**. Attack times can be set with the register **ADC_DRC_ATKDCY.DRC_PK_COEF1_ADC1 REG0X3B[15:12]**. The decay times are similarly set using **ADC_DRC_ ATKDCY.DRC_PK_COEF2_ADC1 REG0X3B[11:8]**. Time constant Ts shown in the register map is the sampling time given by 1/(Sampling Frequency.

Table 11 ADC DRC Level Estimation Time Register Settings

Bits	DRC_PK_ COEF1_ADC1	DRC_PK_ COEF2_ADC1
0000	TS	63*TS
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

7.3.2 Static Curve Control

DRC Static Curve Control supports five programmable sections: NG, EXP, CMP2, CMP1, and LMT that can be enabled by using **ADC_DRC_KNEE_IP12.DRC_ENA_ADC1 REG0X38[15]**. **Figure 13** illustrates the five programmable sections.

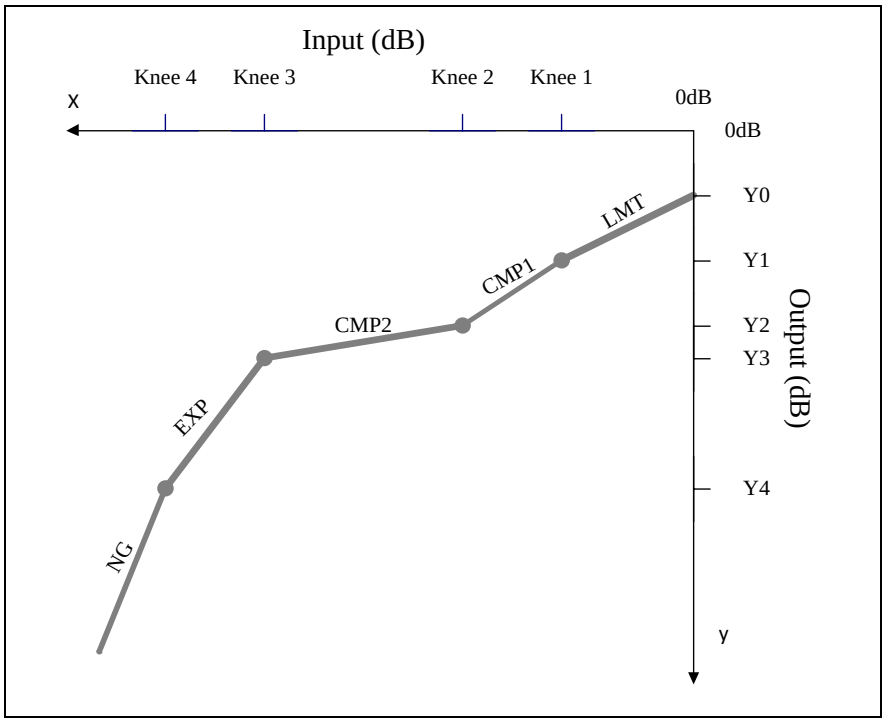


Figure 13 DRC Static Curve Characteristics

Each section is controlled by setting the slope and knee point values in the registers**.**

LMT = Limit

CMP1 = High Compression

CMP2 = Low Compression

EXP = Expansion

NG = Noise Gate

Table 12 identifies the corresponding registers and their locations.

Table 12 ADC DRC Static Curve Control Settings

Section	Slope	Knee Point
LMT	**ADC_DRC_ SLOPES.DRC_LMT_SLP_ADC1 REG0X3A[2:0]**	
CMP1	**ADC_DRC_ SLOPES.DRC_CMP1_SLP_ADC1 REG0X3A[5:3]**	**ADC_DRC_ SLOPES.DRC_KNEE1_IP_ADC1 REG0X38[4:0]**
CMP2	**ADC_DRC_ SLOPES.DRC_CMP2_SLP_ADC1 REG0X3A[8:6]**	**ADC_DRC_ SLOPES.DRC_KNEE2_IP_ADC1 REG0X38[13:8]**
EXP	**ADC_DRC_ SLOPES.DRC_EXP_SLP_ADC1 REG0X3A[11:10]**	**ADC_DRC_ SLOPES.DRC_KNEE3_IP_ADC1 REG0X39[5:0]**
NG	**ADC_DRC_ SLOPES.DRC_NG_SLP_ADC1 REG0X3A[13:12]**	**ADC_DRC_ SLOPES.DRC_KNEE4_IP_ADC1 REG0X39[13:8]**

Note: The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

Y1 = Knee 1

Y0 = Y1 - (Knee 1) * (LMT Slope)

Y2 = (Knee 2 - Knee 1) * (CMP1 Slope) + Y1

Y3 = (Knee 3 - Knee 2) * (CMP2 Slope) + Y2

Y4 = (Knee 4 - Knee 3) * (EXP Slope) + Y3

Note: The Y axis distance adjustments along the static curve cannot exceed 36 dB. The Smooth Knee filter function can be enabled by using the register **ADC_DRC_ KNEE_IP12.DRC_SMTH_ENA_ADC1 REG0X38[7]**.

As shown in **Table 13,** two registers are used to set the attack time and decay time: Attack time can be set using **ADC_DRC_ ATKDCY.DRC_ATK_ADC1REG0X3B[7:4]**. Decay time can be set using **ADC_DRC_ ATKDCY.DRC_DCY_ADC1 REG0X3B[3:0]**.

Table 13 ADC Attack and Decay Time Register Settings

BITS	DRC_ATK_ ADC1_CH##	DRC_DCY_ ADC1_CH##
0000	TS	63*TS
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts

BITS	DRC_ATK_ ADC1_CH##	DRC_DCY_ ADC1_CH##
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

7.4 ADC Digital Volume Control

The Digital Volume Control enables adjustment of the effective audio volume coming from the ADC using a two-stage volume control. This allows the gain to be adjusted from -103 dB to +24 dB. Also included is a mute value to reduce the ADC output to '0'. To adjust the channel volume controls, use **ACDC_CTRL.DGAIN_ADC0 REG0X30[8:0]**.

7.4.1 ADC Digital Volume Control Application Notes

CLK_DIVIDER.CLK_ADC_PL REG0X03[10] sets the ADC clock polarity.

CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6] can reduce the clock speed.

TDM_CTRL.ADC_TX_SEL REG0X1B[1:0] allows ADC data put into a selected time slot to output on the I2S Interface.

Note: It is recommended to match **ADC_RATE.ADC_RATE_ REG0X2B[1:0]** with **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** according to Table 14.

Table 14 ADC_RATE and CLK_ADC_SRC Pairs

ADC_RATE	CLK_ADC_ SRC
00(OSR=32)	11(CODEC 1/8)
01(OSR=64)	10(CODEC1/4)
10(OSR=128)	01(CODEC 1/2)
11(OSR=256)	00(CODEC CLK)

7.5 Digital Audio Interfaces

Following signal processing by the various functions in the Analog-to-Digital Converter Block, data passes to the PCM and I2S Digital Audio Interfaces. The NAU88L25B can be configured as either the Master or the Slave. The NAU88L25B Audio CODEC supports six audio modes: Right Justified, Left Justified, I2S, PCM A, PCM B, and PCM Time Slot. Time Division Multiplexing of Audio data can be handled by the NAU88L25B in I2S Mode, PCM A Mode, PCM B Mode, and PCM Offset Mode.

See **Chapter 11** for detailed information on the various conditions, modes, and timing diagrams.

8 DAC Digital Block

The NAU88L25B DAC Digital Block uses 24-bit signal processing to generate high-quality analog audio with a 16-bit digital sample stream input. As shown in **Figure 14**, the DAC digital path consists of Digital Audio Interfaces, Volume Control, Programmable Bi-Quad Filters, Dynamic Range Compression, a digital decimator/filter, and a sigma-delta modulator. The DAC has left and right audio channels. The two DAC channels are enabled by the **ENA_CTRL.LDACEN REG0X01[9]** and **ENA_CTRL.RDACEN REG0X01[10]** registers. The DAC coding scheme is in twos complement format. The full-scale input level is proportional to VDDA. For example, with a 1.8 V supply voltage, the full-scale level is 1.0 V_{RMS}.

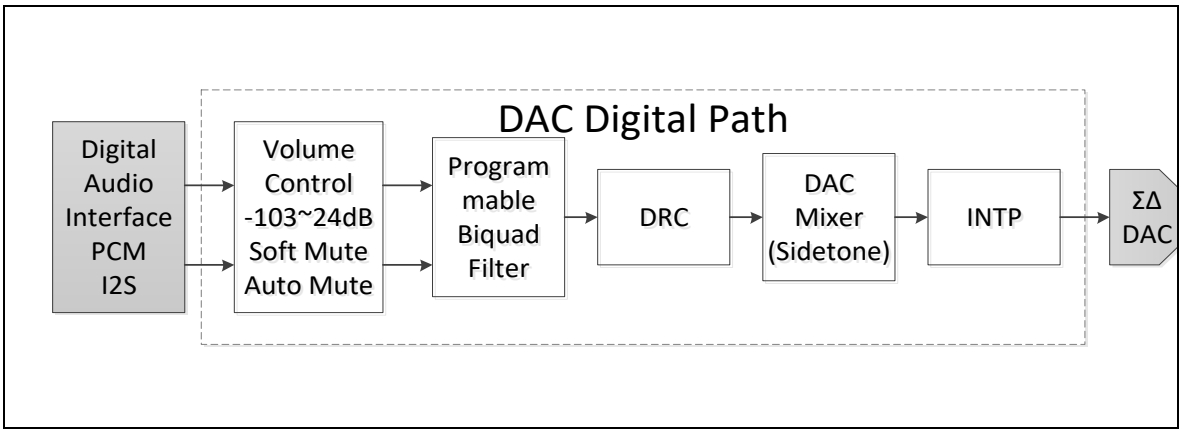


Figure 14 DAC Digital Path

The oversampling rate of the DAC can be changed from 32x to 256x for improved audio performance at higher power consumption using **DAC_CTRL1.DAC_RATE REG0X2C[2:0]**. The DAC output signal polarity can be changed **DAC_CTRL2.DACPL REG0X2D[3]**. This can help minimize audio processing that may be required as the data is passed from other stages of the system.

8.1 Digital Audio Interfaces

The Digital Audio Interface passes PCM and I2S data into the DAC block for processing by Volume Control, the Programmable Bi-Quad Filters, the DRC, the Mixer and out to the Sigma Delta Modulator.

The NAU88L25B can be configured as either the Master or the Slave. The NAU88L25B Audio CODEC supports six audio modes: Right Justified, Left Justified, I2S, PCM A, PCM B, and PCM Time Slot. Time Division Multiplexing of Audio data can be handled by the NAU88L25B in I2S Mode, PCM A Mode, PCM Mode, PCM B, and PCM Offset Mode.

See **Chapter 11** for detailed information on the various conditions, modes, and timing diagrams.

8.2 DAC Digital Volume Control

The Left and Right DAC channels, DACL (Left) and DACR (Right), have separate digital volume controls to allow the gain to be adjusted from -103 dB to +24 dB in 0.5 dB steps. The two channels are selected through the **DACL_CTRL.DGAINL_DAC REG0X33[7:1]** and **DACR_CTRL.DGAINR_DAC REG0X34[7:1]** registers. The channels are adjustable separately and are accessed through **DACL_CTRL.DAC_CH_SEL0 REG0X33[9]** and **DACR_CTRL.DAC_CH_SEL1 REG0X34[9]** respectively. Also included is a mute setting that will reduce the path gain to a minimum; control is achieved through registers **DACL_CTRL.DGAINL_DAC REG0X33[0]** and **DACR_CTRL.DGAINR_DAC REG0X34[0]**

8.2.1 DAC Soft Mute and Soft UnMute

The Soft Mute function ramps the DAC digital volume down to zero when enabled by **MUTE_CTRL.SMUTE_EN REG0X31[9** When Soft Mute is disabled (Soft UnMute), the volume increases to the register specified volume level for each channel. This feature is helpful for using the DAC without introducing pop- and-click sounds.

8.2.2 DAC Volume Auto-Attenuation

Auto-Attenuation can greatly increase the perceived Signal-to-Noise-Ratio (SNR) during playback of silence. The last analog output stage is attenuated such that the noise contribution of the preceding stages is eliminated. Attenuation of the analog output on a DAC path when the digital input represents a zero signal needs to be done gradually to avoid audible pops due to sudden offset changes. It is desirable to slowly ramp down the gain of the analog output stage to the maximum the attenuation level. This function is referred to as auto-attenuation.

Additionally, the auto attenuation logic can be used to attenuate the analog output manually, saving some software routines and allowing pop-less ramp up and ramp down of the analog outputs with few register writes. Attenuation can be enabled manually or automatically.

Auto-attenuation requires that the **MUTE_CTRL.AMUTE_EN REG0X31[11]** register must be enabled and that the **HSVOL_CTRL.MUTE_HSPGA1 REG0X32[12]** and **HSVOL_CTRL.MUTE_HSPGA0 REG0X32[13]** must be '0'. When **HSVOL_CTRL.HSPGA_MUTE_AUTO_MODE REG0X32[14]** is set ='1', the auto-attenuate process starts with the detection of a zero signal at the I2S port. If both the left and the right channel receive 1024 consecutive samples of '0', then the auto-attenuate will read and store the value of the Headset Driver Volume Control registers, **HSVOL_CTRL.HSPGA1_VOL REG0X32[11:6]** and **HSVOL_CTRL.HSPGA0_VOL REG0X32[5:0]** into temporary registers and attenuate the headset driver output by 1 dB for every 128 samples, until -54 dB is reached (54 steps maximum). The result is that the headset output drivers are fully attenuated.

If, at any time, the I2S DACIN signal receives non-zero signal samples, the headset output driver gain is increased by 1 dB per step and in 1, 16, 32, or 128 samples- per-step (programmable by the register **MUTE_CTRL.PGA_SMUTE_STEP REG0X[15:14]**, because of the trade-off between pop and loss of audio). The gain will be stepped up until the original gain settings of the HSPGA1_VOL and HSPGA2_VOL registers are reached.

Manual-attenuation can be implmented in the NAU88L25B by enabling the manual attenuate registers **MUTE_CTRL.AMUTE_EN REG0X31[11]** and **HSVOL_CTRL.HSPGA_MUTE_EN REG0X32[15]**. Also, the **HSVOL_CTRL.MUTE_HSPGA1 REG0X32[12]** and **HSVOL_CTRL.MUTE_HSPGA0_ REG0X32[13]** registers must be '0'. Manual-attenuate will ignore the DAC input sample values read and store the value of the headset driver volume control (**HSPGA1_VOL** & **HSPGA0_VOL**) into temporary registers and attenuate the headset driver output by 1 dB for every 128 samples, until -54 dB is reached (54 steps maximum). Then, the headset output drivers are fully attenuated.

If, at any time, the manual-attenuate is disabled, the headset output driver gain is increased by 1 dB per step and in 1, 16, 32 or 128 samples-per-step (programmable by the register PGA_SMUTE_STEP, because of the trade-off between pop and loss of audio). The gain will be stepped up until the original gain register settings (**HSPGA1_VOL** and **HSPGA0_VOL**) are reached.

When both **HSVOL_CTRL.HSPGA0** and **HSVOL_CTRL.HSPGA1** are '1', the headphone driver will be muted without either auto mute or manual mute. **Table 15** provides the register settings for the mute operation.

Table 15 Auto and Manual Mute Register Settings

AUTO-MUTE	MANUAL-MUTE	REGISTER NAME
1	1	AMUTE_EN(REG0X31)
1	x	HSPGA_ MUTE_AUTO_MODE(REG0X32)
x	1	HSPGA_ MUTE_EN(REG0X32)
0	0	MUTE_ HSPGA0(REG0X32)
0	0	MUTE_ HSPGA1(REG0X32)

8.3 DAC Programmable Bi-Quad Filters

The NAU88L25B has 3 dedicated digital Bi-Quad Filters. Two for the DAC path (one for each channel) and one for the ADC path. The Bi-Quad Filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain consisting of a second order quadratic function:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The Bi-Quad Filter coefficients A_1, A_2, B_0, B_1, B_2 are represented in the 3.16 format shown in **Figure 15** and **Figure 16.** The register locations are listed in **Table 16**.

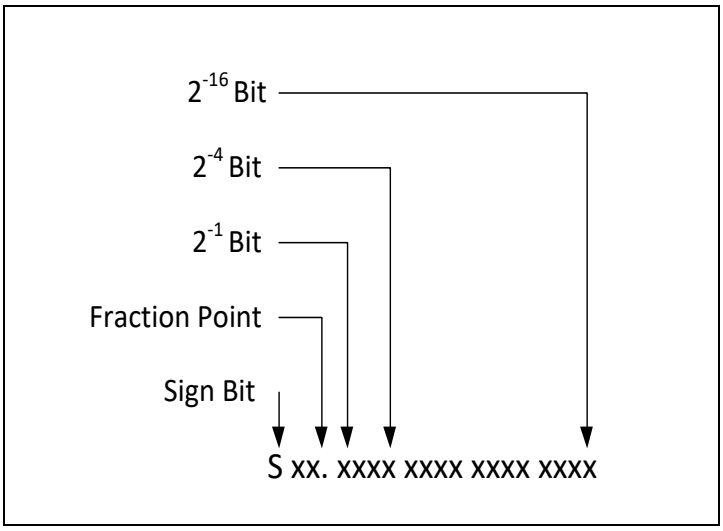


Figure 15 Bi-Quad Filter Coefficient Number Format

Each Bi-Quad Coefficient has 19 bits in Sxx.16 format where:

- S is the sign bit (1 bit),
- xx are integers (2 bits)
- 16 fractional bits (16 bits)

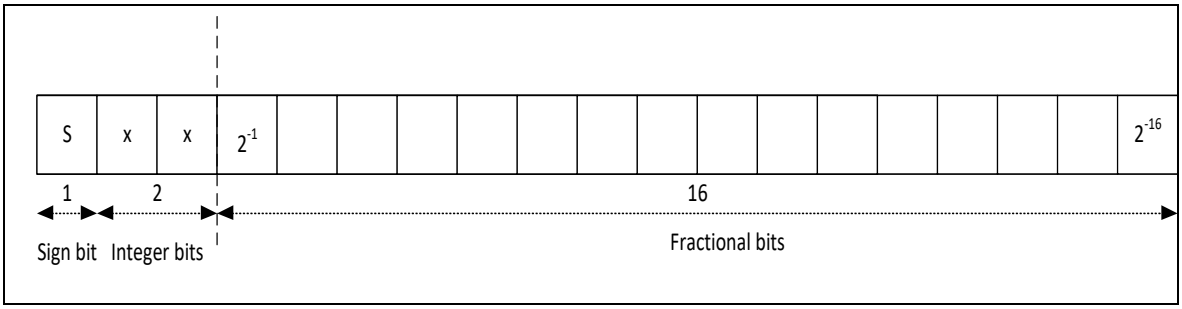


Figure 16 Bi-Quad Filter Coefficient Bit Map

Table 16 Bi-Quad Filter Coefficient Register Locations

Coefficient	Register Location
A1	**BIQ_COF2.BIQ_A1_H REG0X22[2:0]** and **BIQ_COF1.BIQ_A1_L REG0X21[15:0]**
A2	**BIQ_COF4.BIQ_A2_H REG0X24[2:0]** and **BIQ_COF3.BIQ_A2_L REG0X23[15:0]**
B0	**BIQ_COF6.BIQ_B0_L REG0X26[2:0]** and **BIQ_COF5.BIQ_B0_L REG0X25[15:0]**
B1	**BIQ_COF8.BIQ_B1_L REG0X28[2:0]** and **BIQ_COF7.BIQ_B1_L REG0X27[15:0]**
B2	**BIQ_COF10.BIQ_B2_L REG0X2A[2:0]** and **BIQ_COF9.BIQ_B2_L REG0X29[15:0]**

Note: Values for MCLK, FS, and BCLK are also required for programming the filter. **ENA_CTRL REG0X1** needs to be set to 7FF.

8.3.1 Bi-Quad Filter Application Notes

After the Bi-Quad coefficients are set, the values cannot be cleared by **SOFTWARE_RST REG0X00**. Coefficients can only be cleared by either: (1.) POR (Power ON Reset,) or (2.) Disabling it by choosing **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]** for ADC (='0') or DAC (='1') path; **BIQ_COF10.PATH_EN REG0X2A[15**] = '0'; **BIQ_CTRL.BIQ_WRT_EN REG20[4]** = '1'.

To enable Write: use **BIQ_CTRL.BIQ_WRT_EN REG0X20[4]** = '1':

- To select the ADC or DACs Bi-Quad Filter function, use **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]:** 0b'1 sets both DAC paths with same coefficient; 0b'0 sets ADC path.
- Write Write **REG0X21** to **REG0X2A** for the coefficients.

After the Bi-Quad coefficients are entered, set **BIQ_CTRL.BIQ_COF_SE REG20X[1]** ='1' to update all coefficients for the next frame sync clock.

To read back coefficients, use **BIQ_CTRL.BIQ_WRT_EN REG0X20[4]** ='0':

- Read from from **REG0X21** to **REG0X2A.**
- To select the ADC or DACs Bi-Quad Filter function, use **BIQ_CTRL.BIQ_PATH_SE REG0X20[0]**.

After programming the coefficients, the Bi-Quad Filter can be enabled by **BIQ_COF10.PATH_EN REG0X2A[15]**:

- Use **BIQ_CTRL.DAC_PATH_EN REG0X20[3]** for the DAC path.
- Use **BIQ_CTRL.ADC_PATH_EN REG0X20[2]** for the ADC path.

Note: The Bi-Quad Filters can be bypassed if they are not used.

Bi-Quad needs to work with DRC enabled

8.4 Dynamic Range Control

The NAU88L25B Audio CODEC includes a Dynamic Range Compressor (DRC) for the two DAC channels. The DRC function for the DAC channels uses Peak Level Estimation and Static Curve Control in the same way as for the ADC explained in **Chapter 7.3.** However, different control registers are used for the DAC channels.

Note: DRC needs to be used carefully in combination with the Crosstalk function. A small Crosstalk signal may be filtered out by the DRC.

8.4.1 Level Estimation

The NAU88L25B uses Peak Level Estimation that depends on attack and decay times settings. The values for the peak coefficients are shown in **Table 17**. Attack times can be set with the register **DAC_DRC_ATKDCY.DRC_PK_COEF1_DAC REG0X48[15:12]** Decay times are set by register **DAC_DRC_ATKDCY.DRC_PK_COEF2_DAC REG0X48[11:8]**,.

Table 17 DAC Level Estimation Attack and Decay Time Settings

BITS	DRC_PK_COEF1_DAC	DRC_PK_COEF2_DAC
0000	TS	63*TS
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Note: Time constant (Ts) in the register map is the sampling time given by 1/(Sampling Frequency)

8.4.2 Static Curve Contol

The DRC static curve supports five programmable sections and can be enabled by using the register **DAC_DRC_ KNEE_IP12.DRC_ENA_DAC_ REG0X45[15]**. **Figure 17** shows the five programmable sections and **Table 18** shows the related control registers for the DAC DRC.

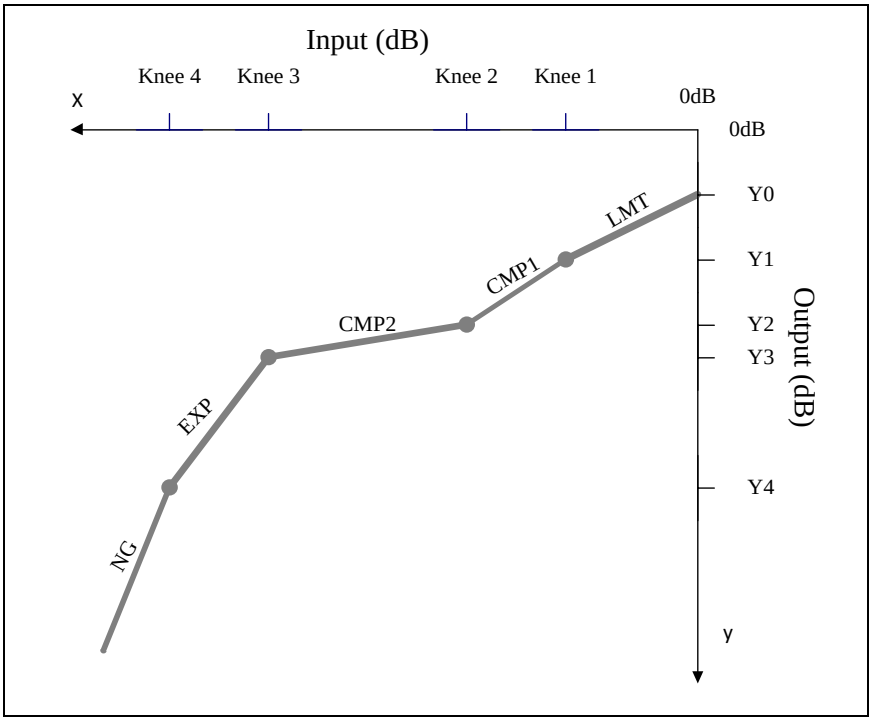


Figure 17 DRC Static Curve Characteristics

Each section is controlled by setting the slope and knee point values in the registers**.**

LMT = Limit

CMP1 = High Compression

CMP2 = Low Compression

EXP = Expansion

NG = Noise Gate

Table 18 identifies the corresponding registers and their locations.

Table 18 DAC DRC Static Curve Control Registers

Section	Slope	Knee Point
LMT	**DAC_DRC_ SLOPES.DRC_LMT_SLP_DAC REG0X47[2:0]**	
CMP1	**DAC_DRC_ SLOPES.DRC_CMP1_SLP_DAC REG0X47[5:3]**	**DAC_DRC_ KNEE_IP12.DRC_KNEE1_IP_DAC REG0X45[13:8]**
CMP2	**DAC_DRC_ SLOPES.DRC_CMP2_SLP_DAC REG0X47[8:6]REG0X47[8:6]**	**DAC_DRC_ KNEE_IP12.DRC_KNEE2_IP_DAC REG0X45[4:0]**

Section	Slope	Knee Point
EXP	**DAC_DRC_ SLOPES.DRC_EXP_SLP_DAC REG0X47[10:9]**	**DAC_DRC_ KNEE_IP34.DRC_KNEE3_IP_DAC REG0X46[13:8]**
NG	**DAC_DRC_ SLOPES.DRC_NG_SLP_DAC REG0X47[13:12]**	**DAC_DRC_ KNEE_IP34.DRC_KNEE4_IP_DAC REG0X46[5:0]**

Notes: The Smooth Knee function can be enabled by using the register **DAC_DRC_ KNEE_IP12.DRC_SMTH_ENA_DAC REG0X45[7]**.

The attack time can be set using **DAC_DRC_ATKDCY.DRC_ATK_DAC REG0X48[7:4]**.

The decay time can be set using **DAC_DRC_ATKDCY.DRC_DCY_DAC REG0X48[3:0]**.

Table 19 provides the DAC Static Curve Attack and Decay time and bit settings.

Table 19 DAC Static Curve Attack and Decay Time Settings

BITS	DRC_ ATK_DAC	DRC_ DCY_DAC
0000	TS	63*TS
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

8.5 DAC Path Digital Mixer with Sidetone

The NAU88L25B implements a channel-based digital mixer for DAC output that can select from ADC input channels, I2S channels, and the opposing DAC output channel to mix into the output of the two DAC channels. **Figure 18** shows the mixer and its related registers, while **Table 20** identifies the registers and their associated channels.

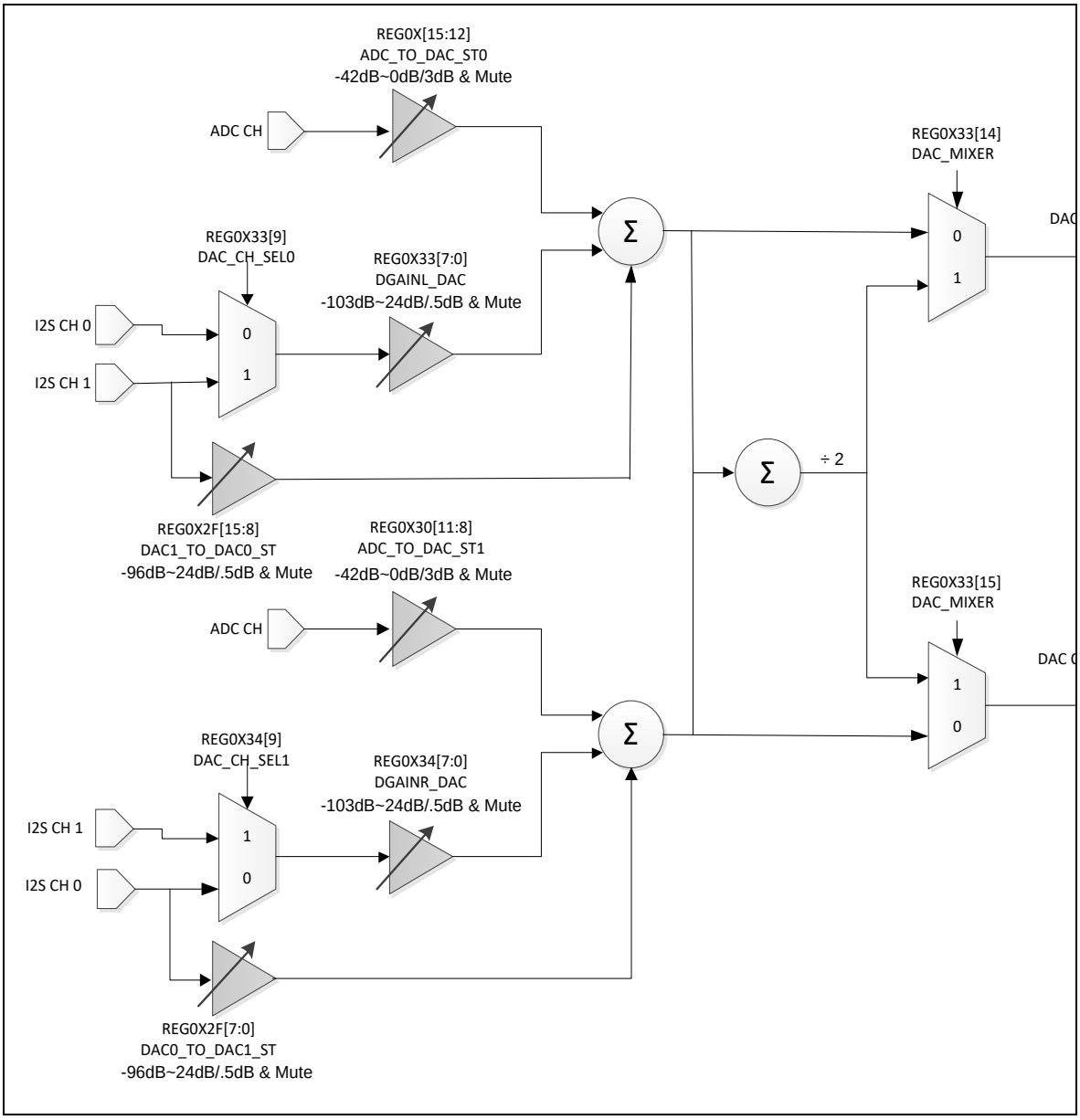


Figure 18 DAC Path Digital Mixer with Sidetone

The commands shown in **Figure 18** can be found in the **ADC_ DGAIN_CTRL REG0X32**, **DACL_CTRL REG0X33**, and **DACR_CTRL REG0X34** registers for the DAC Left and Right channels. For sidetone from ADC path, Reg0x1C[7].ADDAP0 needs to turn on.

Table 20 DAC Digital Mixer Control Registers

Function	Left Channel	Right Channel
DAC Output Mixer Select	**DACL_CTRL.REG0X33[14]**	**DACL_CTRL.REG0X33[15]**
ADC Channel Gain	**ADC_DGAIN_CTRL.REG0X30[15:12]**	**ADC_DGAIN_CTRL.REG0X30[11:8]**
I2S Channel Select	**DACL_CTRL.REG0X33[9]**	**DACR_CTRL.REG0X34[9]**
I2S Channel Gain	**DACL_CTRL.REG0X33[7:0]**	**DACR_CTRL.REG0X34[8:0]**

8.5.1 DAC Application Notes

The following registers are also significant in optimizing the application design and performance:.

CLK_DIVIDER.CLK_DAC_PL REG0X03[11] inverts the clock polarity.

CLK_DIVIDER.CLK_DAC_SRC REG0X03[5:4] scales the clock speed.

Two registers select the Left and Right Channel slot numbers in I2C/PCM TDM Mode:

- **TDM_CTRL.DAC_LEFT_SEL_REG0X1B[7:6]** selects the DAC Channel L slot number in I2C/PCM TDM Mode.
- **TDM_CTRL.DAC_RIGHT_SEL_REG0X1B[5:4]** selects the DAC Channel R slot number in I2C/PCM TDM Mode.

DAC_CTRL1.DISABLE_DEM REG0X2C[15] disables DEM control to RateConvert2 module.

DAC_CTRL1.DAC_RATE REG0X2C[2:0] sets the DAC Over Sample Rate.

DAC_CTRL2.DEM_DITHER REG0X2D[15:12] sets the probability of first order dynamic element matching dither.

DAC_CTRL2.DAC_STEP_SEL REG0X2D[6:4] sets the DAC output delay.

DAC_CTRL2.DACPL REG0X26[3] sets the DAC output polarity.

MODE_CTRL.DACIN_SRC REG0X4C[2:0] selects the DAC input source.

MUTE_CTRL.DAC_ZC_EN REG0X31[12] enables zero crossing on the DAC output to reduce pops or clicks when changing the gain.

DACL_CTRL.DACMIXER REG0X31[15:14] enables half power mixing of the two DAC output channels.

9 Clocking and Sample Rates

9.1 Master System Clock

The internal clocks for the NAU88L25B are derived from a common internal clock source, **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]**. This Master System Clock (MCLK) can be set directly by the MCLK pin input or can be generated from a Frequency Locked Loop (FLL) using the MCLK_PIN, the Bit Clock (BCLK) or Frame Sync (FS) as a reference. While most of the common audio sample rates can be derived directly from typical MCLK frequencies, the FLL provides additional flexibility for a wide range of MCLK inputs or as a free running clock in the absence of an external reference.

Figure 19 shows the registers used to adjust or select the MCLK and the ADC_CLK clock frequencies.

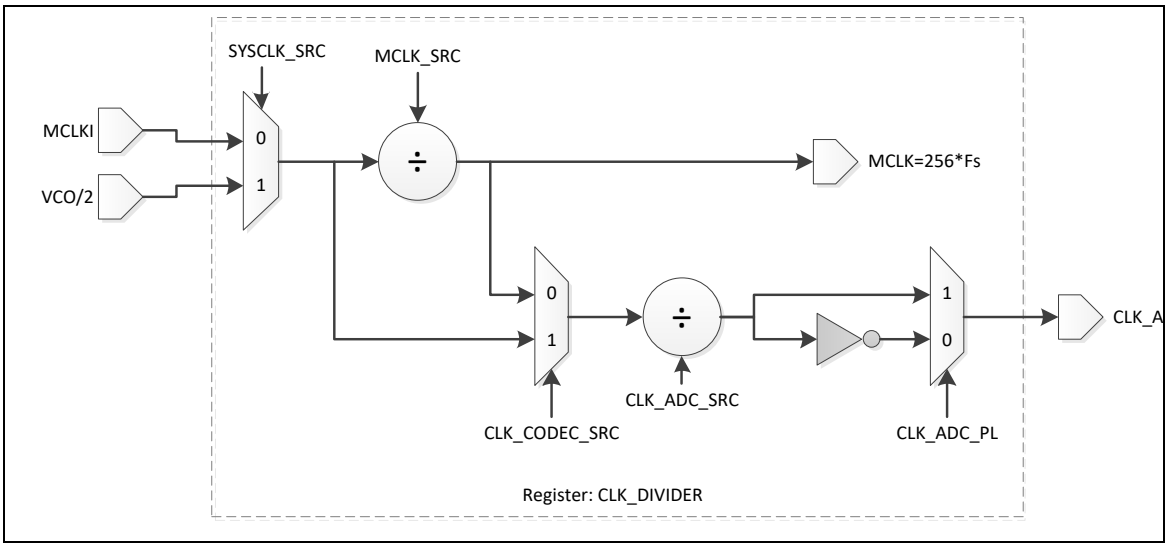


Figure 19 MCLK and ADC_CLK Frequency Selection

CLK_DIVIDER.MCLK_SRC REG0X03[3:0 sets the MCLK_SRC register, as shown in **Table 21**.

Table 21 MCLK_SRCRegister Settings

Bits	MCLK_SRC
0000	Divide by 1
0001	Invert
0010	Divide by 2
0011	Divide by 4
0100	Divide by 8
0101	Divide by 16
0110	Divide by 32
0111	Divide by 3
1001	Invert
1010	Divide by 6

Bits	MCLK_SRC
1011	Divide by 12
1100	Divide by 24
1101	Divide by 48
1110	Divide by 96
1111	Divide by 5

Use the **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** register to set the ADC_SRC register**.**

Table 22 identifies the register settings for the ADC_SRC clock frequencies.

Table 22 CLK_ADC_ SRC Register Settings

Bits	CLK_ADC_ SRC
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

BCLK, LRC, and FS are illustrated in **Figure 20** The register settings for BCLK are listed in **Table 23.**

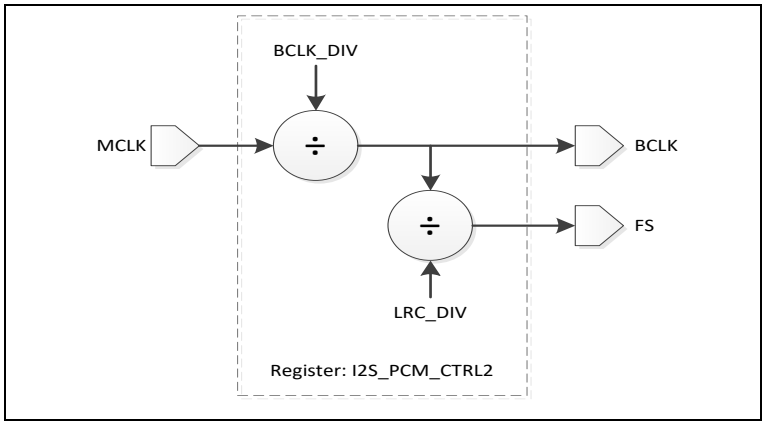


Figure 20 BCLK, LRC and FS Frequency Selection

Table 23 BCLK_DIV Register Settings

Bits	BCLK_DIV
000	Divide by 2
001	Divide by 4
010	Divide by 8
011	Divide by 16
100	Divide by 32
101	Divide by 64

Register **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]** sets BCLK from SYSCLK in Master Mode. The register settings for LRC are shown in **Table 24.**

Table 24 LRC_DIV Register Settings

Bits	LRC_DIV
00	Divide by 256
01	Divide by 128
10	Divide by 64
11	Divide by 32

Register **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** and BCLK are used to set the FS. MCLK, internal clock frequency, must be running at 256*Fs (Fs = sample rate in Hz) in order to achieve the best performance. For example, when targeting 48 kHz sample rate audio, the MCLK must be set to 256*48k = 12.288 MHz. When the input clock MCLKI is higher than this speed, the **CLK_DIVIDER.MCLK_SRC REG0X03[4:0]** provides the required flexible division selection.

9.2 Over Sampling Rate

Over Sampling Rate (OSR) is defined as CLK_ADC frequency divided by the audio sample rate (Fs).

$$OSR = \frac{CLK\_ADC}{Fs}$$

The available Over Sampling Rates are 32, 64, 128 or 256. The OSR is set in the **ADC_RATE.ADC_RATE REG0X2B[1:0]** register. The CLK_ADC frequency is set by the **CLK_DIVIDER.CLK_CODEC_SRCREG0X03[13]** register and the **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** registers.

Note that the OSR and Fs values must be selected such that the maximum frequency of CLK_ADC is less than 6.144 MHz. When CLK_ADC is determined, **ADC_RATE.ADC_RATE REG0X2B[1:0]** should be set to provide appropriate down sampling through digital filters.

Example 1

To configure Fs = 48 kHz, MCLK = (256*Fs) = 12.288 MHz, and CLK_ADC = 6.144 MHZ

Set **CLK_DIVIDER.CLK_CODEC_SRC REG0X03[13]** = 1'b0, **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** = 2'b01, and **ADC_RATE.ADC_RATE REG0X2B[1:0],** OSR = 2'b10 (128)

Example 2

To configure Fs = 16 kHz, MCLKI = 12.288 MHz, and CLK_ADC = 4.096 MHz

Set **CLK_DIVIDER.MCLK_SRC REG0X03[4:0]** = 3'b111 (Divide MCLKI by 3) to get MCLK = (256*Fs) = 4.096MHz

Set **CLK_DIVIDER.CLK_CODEC_SRC REG0X03[13]** = 1'b0, **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** = 2'b00, and OSR = 2'b11 (256)

9.2.1 Clocking Application Notes

To avoid audible glitches, all clock configurations must be setup before enabling playback.

If MCLK is at a higher frequency than desired, **CLK_DIVIDER.MCLK_SRC REG0X03[3:0]** can be used to scale the MCLK frequency.

The GPIO1 pin can be set to output a clock with frequency scaled by the register **CLK_DIVIDER.CLK_GPIO_SRC REG0X03[9:8]** and can be enabled using the register **GPIO12_CTRL.GPIO1SEL REG0X1A[6:4]**.

CLASSG_CTRL.CLASSG_EN REG0X50[0] and **CLASSG_CTRL.CLASSG_CLK_SRC REG0X50[15:14]** are used to enable a slower clock to de-bounce the button/accessory detect inputs and set the time period for volume updates when zero crossing is enabled.

It is recommended to disable SYSCLK_SRC and then re-enable it after the entire setting shave been updated.

When FLL uses Free Running Mode, the NAU88L25B CODEC needs to be set as a master in **I2S_PCM_CTRL2.MS0 REG0X1D[3]** = 1.

9.3 I2S/PCM Clock Generation

In Master Mode, BCLK is derived from MCLK via a programmable divider set by **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]** and the FS is derived from BCLK via a programmable divider **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]**.

In order to select specific FS values, both **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]** and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** must be set according to the block diagram seen in **Figure 20** and this equation:

$$BCLK = FS \times data\ length \times channels$$

Example 1

To configure Fs = 48 kHz for 16-bit data to be sent to the I2S bus (2 channels):

BCLK = 48000*16*2 = 1.536 MHz and MCLK = 48000*256 = 12.288 MHz

Set **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]**= 3'b011 (8) and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** = 2'b11 (32)

To configure Fs = 48 kHz for 32-bit data to be sent to the I2S bus (2 channels):

BCLK = 48000*32*2 = 3.073 MHz and MCLK = 48000*256 = 12.288 MHz

Set **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]**= 3'b010 (4) and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** = 2'b10 (64))

Example 2

To configure Fs = 16 kHz for 16-bit data to be sent to the I2S bus (2 channels):

BCLK = 16000*16*2 = 512 kHz and MCLK = 16000*256 = 4.096 MHz

Set **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]** = 3'b011 (8) and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** = 2'b11 (32)

To configure Fs = 16 kHz for 32-bit data to be sent to the I2S bus (2 channels):

BCLK = 16000*32*2 = 1.024 MHz and MCLK = 16000*256 = 4.096 MHz

Set **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]** = 3'b100 (4) and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** = 2'b10 (64))

Example 3

To configure Fs = 16 kHz for 32-bit data to be sent to the I2S TDM bus (4 channels)

BCLK = 16000*32*4 = 2.048 MHz and MCLK = 16000*256 = 4.096 MHz

Set **I2S_PCM_CTRL2.BCLK_DIV REG0X1D[2:0]**= 3'b001 (2) and **I2S_PCM_CTRL2.LRC_DIV REG0X1D[13:12]** = 2'b01 (128)

9.4 Frequency Locked Loop (FLL)

The integrated Frequency Locked Loop (FLL) can be used to generate a System Clock (SYSMCLK) from a variety of reference sources such as, MCLK, BCLK, and FS or the FLL can be set as a Free Running Clock in the absence of an external reference. The FLL can also create a stable SYSMCLK from less stable sources due to its tolerance for jitter. To select among the various clock sources, use **FLL3.FLL_CLK_REF_SRC REG0X06[11:10]** or to run the FLL as a Free Running Clock, enable **FLL6.DCO_EN REG0X09[15]**, set **FLL_VCO_RSV.DOUT2VCO_RSVREG0X0A[15:0]** to 16'hF13C and set **BOOST.BIASEN REG0X76[12**] = '1'. **Figure 21** shows the block diagram of the Frequency Locked Loop.

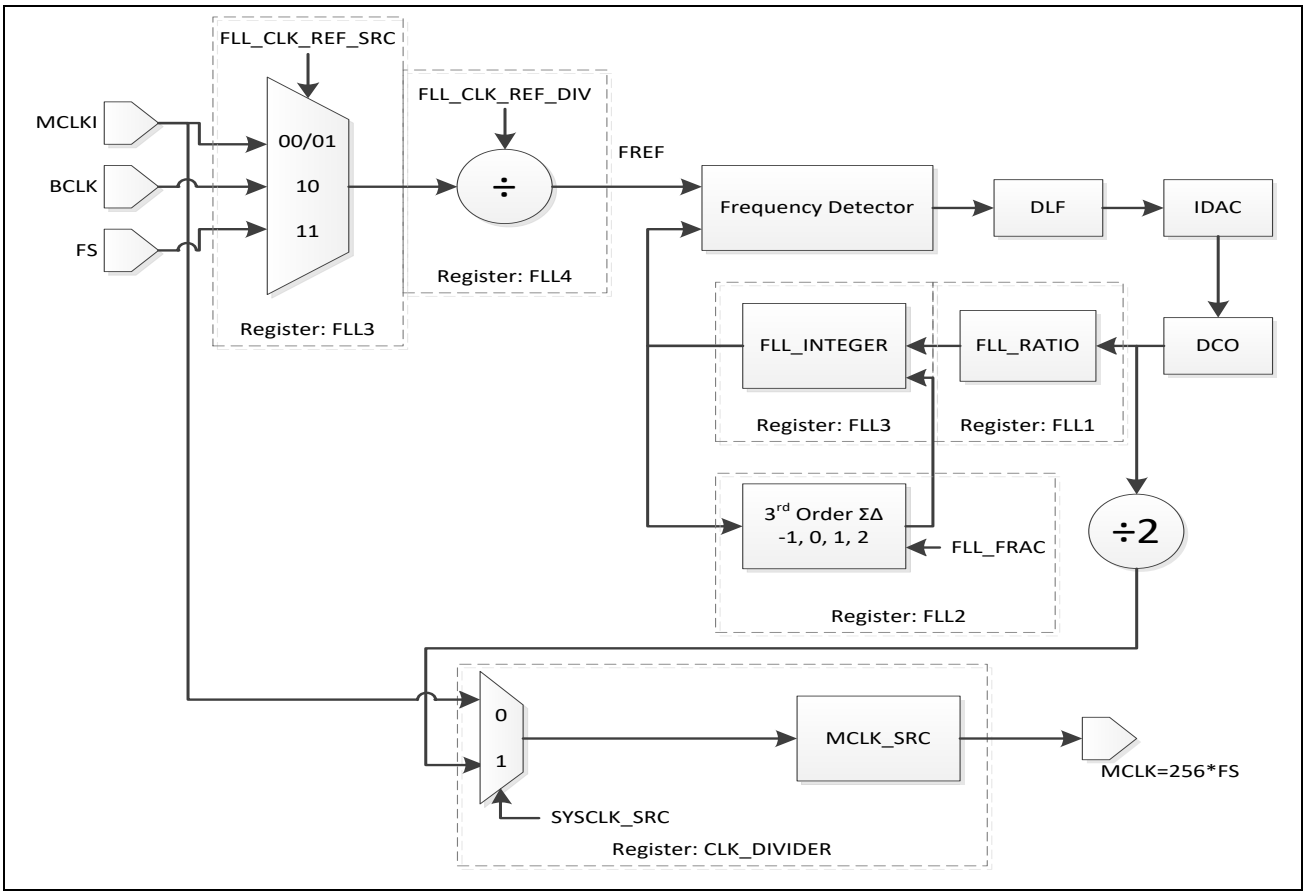


Figure 21 Frequency Locked Loop Block Diagram

The FLL output frequency is determined by the following parameters:

FLL1.FLL_RATIO REG0X04[6:0]

CLK_DIVIDER.MCLK_SRC REG0X03[3:0]

FLL3.FLL_INTEGER REG0X06[9:0]

FLL2.FLL_FRAC REG0X05[15:0]

FREF is the output of **FLL4.FLL_CLK_REF_DIV REG0X07[11:10]**

The following two output frequency equations are used to determine these settings:

1. FDCO = (FREF/**FLL_CLK_REF_DIVFLL_CLK_REF_DIV REG0X7[11:10]**)× **FLL_CLK_REF_DIVFLL_INTEGER REG0X06[9:0]**.**FLL2.FLL_FRAC REG0X05[15:0]**×**FLL1.FLL_RATIO REG0X4[6:0]**
2. MCLK = (FDCO × **CLK_DIVIDER.MCLK_SRC REG0X03[3:0]**) /2

Where FREF is the reference clock frequency for FLL, MCLK is the desired system frequency, and FDCO is the frequency of DCO in decimal format.

Example

If the reference frequency (FREF) is 12 MHz, the desired sampling rate (Fs) is 48 kHz, and SYSCLK = 256 Fs, what are the output frequency parameters?

Using these requirements, the following can be determined.

- MCLK = 256 × 48kHz = 12.288 MHz
- Using Equation 2:
  - FDCO = (2 × 12.288MHz) /**MCLK_SRCREG0X03[3:0]**
    - For FDCO to remain between 90 – 100 MHz, **MCLK_SRCREG0X03[3:0]** must be chosen to be 1/4. This and other values for **MCLK_SRCREG0X03[3:0]** can be seen in the register tables.
  - FDCO = (2 × 12.288 MHz) / (1/4) = 98.304 MHz
- Using Equation 1:
  - **FLL_INTEGEREG0X06[9:0]**.**FLL_FRAC REG0X05[15:0]** = FDCO / (FREF ×**FLL_RATIOREG0X04[6:0]**)
    - **FLL_RATIOREG0X04[6:0]**= 1 because FREF ≥ 512 kHz. This and other values for **FLL_RATIOREG0X04[6:0]** can be seen in the register tables.
  - **FLL_INTEGE**. **FLL_FRAC REG0X06[15:0]** = 98.304 MHz / (12 MHz × 1) = 8.192
    - **FLL_INTEGEREG0X06[9:0]**.**FLL_FRAC REG0X05[15:0]** represents an integer + decimal number.
  - **FLL_INTEGEREG0X06[9:0]** = 8
  - **FLL_FRACREG0X05[15:0]** = 0.192
- Now retrieve or convert the parameter values into their corresponding HEX values
  - **FLL_RATIOREG0X04[6:0]** = 7'h1 (this value is taken from the register chart in FREF≥ 512 kHz condition.)
  - **MCLK_SRCREG0X03[3:0]**= 4'h3 (this value is taken from the register chart for **MCLK_SRCREG0X03[3:0]** = 1/4)
  - **FLL_INTEGEREG0X06[9:0]** = 8 = 10'h8
  - **FLL_FRACREG0X05[15:0]** = 0.192 × 2^16 = 12583=16'h3126

9.4.1 FLL Application Notes

FLL4.FLL_CLK_REF_DIV REG0X07[11:10] can be used to reduce the reference frequency for SYSMCLK by dividing the input by 1, 2, 4, or 8. Use this to ensure the reference clock frequency is less than or equal to 13.5 MHz.

FLL3.GAIN_ERR_REG0X06[14:12] and **FLL5.FLL_CLK_REF_DIV_4CHK_REG0X07[14:12]** are used to control the gain and resolution, respectively. It is recommended that the default settings are used for these parameters.

FDCO must be within the 90 – 100 MHz or the FFL cannot be guaranteed across the full range of operation.

FLL2.FLL_FRAC REG0X05[15:0] must be set to '0' for Low Power Mode.

FLL6.SDM_EN REG0X09[14] to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption.

Set **FLL6.CHB_FILTER_EN REG0X08[14]** = '1' to enable FLL Loop Filter. Select filter clock source by **FLL6.CHB_FILTER_EN REG0X08[13]**. Select DCO input by **FLL6.FILTER_SW REG0X08[12]**. **FLL6.CUTOFF500 REG0X09[13]** & **FLL6.CUTOFF600 REG0X09[12]** can be used to define FLL cuttoff frequency at 500KHz or 600KHz. 500KHz will provide the best FLL performance but consume more power.

set **FLL6.FLL_FLTR_DITHER_SEL REG0X09[7:6]** = '01' or '10' or '11' **as 1LSB / 2LSB / 3LSB random bits** to Randomize the number of Filter Output Bits to average out output noise. If '00', there is no dither.

set **FLL6.FLL_FLTR_DITHER_SEL REG0X09[5:4]** = '00' or '01' or '10' or '11' **as no dither / 1LSB / 2LSB / 3LSB random bits** to Randomize the number of SD Modulator Input Bits.

10 Control Interfaces

The NAU88L25B includes a Serial Control Bus that provides access to all of the device control registers and may be configured as a 2-wire interface conforming to industry standard implementations of the I2C serial bus. See **Chapter 10.1** for detailed information on the 2-wire I2C Control Interface. When the 42-ball WLCSP package of the NAU88L25B is used, an SPI 4-Wire Control Interface Mode is also available. Refer to **Chapter 10.2** for details.

10.1 Two-Wire-Serial I2C Control Interface

The 2-wire bus has a bi-directional serial bus protocol. This protocol defines any device that sends data onto the bus as a Transmitter (Master), and the receiving device as the Receiver (Slave). The NAU88L25B can function only as a slave device when used in 2-Wire Interface Mode.

10.1.1 Two-Wire I2C Protocol Conventions

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device into Standby Mode. Acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the receipt of the eight bits of data.

Following a START condition, the Master must output a Device Address Byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W = '1', this indicates the Master is initiating a Read operation from the Slave device, and when R/W = '0', the Master is initiating a Write operation to the Slave device. If the Device Address matches the address of the Slave device, the Slave will output an ACK during the period when the Master allows for the ACK signal. **Figure 22** illustrates the START, ACK, and STOP conditions.

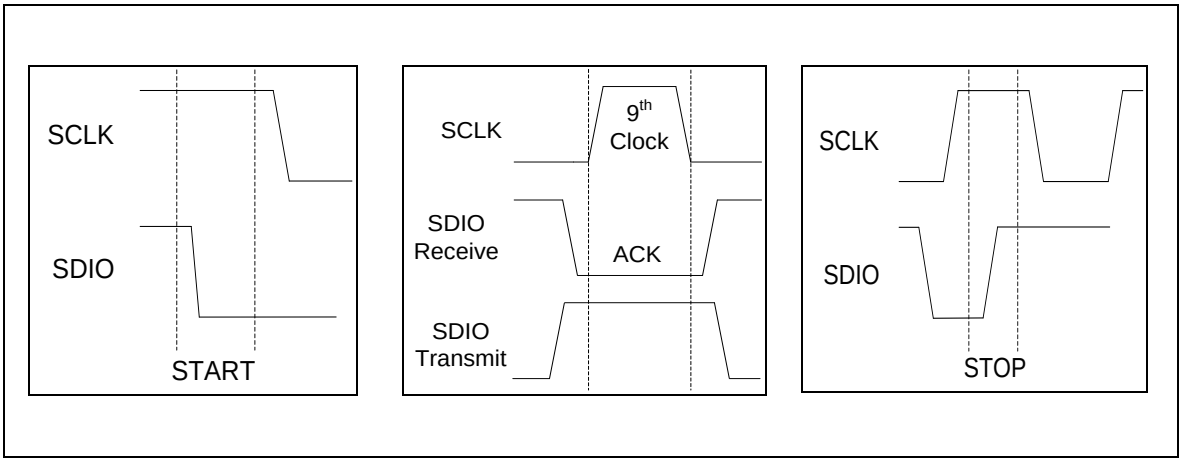


Figure 22 Two-Wire I2C START, ACK and STOP Conditions

Sometimes, the I2C Interface needs to use a Level Shifter between different supply domains, such as in **Figure 23**. In this case, during Acknowledge, the Receiver side (CODEC) will pull LOW, and the Transmit side (MCU) is disabled and is pulled HIGH by the pull high resistor. Because the NAU88L25B SDIO can sink 2 mA by default setting (maximum up to 8 mA,) as shown in **Figure 23**, R_{PU1} and R_{PU2} need to be selected such that the total current VDDB/R_{PU1}+ VDD_MCU/R_{PU2} during Acknowledge will not exceed the SDIO sinking capability.

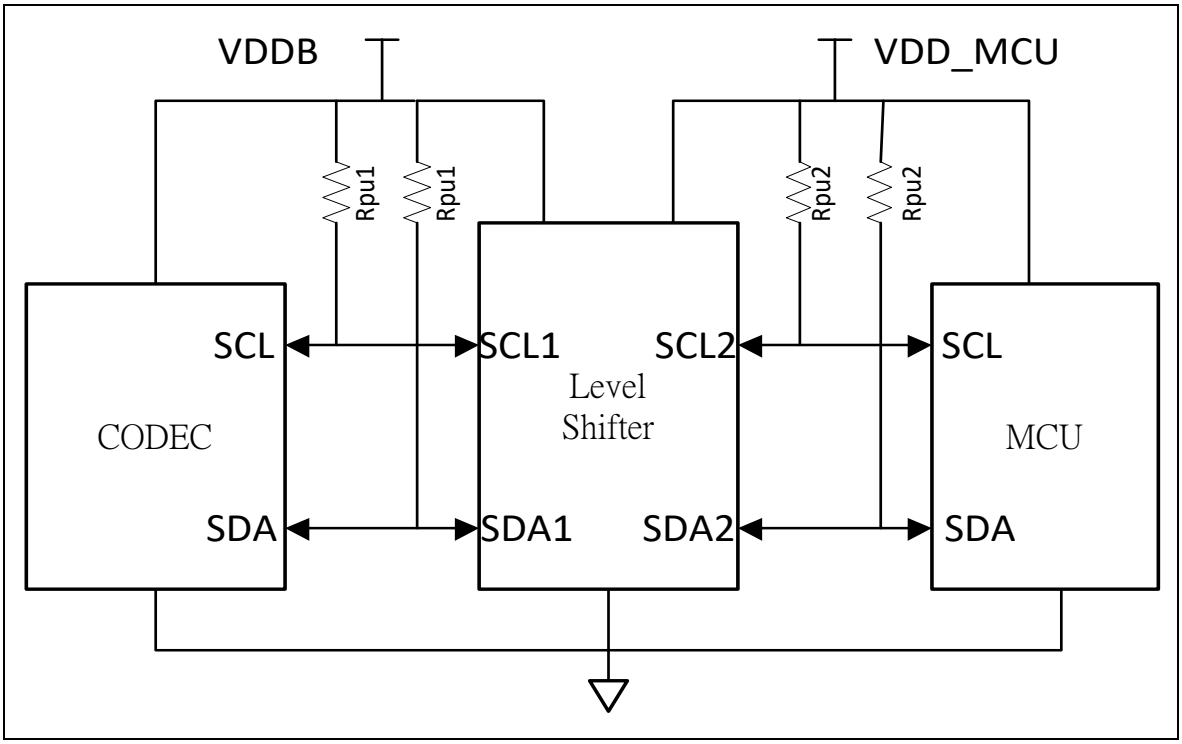


Figure 23 Typical I2C Level Shifter Circuit

10.1.2 Two-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid Device Address Byte with R/W='0', a valid Control Address Byte, Data Byte(S), and a STOP condition. See **Figure 24** for the Write format and refer to **Figure 25** for the Write sequence. The Device Address of the NAU88L25B is either 0x1A (CSB='0') or 0x1B (CSB='1'). In I2C Mode, the CSB pin will set the LSB of the Slave Address. If the Device Address matches this value, the NAU88L25B will respond with the expected ACK signal as it accepts the data being transmitted to it.

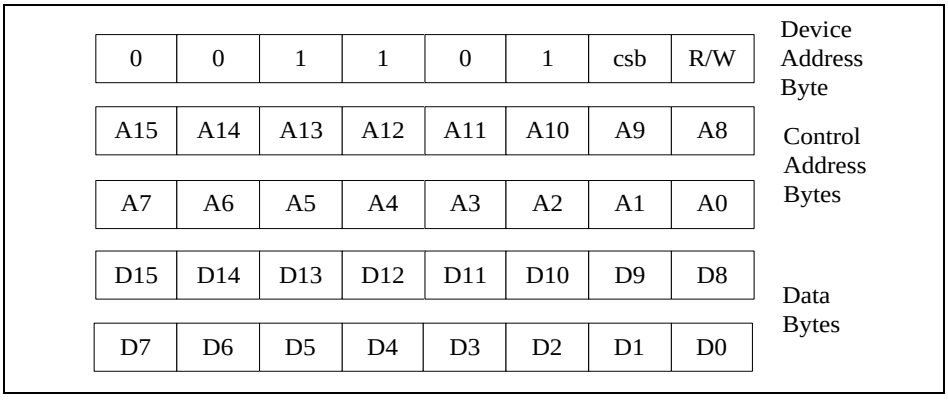


Figure 24 Two-Wire I2C Write Byte Format

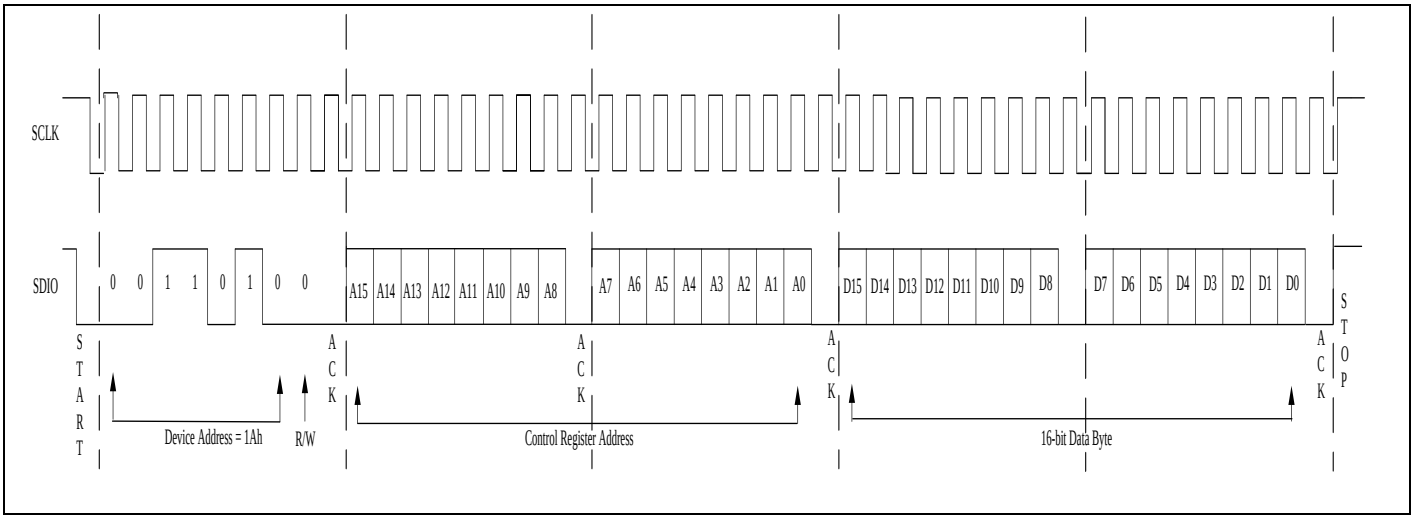


Figure 25 Two-Wire I2C Write Sequence

10.1.3 Two-Wire Write Application Note

The suggested flow to change the I2C address is as follows: After the PORB, the GPIO1 is under Input Mode, tie the GPIO pin to '1' or '0', then set **I2C_ADDR_SET.I2C_ADDR_SEL REG0X2[0]** = '0' to read the correct I2C address (depending on the tie 1 or 0). Apply **I2C_ADDR_SET.I2C_ADDR_SEL REG0X2[0]** = '1' to latch the GPIO pin status and use it for the future I2C address. When reading back REG0x02, bit 1 is the saved I2C LSB, bit 0 is the **I2C_ADDR_SEL**.

10.1.4 Two-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The Bus Master initiates the operation issuing the following sequence: a START condition, Device Address Byte with the R/W bit set to '0', and a Control Register Address byte. This indicates to the Slave device which of its control registers is to be accessed.

The 2-Wire Read Sequence is shown in **Figure 26.** If the device address matches this value, the NAU88L25B will respond with the expected ACK signal as it accepts the Control Register Address being transmitted into it. After this, the Master transmits a second START condition, and a second instantiation of the same Device Address, but now with R/W='1'. After again recognizing its Device Address, the NAU88L25B transmits an ACK, followed by a two-byte value containing the 16 bits of data from the selected control register inside the NAU88L25B. During this phase, the Master generates the ACK signal with each byte transferred from the NAU88L25B. If there is no STOP signal from the Master, the NAU88L25B will internally auto-increment the target Control Register Address and then output the two Data Bytes for this next register in the sequence.

This process will continue as long as the Master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU88L25B reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the Master terminates the read operation by issuing a STOP condition

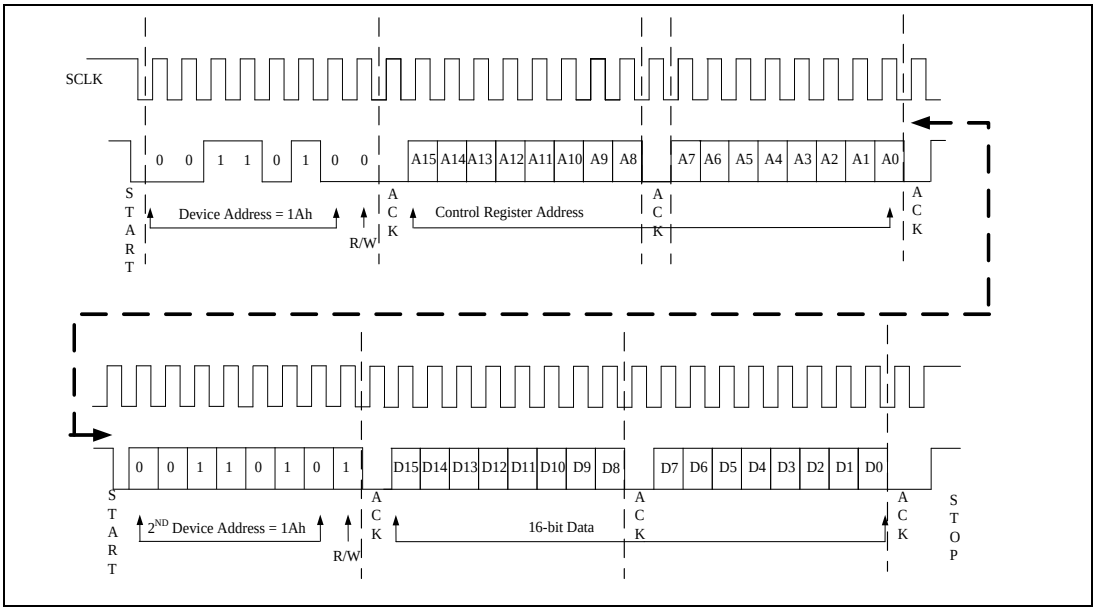


Figure 26 Two-Wire I2C Read Sequence

10.1.5 Two-Wire I2C Control Mode Timing

Two-Wire I2C Control Mode timing is shown in **Figure 27**.

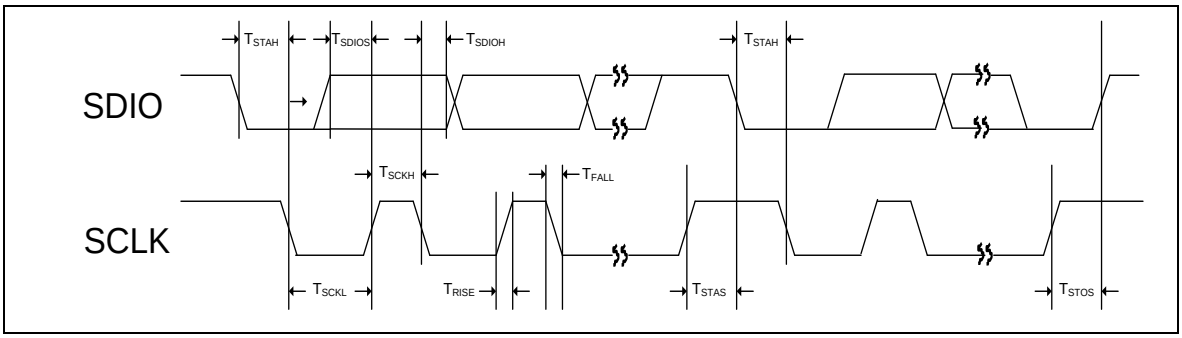


Figure 27 Two-Wire I2C Control Mode Timing

The I2C Timing parameters are shown in **Table 25.**

Table 25 I2C Timing Parameters

Description	Symbol	Min	Typ	Max	Unit
SDIO Falling Edge to SCLK falling edge hold timing in START / Repeat START condition.	T_{STAH}	600	-	-	ns
SCLK Rising Edge to SDIO falling edge setup timing in Repeat START condition.	T_{STAS}	600	-	-	ns
SCLK Rising Edge to SDIO rising edge setup timing in STOP condition.	T_{STOS}	600	-	-	ns
SCLK High Pulse Width	T_{SCKH}	600	-	-	ns
SCLK Low Pulse Width	T_{SCKL}	1,300	-	-	ns

Description	Symbol	Min	Typ	Max	Unit
Rise Time for all 2-Wire Mode Signals	T_{RISE}	-	-	300	ns
Fall Time for all 2-Wire Mode Signals	T_{FALL}	-	-	300	ns
SDIO to SCLK Rising Edge DATA Setup Time	T_{SDIOS}	100	-	-	ns
SCLK Falling Edge to SDIO DATA Hold Time	T_{SDIOH}	0	-	600	ns

10.2 Four-Wire SPI Control Interface

The 42-Ball WLCSP package of the NAU88L25B supports 4-Wire SPI Write and Read Control Interface Modes. For SPI Writes, only the CSB, SCLK, and SDIO pins are needed. During SPI Reads, an additional pin, GPIO4, is needed. The SPI 4-Wire Read/Write Modes are enabled when the NAU88L25B IFSEL pin is in a logical HIGH condition. In Read Mode, GPIO4 needs to be enabled by writing **GPIO4_OEREG0X19[7]**.

10.2.1 Four-Wire SPI Write Operation

The SPI 4-Wire Write operation is a full SPI data transaction. However, only three wires are needed, as this is a write-only operation with no return data. A fourth wire is needed only when there are bi-directional data. The CSB/GPIO1 pin on the NAU88L25B is used as the Chip Select function in an SPI transaction. Refer to **Figure 28**.

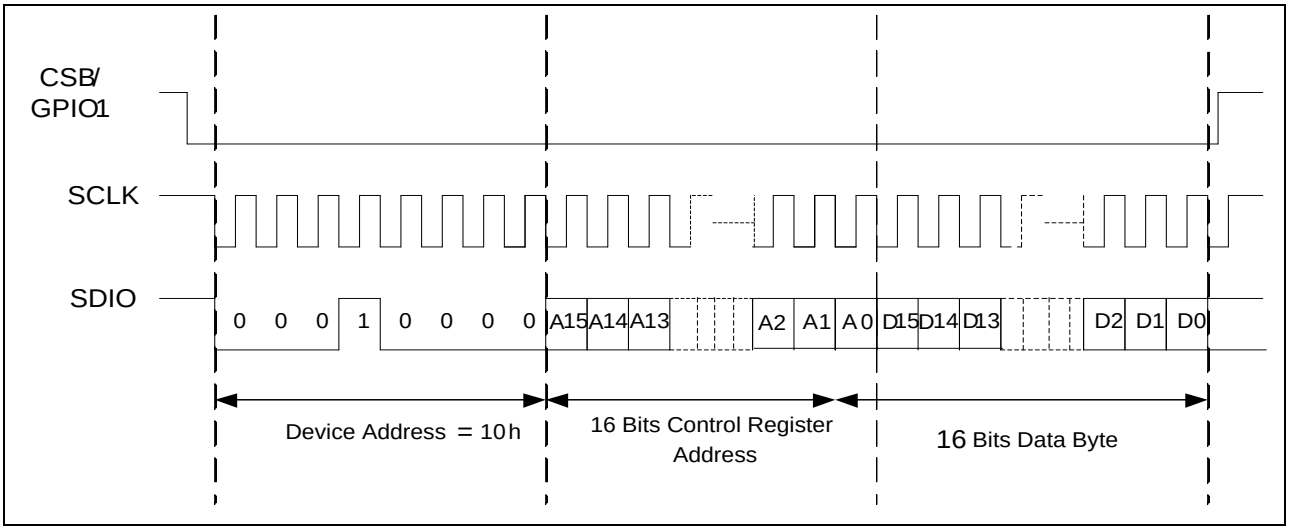


Figure 28 Four-Wire SPI Interface Write Operation

Note: The 4-wire SPI Interface is supported *only* when using the 42-Ball WLCSP package.

After CSB/GPIO1 is held in a logical LOW condition, data bits from SDIO are clocked into the NAU88L25B on every rising edge of SCLK. A Write operation is indicated by the value 0x10 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 16-bit Control Register Address and a 16-bit data value packed into the next two bytes of a four-byte sequence. After the Least Significant Bit (LSB) of the 16-bit data is clocked into the NAU88L25B, the 16-bit data value is automatically transferred to the NAU88L25B register addressed by the Control Register Address value.

If only a single register is to be written, CSB/GPIO1 must be put into a logical HIGH condition after the LSB of the Data Byte is clocked into the device. If CSB/GPIO1 remains in a logical LOW condition, the NAU88L25B will auto-index the Control Register Address value and the next two bytes will be

clocked into the next sequential NAU88L25B register address. This will continue as long as CSB/GPIO1 is in the logical LOW condition. If the Control Register Address being indexed inside the NAU88L25B reaches the value 0x82 (hexadecimal), then after the value for this register is written, the index will roll over to 0x01 and the process will continue.

10.2.2 Four-Wire SPI Read Operation

The Four-Wire SPI Read Operation is a full SPI data transaction with a two-byte address phase and a two-byte data phase. The CSB/GPIO1 pin on the NAU88L25B is used as the Chip Select function in the SPI transaction. Refer to **Figure 29**.

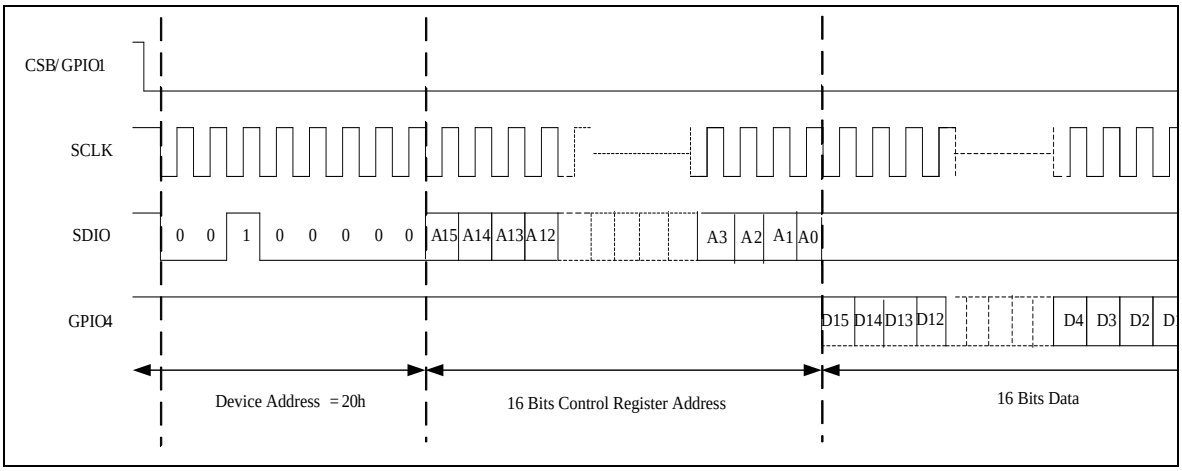


Figure 29 Four-Wire SPI Interface Read Operation

Note: The four-wire SPI Interface is supported *only* when using the 42-Ball WLCSP package.

After CSB/GPIO1 is held in a logical LOW condition, a Read operation is indicated by the value 0x20 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 16-bit Control Register Address.

After the LSB of the Control Register Address is clocked, the NAU88L25B will begin outputting its 16-bit data on the GPIO4 pin, beginning with the very next SCLK rising edge provided by the Master. This data is transmitted in two bytes, which are transmitted Most Significant Bit (MSB) first.

If only a single register is to be read, CSB/GPIO1 must be put into a logical HIGH condition after the LSB of the 16-bit data is clocked from the NAU88L25B. If CSB/GPIO1 remains in a logical LOW condition, the NAU88L25B will auto-index the Control Register Address value and the next two bytes will be clocked from the next sequential NAU88L25B register address. This will continue as long as CSB/GPIO1 is in the logical LOW condition. If the Control Register Address being indexed inside the NAU88L25B reaches the value 0x82 (hexadecimal), then after the value for this register is output, the index will roll over to 0x01 and the process will continue.

10.3 Software Reset

All the control registers of the NAU88L25B can be reset to their initial default conditions by writing any value to REG0X00 *twice* -- in any control interface mode. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their Power-On default values.

11 Digital Audio Interfaces

The NAU88L25B can be configured as either the Master or the Slave, by setting register **I2S_PCM_CTRL2.MS0 REG0X1D[3]** to '1' for Master Mode and to'0'; for Slave Mode. Slave Mode is the default if this bit is not written. In Master Mode, NAU88L25B outputs both Frame Sync (FS) and the audio data Bit Clock (BCLK) and has full control of the data transfer. In Slave Mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs. When FLL is set to Free Running Mode, the NAU88L25B must be set as a Master. When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the Time Slot function is enabled, there are additional output state options, including controlled tri-state capability.

11.1 Digital Audio Modes

The NAU88L25B Audio CODEC supports six digital audio modes: Right Justified, Left Justified, I2S, PCM A, PCM B, and PCM Time Slot. Select the desired Digital Audio Interface Mode using the **I2S_PCM_CTRL1.AIFMT0 REG0X1C[1:0]** register, the **I2S_PCM_CTRL1.LRP0 REG0X1C[6]** register, and the **I2S_PCM_CTRL2.PCM_TS_EN0 REG0X1D[10]** register, as shown in **Table 26 .**

Table 26 Digital Audio Interface Mode Settings

Mode	I2S_PCM_CTRL1.AIFMT0 REG0X1C[1:0]	I2S_PCM_CTRL1.LRP0 REG0X1C[6]	I2S_PCM_CTRL2.PCM_TS_EN0 REG0X1D[10]
Right Justified	00	0	0
Left Justified	01	0	0
I2S	10	0	0
PCM A	11	0	0
PCM B	11	1	0
PCM Time Slot	11	Don't Care	1

11.1.1 Right-Justified Audio Mode

In Right-Justified Mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, Channel 0 data is transmitted; when FS is LOW, Channel 1 data is transmitted. This can be seen in **Figure 30**.

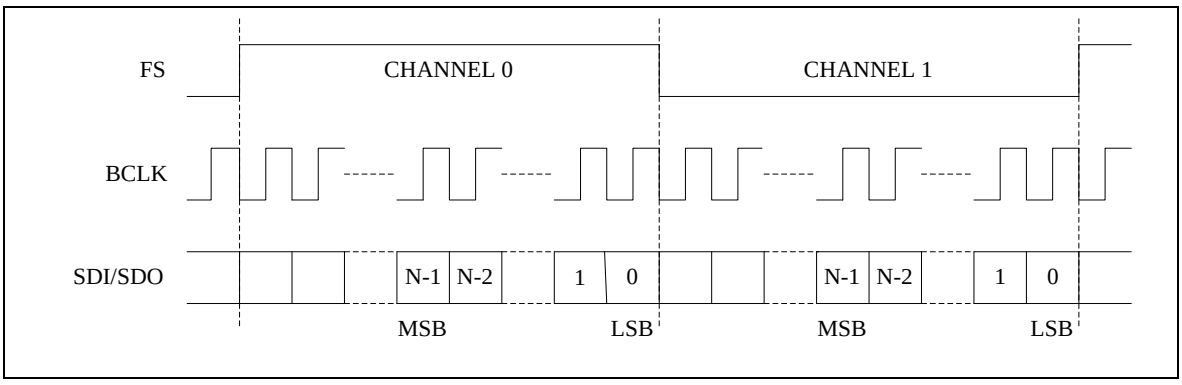


Figure 30 Right-Justified Audio Mode

11.1.2 Left-Justified Audio Mode

In Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, Channel 0 data is transmitted; when FS is LOW, Channel 1 data is transmitted, Refer to **Figure 31.**

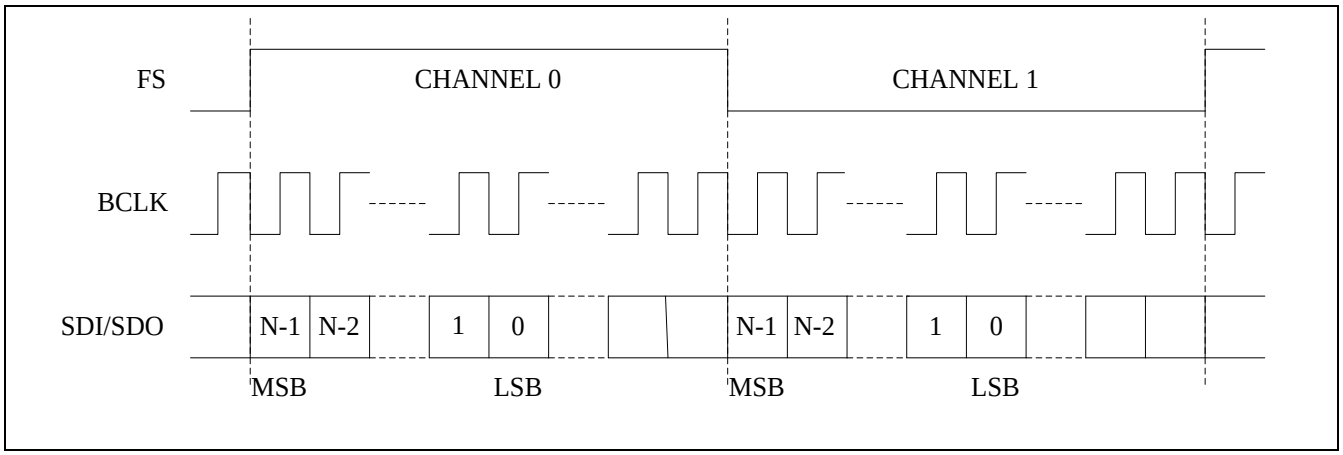


Figure 31 Left-Justified Audio Mode

11.1.3 I2S Audio Mode

In I2S Mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted: when FS is HIGH, right channel data is transmitted. Refer to **Figure 32.**

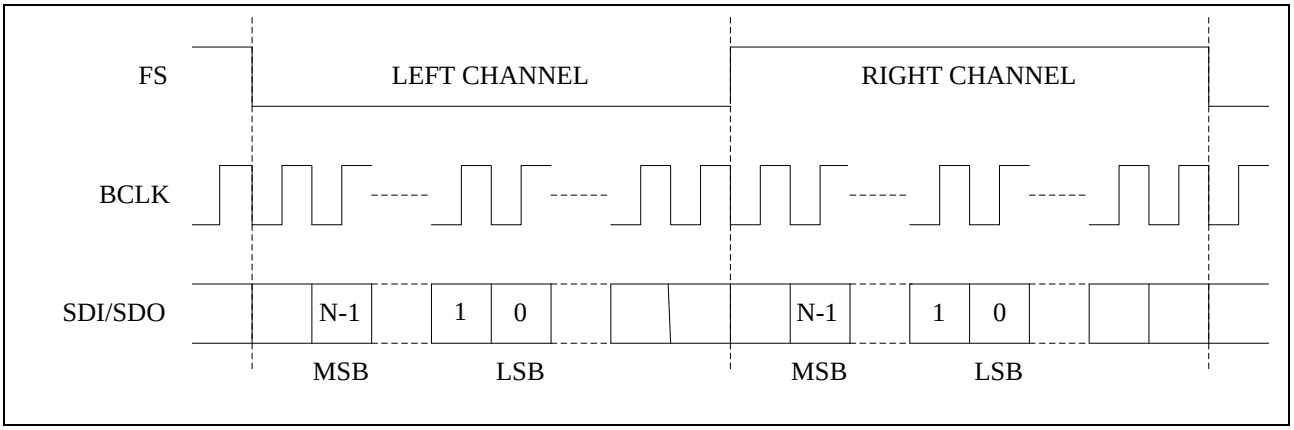


Figure 32 I2S Audio Mode

11.1.4 PCM A Audio Mode

In PCM A Mode, Channel 0 data is transmitted first, followed immediately by Channel 1 data. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next BCLK after the left channel LSB. This is shown in **Figure 33**.

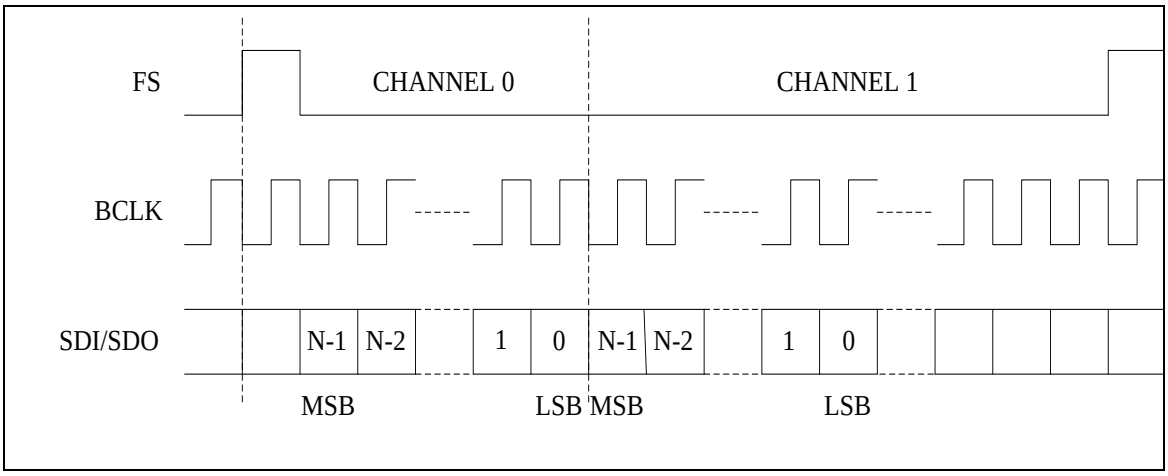


Figure 33 PCM A Audio Mode

11.1.5 PCM B Audio Mode

In PCM B Mode,Channel 0 data is transmitted first, followed immediately by Channel 1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, Channel 1 MSB is clocked on the next BCLK after the Channel 0 LSB. This can be seen in **Figure 34**.

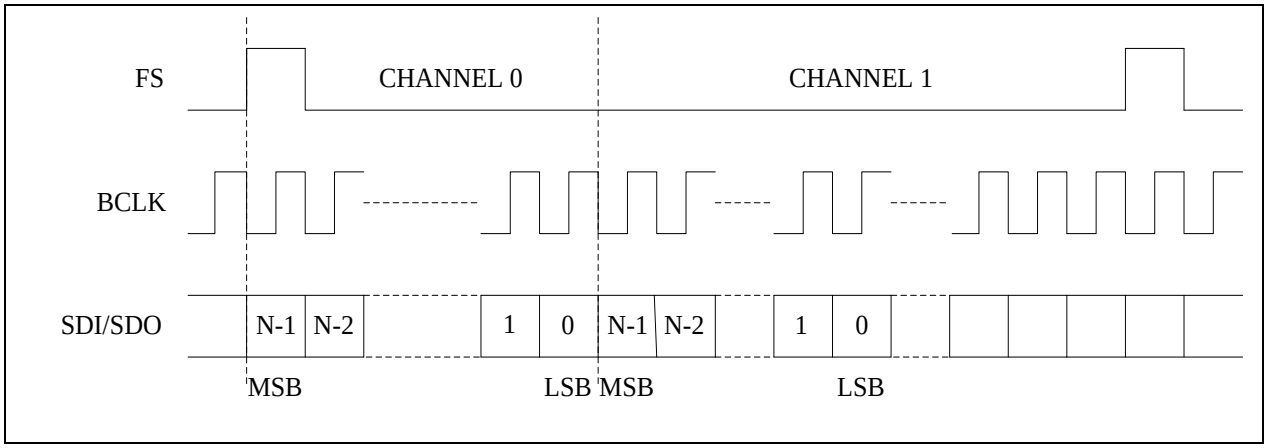


Figure 34 PCM-B Audio Mode

11.1.6 PCM Time Slot Audio Mode

PCM Time Slot Mode is used to delay the time at which the DAC and/or ADC data are clocked. This delay can be useful when multiple NAU88L25B chips or other devices share the same audio bus. This allows the audio of each chip to be delayed around each other without interference. This mode can be used to swap Channel 0 and Channel 1 audio or enable both channels to use the same data.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode; the audio data can be delayed by using the register **LEFT_TIME_SLOT.TSLOT_L0 REG0X1E[9:0]** for the left channel and using the register **RIGHT_TIME_SLOT.TSLOT_R0 REG0X1F[9:0]** for the right channel. The register **I2S_PCM_CTRL2.PCM_TS_EN0 REG0X1D[10]** needs to be set to 1. These delays can be seen in **Figure 35** in front of the MSB.

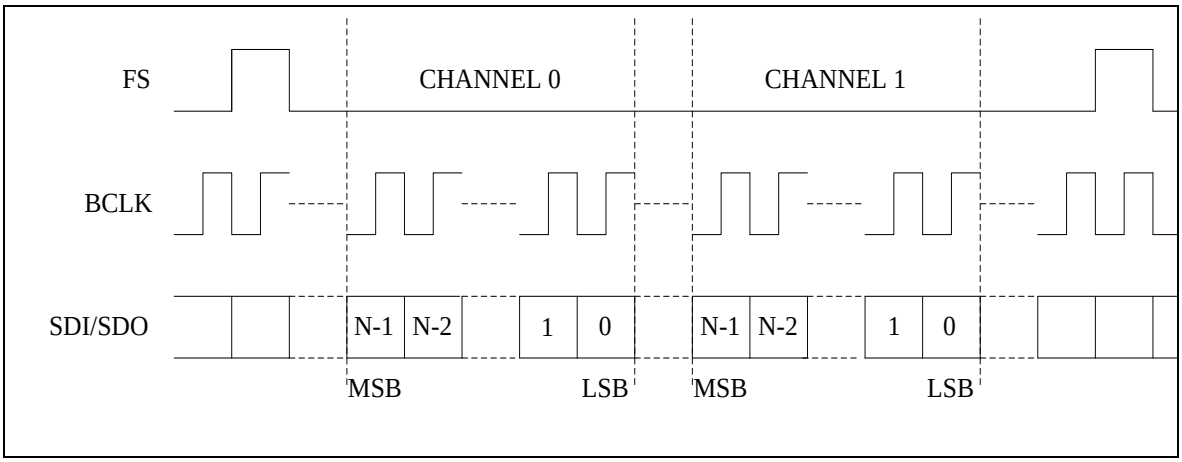


Figure 35 PCM Time Slot Audio Mode

11.1.7 PCM Time Slot Audio Application Notes

When using the NAU88L25B with other driver chips, the SDO pin can be set to pull up or pull down by enabling the register **I2S_PCM_CTRL2.ADCDAT0_PE REG0X1D[6]** and selecting up or down with the register **I2S_PCM_CTRL2.ADCDAT0_PS REG0X1D[5]**. This allows for wired-OR type bus sharing. If both are set to '0', SDO is high impedance, except when transmitting channel audio data. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

By default, **I2S_PCM_CTRL2.ADCDAT_OE REG0X1D[4]** actively drives the SDO pin (never in high impedance state). This must be disabled in order to share the data line.

11.2 Digital Audio Interface Timing Diagrams

11.2.1 Audio Interface Slave Mode

Figure 36 provides the timing for Audio Interface Slave Mode.

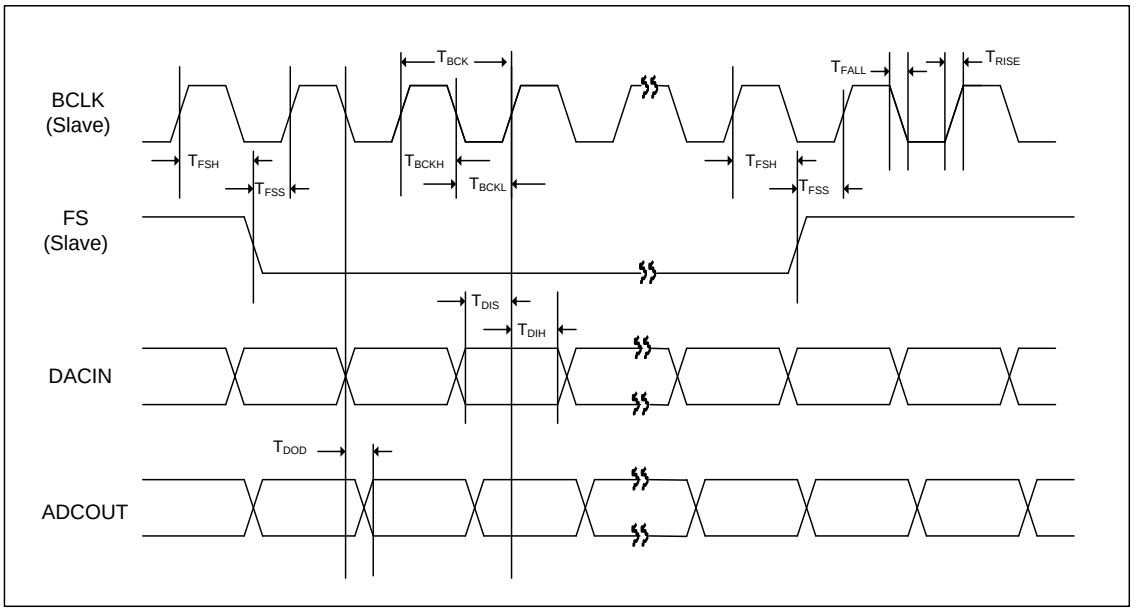


Figure 36 Audio Interface Slave Mode Timing

11.2.2 Audio Interface Master Mode

Figure 37 provides the timing diagram for the Audio Interface Master Mode.

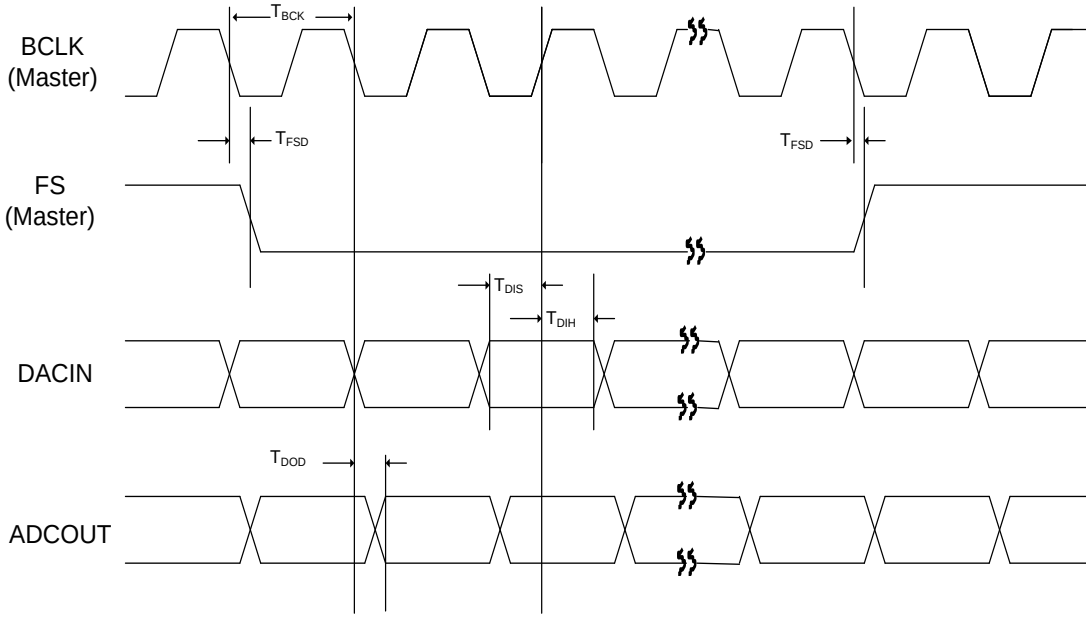


Figure 37 Audio Interface Master Mode Timing

11.2.3 PCM Audio Interface Slave Mode

I2S or PCM Audio Data can be processed using either Slave Mode or Master Mode. The timing diagram for PCM Audio Data in Slave Mode is shown in **Figure 38**.

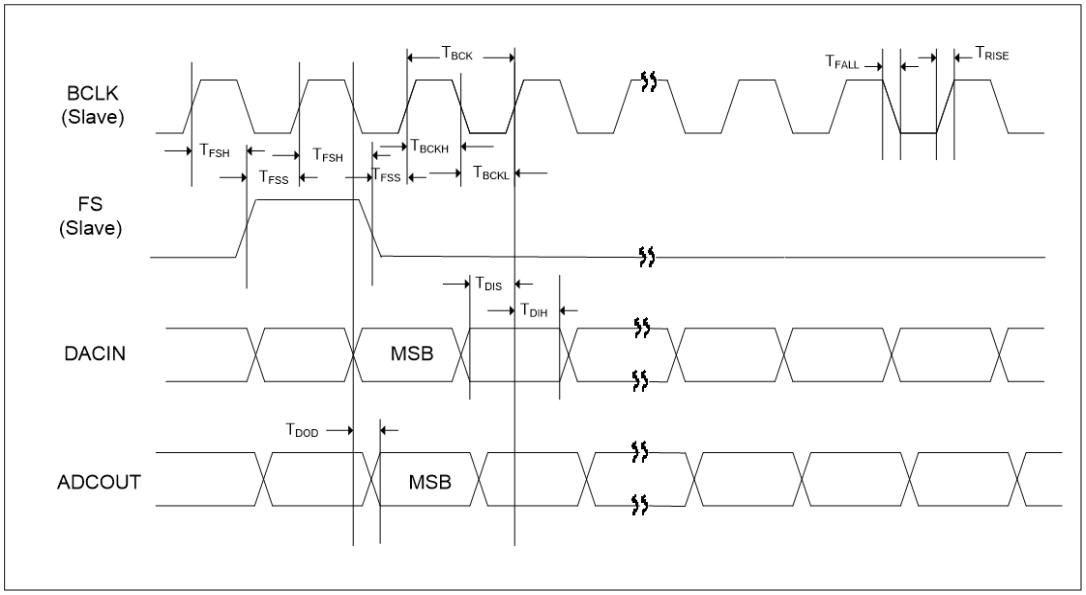


Figure 38 PCM Audio Interface Slave Mode Timing

11.2.4 PCM Audio Interface Master Mode

I2S or PCM Audio Data can be processed using either Master or Slave Mode. The timing diagram for PCM Audio Data in Master Mode is shown in **Figure 39.**

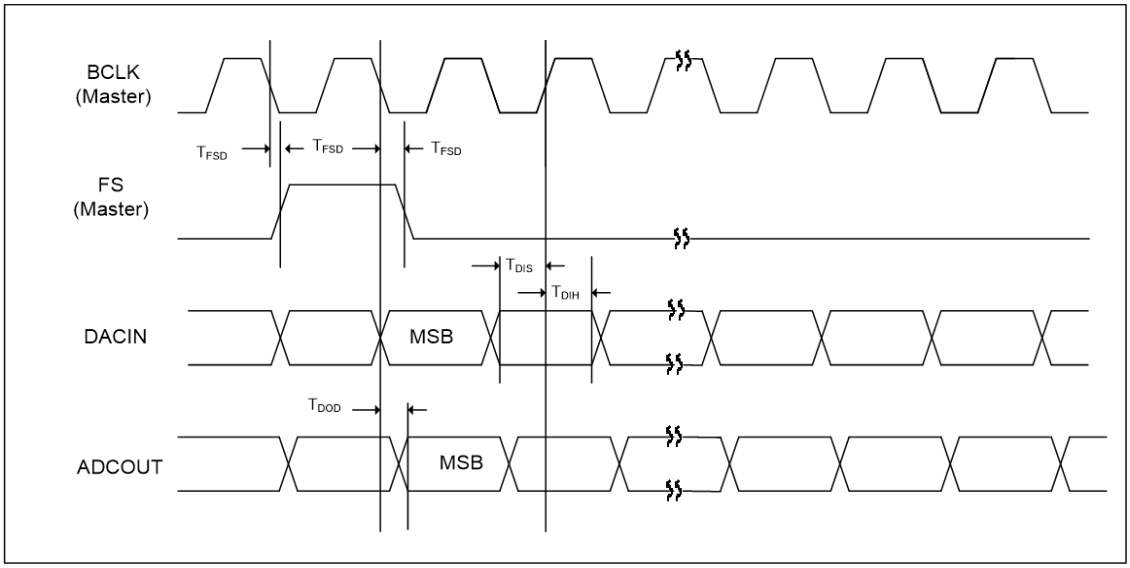


Figure 39 PCM Audio Interface Master Mode Timing

11.2.5 PCM Time Slot Audio Interface Slave Mode

PCM Time Slot Data can be processed using either Slave Mode or Master Mode. The timing diagram for PCM Time Slot Audio Data in Slave Mode is shown in **Figure 40.**

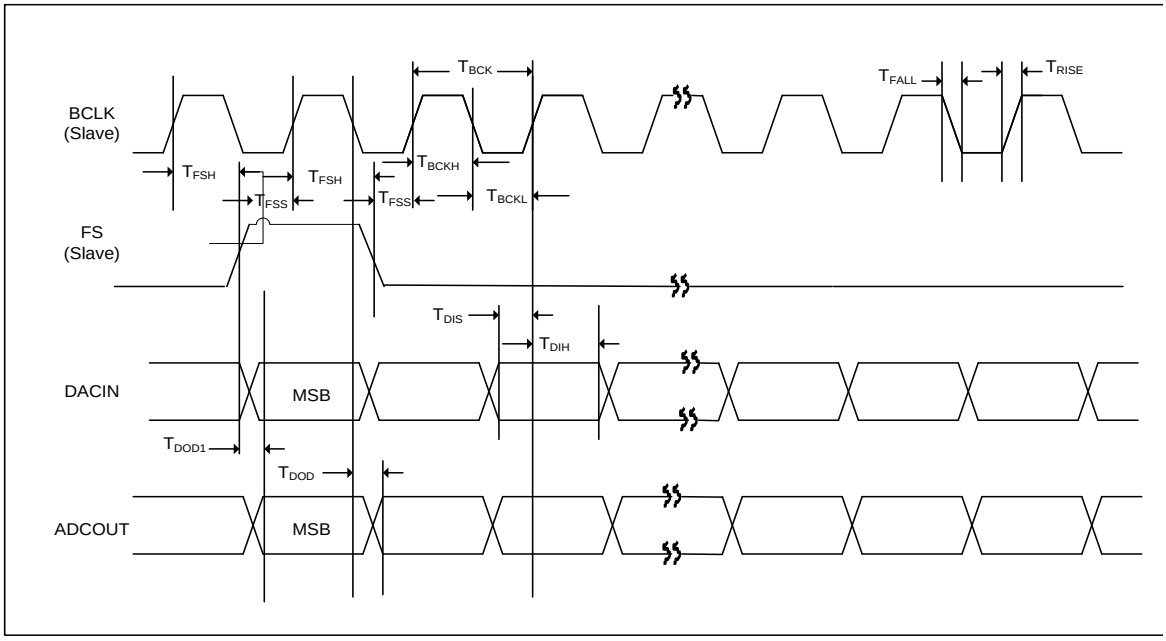


Figure 40 PCM Time Slot Audio Interface Slave Mode Timing

11.2.6 PCM Time Slot Audio Interface Master Mode Timing

The timing diagram for PCM Time Slot Audio Data in Master Mode is shown in **Figure 41**.

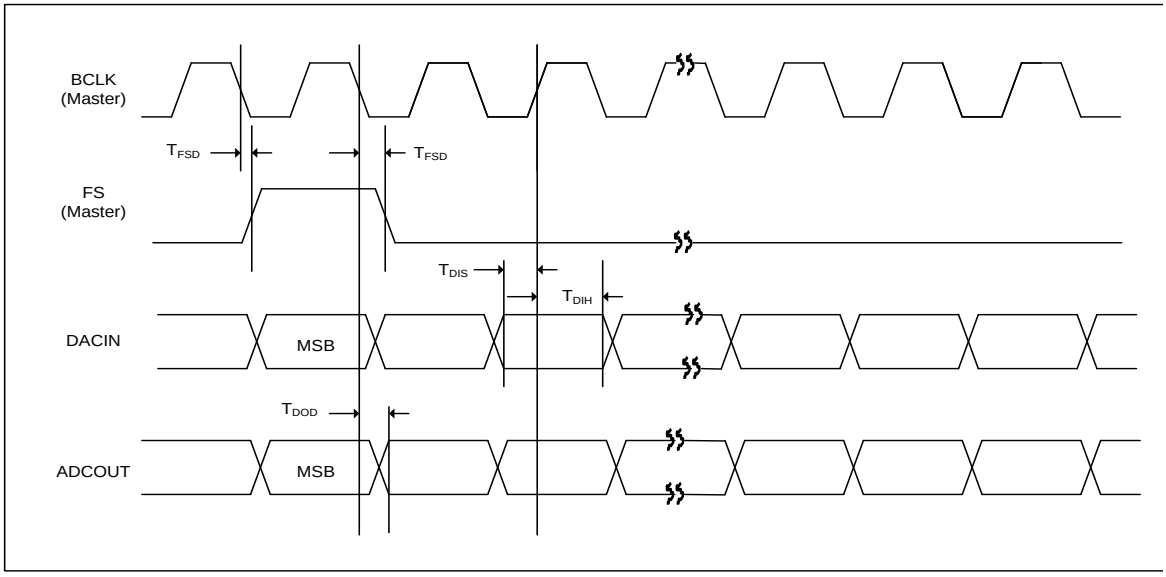


Figure 41 PCM Time Slot Audio Interface Master Mode Timing

11.2.7 Digital Audio Interface Timing Parameters Slave Mode

Table 27 Digital Audio Interface Timing Parameters*

Description	Symbol	Min	Typ	Max	Unit
BCLK Cycle Time	T_{BCK}	50	---	---	ns
BCLK High Pulse Width	T_{BCKH}	20	---	---	ns
BCLK Low Pulse Width	T_{BCKL}	20	---	---	ns
Fs to BCLK Rising Edge Setup Time	T_{FSS}	20	---	---	ns
BCLK Rising Edge to Fs Hold Time	T_{FSH}	20	---	---	ns
Rise Time for All Audio Interface Signals	T_{RISE}	---	---	$0.135T_{BCK}$	ns
Fall Time for All Audio Interface Signals	T_{FALL}	---	---	$0.135T_{BCK}$	ns
DACIN to BCLK Rising Edge Setup Time	T_{DIS}	15	---	---	ns
BCLK Rising Edge to DACIN Hold Time	T_{DIH}	15	---	---	ns
Delay Time from BCLK Falling Edge to ADCOUT	T_{DOD}	---	---	80**	ns

11.2.8 Digital Audio Interface Timing Parameters Master Mode

Table 28 Digital Audio Interface Timing Parameters*

Description	Symbol	Min	Typ	Max	Unit
BCLK Cycle Time	T_{BCK}	50	---	---	ns
Rise Time for All Audio Interface Signals	T_{RISE}	---	---	$0.135T_{BCK}$	ns
Fall Time for All Audio Interface Signals	T_{FALL}	---	---	$0.135T_{BCK}$	ns
BCLK Falling Edge to FS Delay Time in Master Mode	T_{FSD}	---	---	10	ns
DACIN to BCLK Rising Edge Setup Time	T_{DIS}	15	---	---	ns
BCLK Rising Edge to DACIN Hold Time	T_{DIH}	15	---	---	ns
Delay Time from BCLK Falling Edge to ADCOUT	T_{DOD}	---	---	80**	ns

Note:

* Timing measurement was measured by Keysight DSO-4104A 1GHz 5GSa/s with N2894A 700MHz Probe. (High impedence, low capacitance, and high bandwithd Active probe is an optional.)

**ADCOUT pin has no loading.

11.3 TDM Audio Data

Time Division Multiplexing of audio data can be handled by the NAU88L25B Audio CODEC in four modes: I2S Mode, PCM A Mode, PCM B, and PCM Offset Mode.

11.3.1 TDM I2S Audio Mode

In I2S Mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, Channel 0 is transmitted first; then Channel 2 data is transmitted; then when FS is HIGH, Channel 1 then Channel 3 channel data is transmitted. This is shown in **Figure 42**.

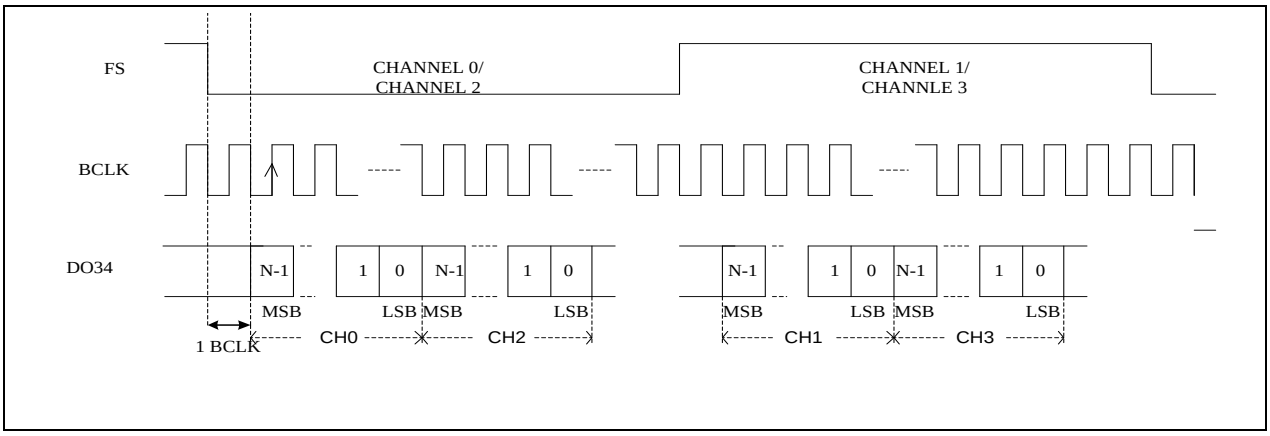


Figure 42 TDM I2S Audio Format

11.3.2 TDM PCM A Audio Mode

In PCM A Mode, Channel 0 data is transmitted first, followed sequentially by Channel 1, 2, and 3. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in **Figure 43**.

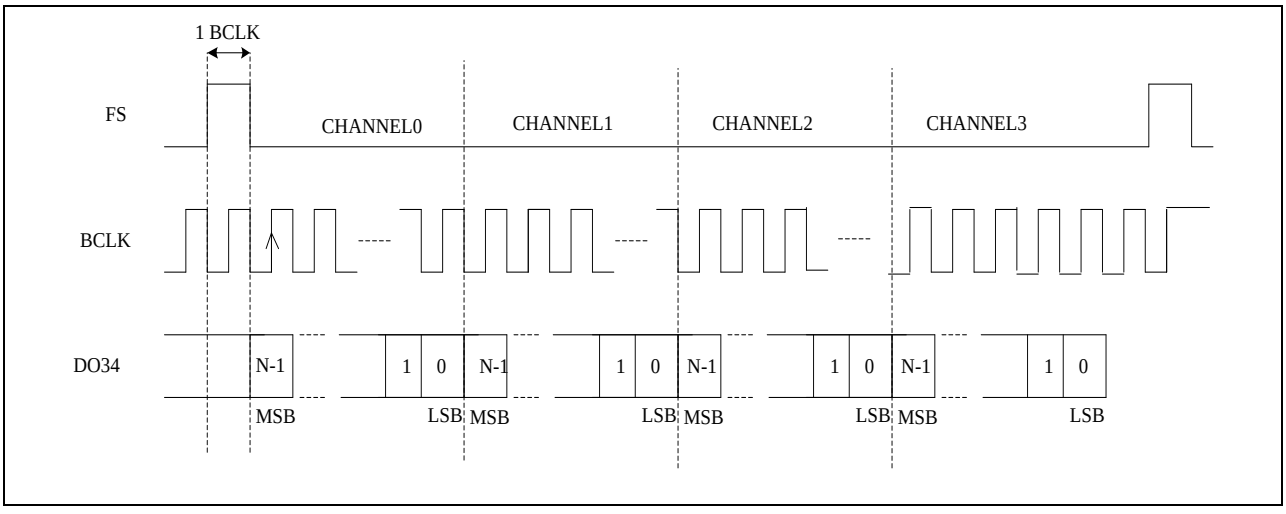


Figure 43 TDM PCM A Audio Format

11.3.3 TDM PCM B Audio Mode

In PCM B Mode, Channel 0 data is transmitted first, followed immediately by Channel 1 data. The Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge; Channel 1 MSB is clocked on the next SCLK after Channel 0 LSB. Refer to **Figure 44.**

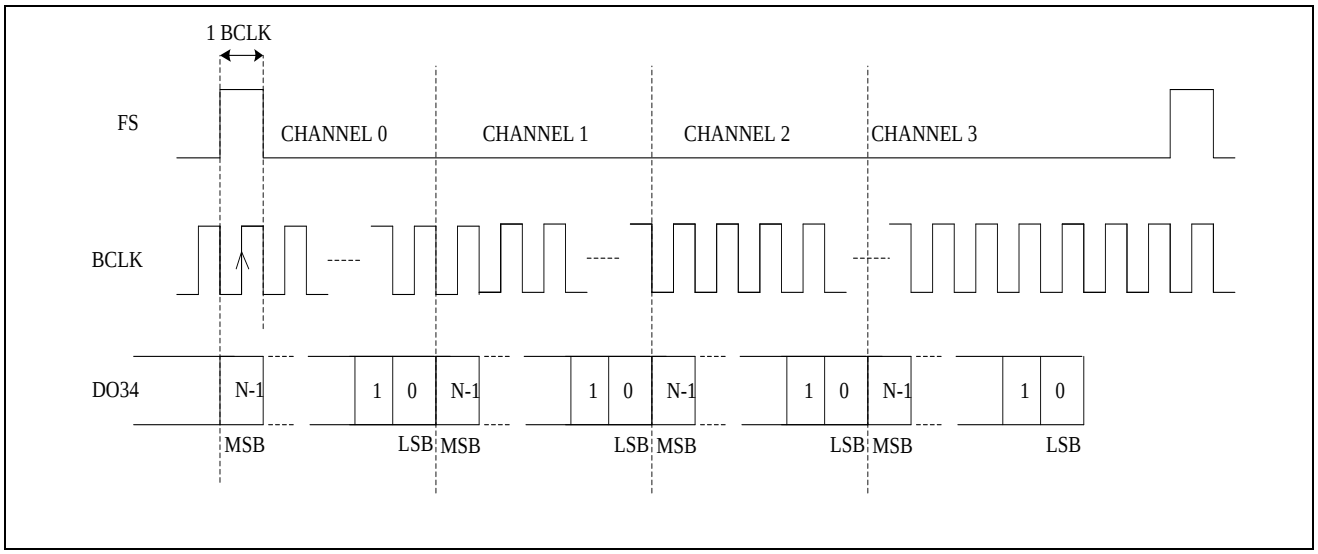


Figure 44 TDM PCM B Audio Format

11.3.4 TDM PCM Offset Audio Mode

PCM Offset Mode is used to delay the time at which DAC data is clocked. This increases the flexibility of the NAU88L25B for a wide range of system designs. One key application of this feature is to enable multiple NAU88L25B chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to allow multiple channels to use the same data. For this application to be used, the **TDM_CTRL.TDM REG0X1B[15]** and **TDM_CTRL.PCM_OFFSET_MODE_CTRL REG0X1B[14]** registers must be set to '1'.

Normally, DAC data are clocked immediately after the Frame Sync (FS). Howevr, in PCM Offset Mode, audio data is delayed by a delay-count specified in the device control registers. The Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in the **LEFT_TIME_SLOT.TSLOT_LREG0X1E[9:0]** register. The subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This can be seen in **Figure 45.**

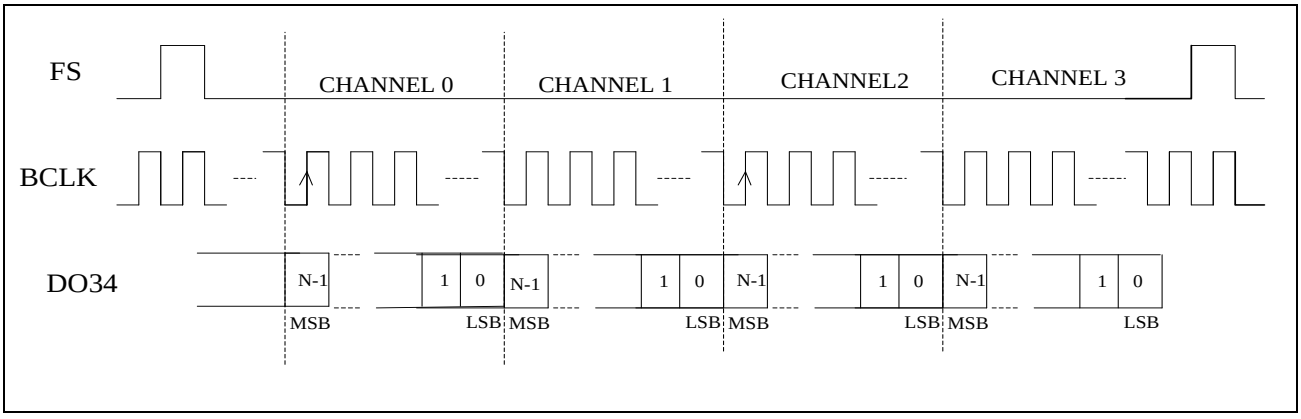


Figure 45 TDM PCM Offset Audio Format

12 Outputs

The NAU88L25B provides one stereophonic, Class G ground-reference headphone output. The Audio CODEC also provides the register (0x0C) setting to control the grounding on/off on the 4 jack terminals. Note that humming noise can be prevented by always providing power to the CODEC after system shutdown.

12.1 Class G Headphone Driver and Charge Pump

The NAU88L25B Audio CODEC uses a stereophonic, Class G speaker driver powered by a Charge Pump for the headphones. For typical operation with large and small signals, the Charge Pump provides ±1.8 V and ±0.9 V, respectively. These output drivers are driven by dedicated Left and Right DACs and can provide 3 mW of power to a 32 Ω load. The Output paths are shown in Figure 46.

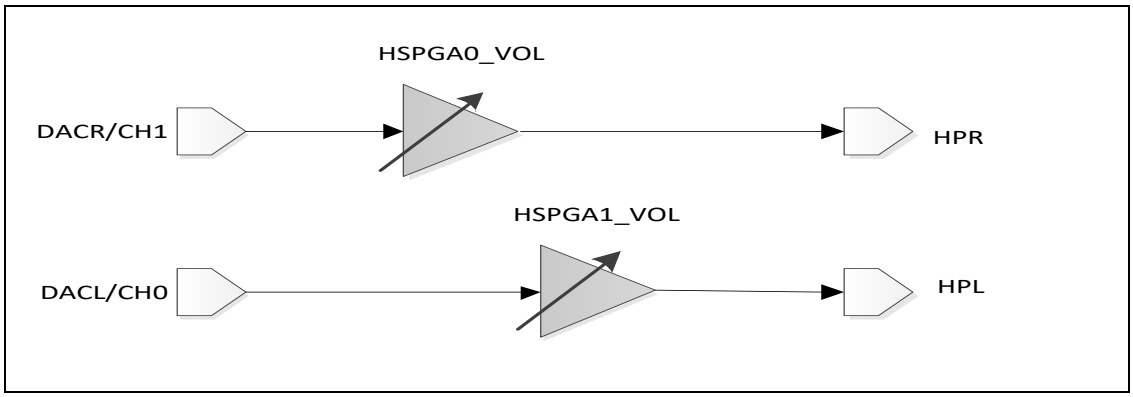


Figure 46 DAC to Headphone Output Paths

To enable the Class-G Driver and Charge Pump in the NAU88L25B CODEC, requires the use of two registers. The Class G Driver is enabled with the **CLASSG_CTRL.CLASSG_EN REG0X50[0]** register; while the Charge Pump is enabled with the register **CHARGE_PUMP_AND_POWER_DOWN_CONTRL.RINN REG0X80[5]**. Three capacitors are needed to generate the negative voltage from the positive 1.8 V. Typically, 2 µF ceramic capacitors are used: A Fly Back capacitor is connected between pins CPCA and CPCB; a Positive Output Decoupling capacitor is applied from pin CPVOUTP to ground (VSSCP); and a Negative Output Decoupling capacitor is applied from pin CPOUTN to ground (VSSCP).

CLASSG_CTRL.CLASSG_CMP_EN REG0X50[2:1] determines which DAC signals are to be monitored. All LOW is the default, which gives the low voltage output. This is used when the headphones have attenuated signals. **CLASSG_CTRL.CLASSG_THRSLD REG0X50[5:4]** sets the threshold from 1/16 to 1/4 Full Scale.

For the HIGH voltage charge up, two registers select the short circuit setting: the **CHARGE_PUMP_AND_POWER_ DOWN_CONTRL.SHCIRSEL1 REG0X80[0]** register and the **CHARGE_PUMP_AND_POWER_ DOWN_CONTRL.SHCIRSEL2 REG0X80[1]** register. When set at the default value, the protection mode is set for 1.7 V and VDD can provide up to 150 mA. When both are enabled, the protection mode is set to 1.4 V and VDD can supply 500 mA. **Table 29** provides the settings for the Charge Pump Short Circuit.

Table 29 Charge Pump Short Circuit Settings

SHCIRSEL2 REG0X80[1]	SHCIRSEL1REG0X80[0]	Short Circuit Select Voltage
0	0	1.7 volts
0	1	1.6 volts
1	0	1.5 volts
1	1	1.4 volts

Headphone volume control registers can be used to mute the headset channels, control the gain for each output and allow adjustment of the gain of each headset output. **HSVOL_CTRL.MUTE_HSPGA0 REG0X32[13]** provides mute control fot he Left headset output; and **HSVOL_CTRL.MUTE_HSPGA1 REG0X32[12],** provides mute control fot he Right headset output. The gain adjustment and control for the Left headset output is provided by **HSVOL_CTRL.HSPGA0_VOL REG0X32[11:6]** from 6b'000000=0dB to 6b'111111=-54dB; in increments of 1dB/step. **HSVOL_CTRL. HSPGA1_VOL REG0X32[5:0]** controls the gain and gain adjustment for the Right headset output.

CHARGE_PUMP_ INPUT_READ.REG0X81 is read only and shows the status of the charge pump's present running conditions. Refer to **Chapter 0** for detailed information on all registers.

12.1.1 Outputs Application Notes

To enable CPVDD = 0.9 V for small signals:

- Set **CLASSG_CTRL.CLASSG_CMP_EN REG0X50[1]** = 1'b0 (**CLASSG_CMP_EN** has two bits; only one channel needs to be enabled to do the comparison).
- Set **CLASSG_CTRL.CLASSG_EN REG0X50[0]** = 1'b0 to force ClassG Mode 0.

To enable CPVDD = 1.8 V for full scale signals:

- Set **CLASSG_CTRL.CLASSG_CMP_ENREG0X50[1]** = 1'b1.
- Set **CLASSG_CTRL.CLASSG_ENREG0X50[0]** = 1'b0 to force ClassG Mode 1.

12.2 Humming Noise and Prevention

As shown in **Figure 47** JKR2 and JKSLV are headset jack pins used to support various headset types. The function MIC or GND could be selected for JKR2 and JKSLV by setting the register Reg0xC[3:2]. As soon as the system powers down, JKR2 or JKSLV set to the GND function becomes floating. Headset JKR2 and JKSLV become floating concurrently.

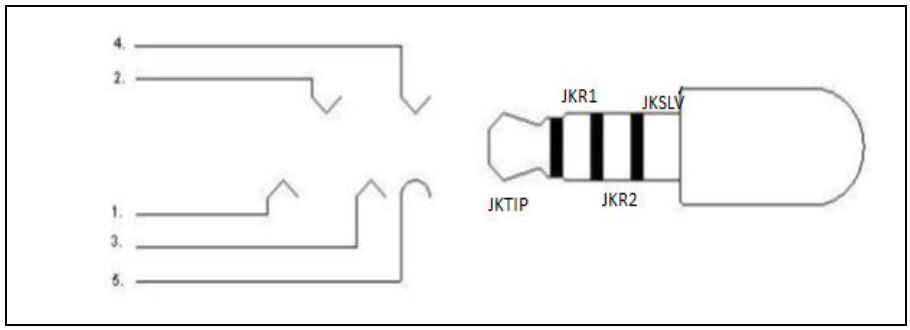


Figure 47 Jack Connector Pinouts

Note: 1. JKTIP (Headphone Left), 2. JKR1 (Headphone Right), 3. JKR2, 4 JKSLV.

When the GND pin of the headset jack becomes floating, and the device is hooked up to an AC-powered charger and the jack is hooked up to an AC-powered speaker, the ground loop may be amplified and may be heard as a humming noise from the loud speaker.

The NAU88L25B provides the register (0x0C) setting to control the grounding on/off on these 4 jack terminals, Jack Tip/Ring1/Ring2/Sleeve. Always providing power to the CODEC can prevent the humming noise after system shutdown. As long as MICBIAS is in sleep mode, the NAU88L25B can hold all 4 pins to ground such that it can avoid the humming noise without adding external components.

The NAU88L25B also has a Field Effect Transistor (FET) control circuit integrated into the IC as shown in **Figure 48.** In this case, only VDDMIC needs to be on to pull down JKR2 and JKSLV pins to ground. In the meanwhile, VDDA, VDDB, and VDDC do not require 1.8 V power sources. When VDDA/VDDB/VDDC=0V, VDDMIC is always on, the current consumption at VDDMIC is < 1uA.

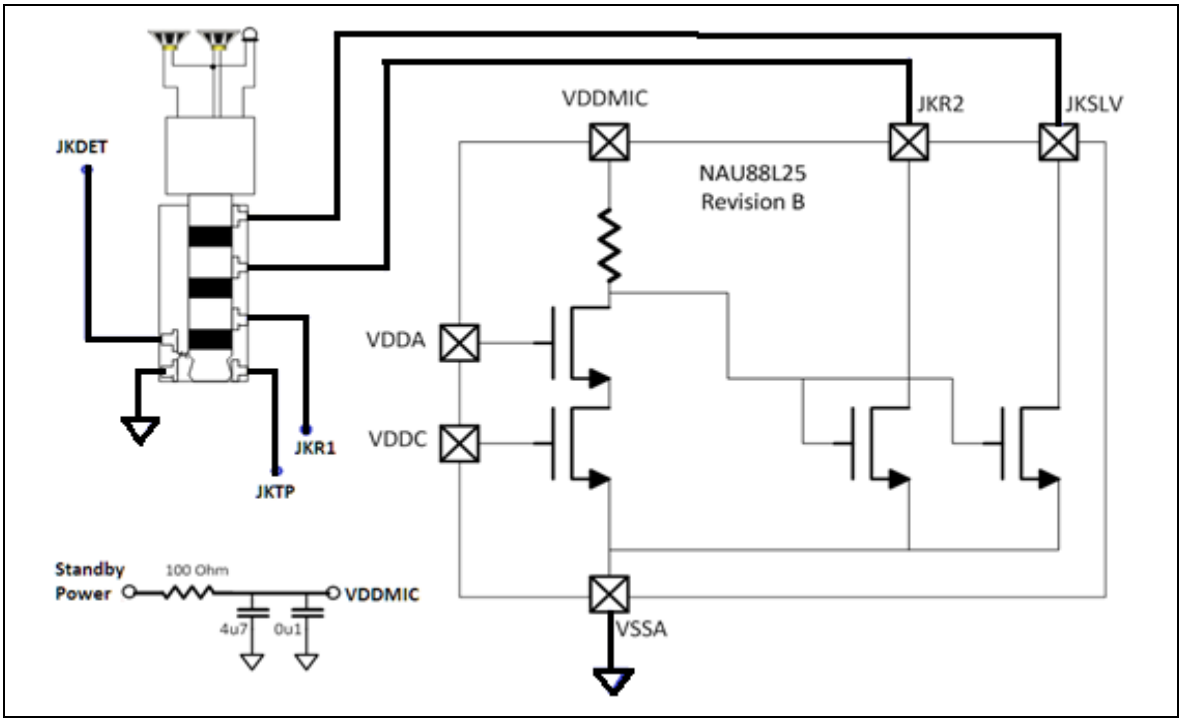


Figure 48 NAU88L25B Humming Noise Preventive Circuit

13 Headset Detection

As an Ultra-Low-Power High-Performance Audio CODEC Ground-Referenced Headphone Amplifier with Advanced Headset Detection, the NAU88L25B includes an extensive set of detection features to support various types of headsets for global compatibility. These features include Jack Dectection, Microphone Detection, Key Detection, and Jack Interrupt Sequences.

13.1 Jack Detection

Jack Detection recognizes when a headset is inserted into or ejected from an external headset jack. This is done by detecting a voltage at the JKDET pin, which then triggers sequences associated with headset support.

13.1.1 Jack Detection Application Notes

Figure 49 illustrates the use of the registers involved in Jack Insertion or Ejection Detection.

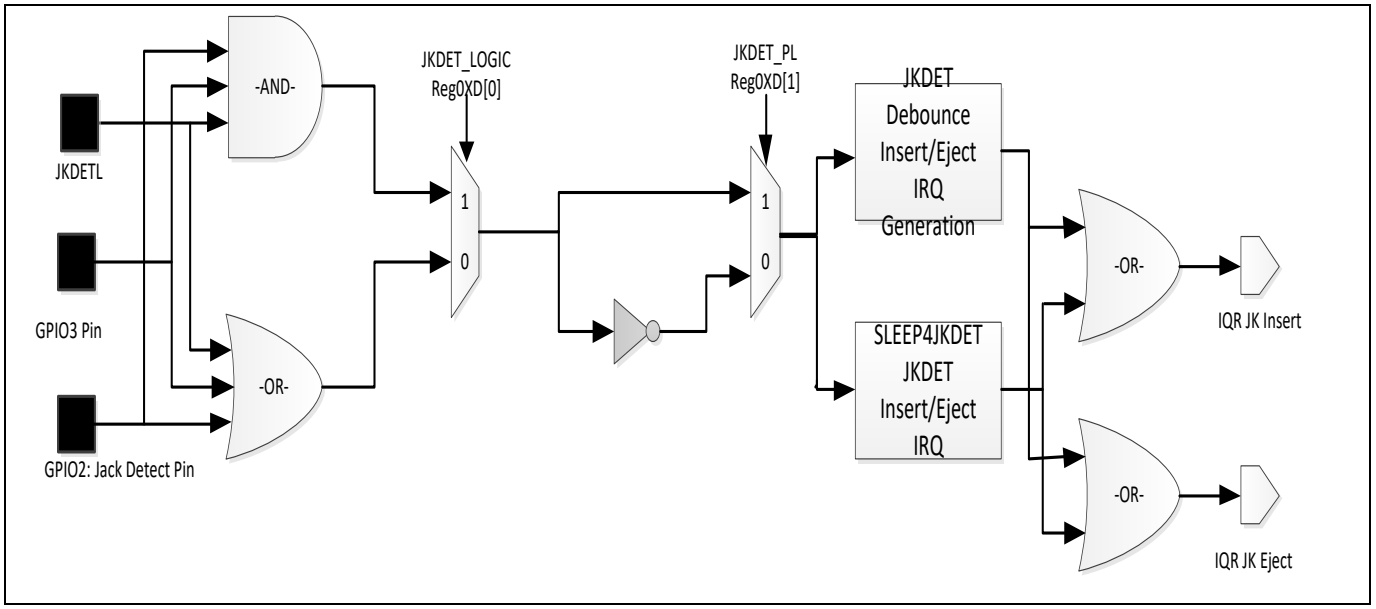


Figure 49 Jack Detection

These registers are used in Jack Detection:

JACK_DET_CTRL.JKDET_PL REG0X0D[1] sets the Jack Insertion status polarity.

JACK_DET_CTRL.INSERT_DT REG0XD[7:5] for Jack Insertion de-bounce time = $2^{(INSERT\_DT+2)}$ mS.

JACK_DET_CTRL.EJECT_DT REG0X0D[4:2] for Jack Ejection de-bounce time = $2^{(EJECT\_DT+2)}$ mS.

JACK_DET_CTRL.JKDET_LOGIC REG0X0D[0] can change the detection logic from OR to AND.

JACK_DET_CTRL.DB_BP_MODE REG0X0D[8] allows the Jack Detection to bypass the de-bounce filter in order to go directly to the IRQ pin without a clock. In this case, one of these two registers needs to be enabled: either the register **INTERRUPT_MASK.JK_EJECT_INTP_MASKREG0XF[2]** or the register **INTERRUPT_MASK.JK_DET_INTP_MASK REG0XF[0]**..

It is recommended that the host checks for the IRQ to be consistently valid within 10 ms to avoid false detection due to glitches. Once the host validates the Jack Detection, the host needs to initiate the power up sequence and headset support sequence.

13.2 Microphone Detection

Microphone detection functions assess the presence of a headset microphone.

For the 32-Lead QFN package: SARADC can be used for microphone detection with software programming algorithm assistance. Without a microphone, when MIC BIAS is on, SARADC readings will be full scale. When a microphone is present, SARADC reading will be less than full scale.

For the 42-Ball WLCSP package: The JKDET2 pin is used as a digital input to provide the microphone detection function. The MICDET pin can be externally connected to JKDET2. Adding a 100 KOhm resistor is recommended between MICDET and JKDET2 to reduce the current. Refer to **Figure 3** for the typical Audio Jack application diagram for the WLCSP. Also, a decoupling capacitor may be needed to filter out AC noise from the microphone.

13.2.1 Key/Button Detection

Key/Button Detection allows programmable support of several eight user-defined actions such as play, record, and accept call. This feature supports up to eight distinct input levels (keys) to be detected at the microphone pin, either JKR2 or JKSLV. One Key Release level can be detected at the microphone pin. Additionally, either a long-key-press or a short-key-press can activate an interrupt on the IRQ pin. **Figure 50** provides a block diagram to illustrate how the headset buttons are detected.

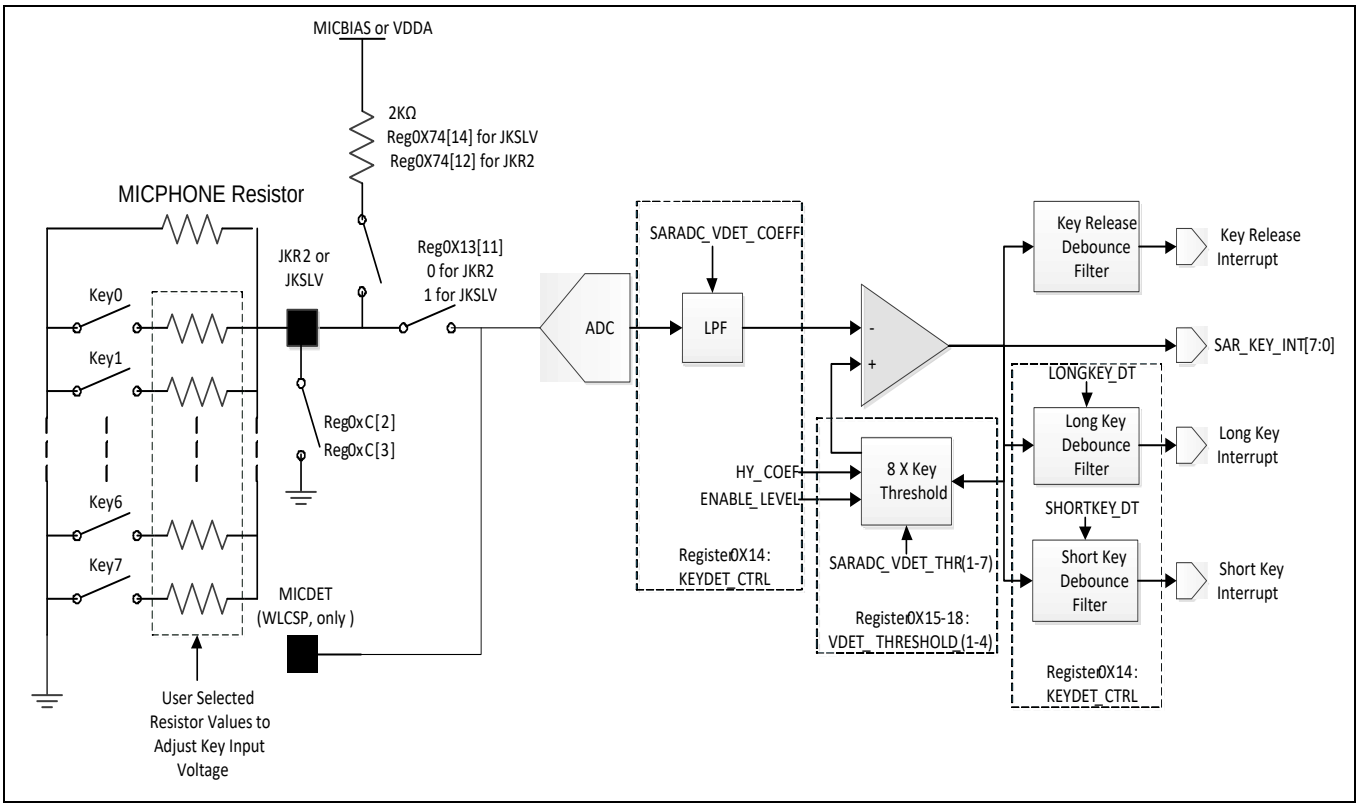


Figure 50 Key Detection

Each output signal from the eight comparators goes through three de-bounce filters (not shown). After the signals are received through the de-bounce filters, the associated interrupts are triggered and read from **INT_CLR_KEY_ STATUS REG0X11**. The options for changing the Long-Key and Short-Key de-bounce filter times are identified in **Table 30**.

Table 30 Key De-Bounce Settings

KEYDET_CTRLLONGKEY_DTREG0X14[14]]	Long Key Debounce Time
0	500 ms
1	1 sec
KEYDET_CTRLSHORTKEY_DTREG0X14[13:12]	**Short Key De-bounce Time**
00	30 ms
01	50 ms
10	100 ms
11	30 ms

13.2.2 Key Press Determination

Changes in DC level at the MIC input pins (JKR2 or JKSLV) are converted into digital representations by a Successive Approximation Register (SAR)-ADC. The SAR ADC is a simple ADC used to detect the voltage level on the MIC input pin to determine which of the 8 Keys has been pressed. The decimal value of **SARDOUT_ RAM_STATUS.SARADC_DOUT REG0X59[7:0]** can be determined using this equation:

$$SARADC = 255 \text{ x } Amb\ x\ Asar\ x\ Rp\ /\ (Rmb + Rp)$$

The various reference voltage levels are derived from the VDDA voltage supply.

If the headset Microphone bias voltage is tied to the MICBIAS pin, the SAR ADC digital output signal decimal representation can be described as:

$$SARADC = 255 \text{ x } Amb\ x\ Asar\ x\ Rp\ /\ (Rmb + Rp)$$

Amb is the MIC bias factor given by **MIC_BIAS.MICBIASLVL1 REG0X74[2:0].**

Asar is the gain of the SAR ADC, which is 1/(VDDA x **SAR_CTRL.SAR_TRACKGAIN REG0X13[10:8]**

Rmb is the MICbias series resistor, which is typically 2 kΩ .

Rp is the parallel resistance of the Microphone and the resistance of the button that is pressed.

The SAR ADC output is filtered by a programmable Low-Pass Filter allowing glitches and audio content to be removed from the ADC output data. The result can be read at any time through the I2C register at **SARDOUT_ RAM_STATUS.SARADC_DOUT REG0X59[7:0].**

The equation of the digital Low Pass Filter is as follows:

$$Yn = \alpha Xn + (1 - \alpha)Yn - 1$$

α is the coefficient of the low pass filter, α=(1/2)n

n is controlled by **KEYDET_CTRL.SARADC_VDET_COEFF REG0X14[7:4]**.

The SAR ADC output signal is fed into 8 comparators each with a unique programmable threshold level and common high and low hysteresis levels. These 8 comparators will generate 8 distinct output signals as determined by the threshold levels and external DC voltage at the JKR2 or JKSLV pin.

There are eight threshold voltages and nine different Key regions. **Figure 51** shows the nine key regions. The lowest SARADC output range indicates when Key 0 is pressed, the second indicates when Key 1 is pressed, and so on. The highest region indicates when no key has been pressed.

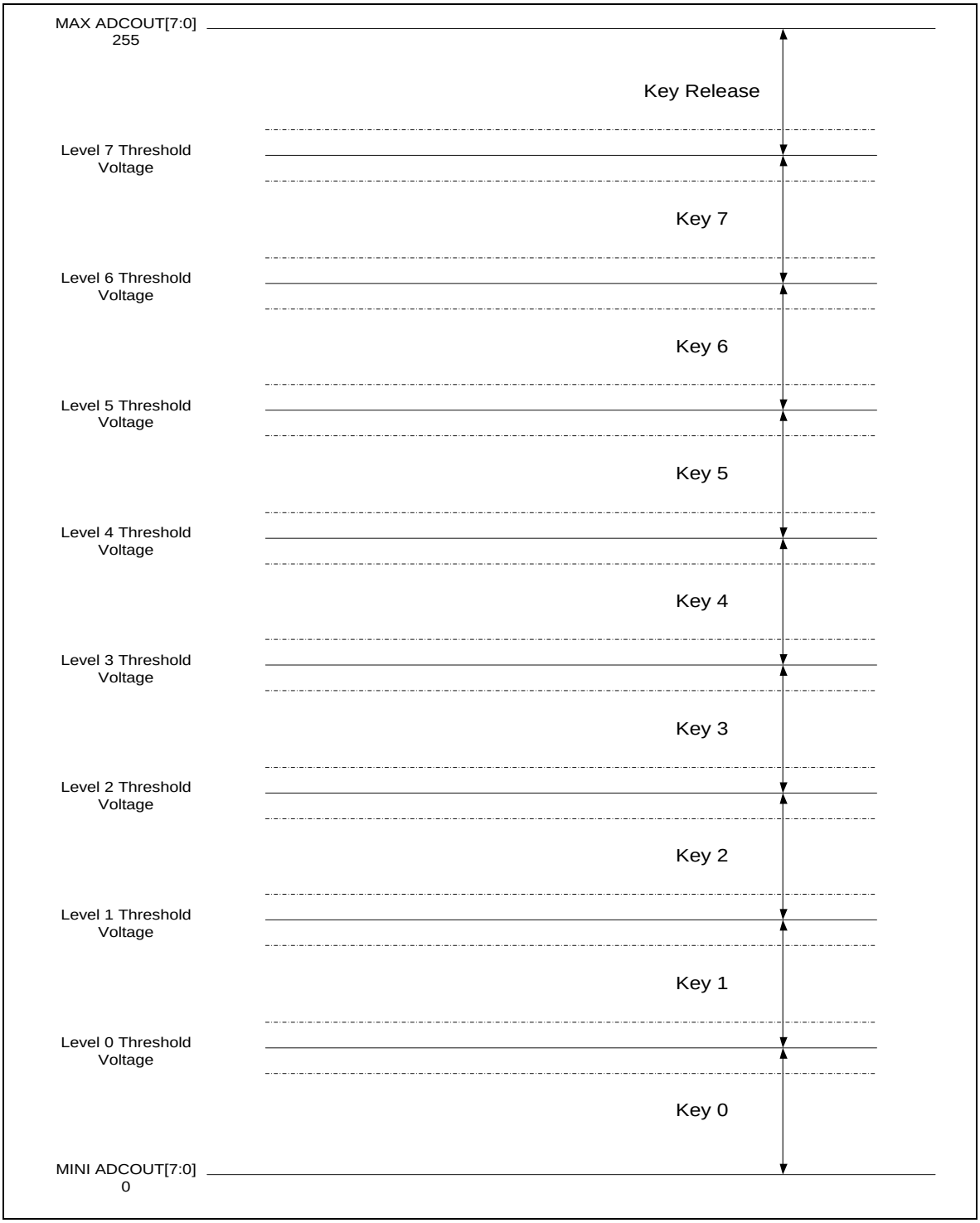


Figure 51 Keys Regions

Example

A headphone has three buttons. MICBIAS voltage is set to 1.53 x VDDA at VDDA = 1.8 V by **MIC_BIAS.MICBIASLVL1** and **SAR__TRACKGAIN** set according to **Table 32.** Microphone resistance is 10 KOhms.

- If no button is pressed, the **SARADC_ DOUT** decimal output is: **SARADC_DOUT** = 255 x 1.53 x 1.8 x 1/(1.53 x 1.8) x 10k/(2k + 10k) = 212
- When a button with 4 KOhms series resistance is pressed, the **SARADC_DOUT** output becomes: **SARADC_DOUT** = 255 x 1.53 x 1.8 x 1/(1.53 x 1.8) x 10k//4k/(2k + 10k//4k) = 150
- When a second button with 2 KOhms series resistance is pressed, the **SARADC_DOUT** output becomes: **SARADC_DOUT** = 255 x 1.53 x 1.8 x 1/(1.53 x 1.8) x 10k//2k/(2k + 10k//2k) = 116
- When the third (last) button with 1 KOhms resistance is pressed, the **SARADC_DOUT** output becomes: **SARADC_DOUT** = 255 x 1.53 x 1.8 x 1/(1.53 x 1.8) x 10k//1k/(2k + 10k//1k) = 80.

According to **Figure 51**, three threshold voltage levels for the Key2 level could be set by ENABLE_LEVEL=010.

- The first threshold voltage could be 98, the middle of 116 and 80 from the second and third buttons, in the example above.
  The Hysteresis value can be set to 15, -- less than 50% of difference 116 and 80.
  SARADC_VDET_THR0=98=8'b01100010,
  HY_COEFF[3:0]=15=4'b1111
- The second threshold voltage could be 133, the middle of 150 and 116 from the first and second buttons, in the example above.
  The Hysteresis value can be set to 15, -- less than 50% of difference 150 and 116.
  SARADC_VDET_THR1=133=8'b10000101,
  HY_COEFF[3:0]=15=4'b1111
- The third threshold voltage could be 181, the middle of 150 and 212 from no button being pressed and the first button, in the example above.
  The Hysteresis value can be set to 15, -- less than 50% of difference 116 and 212.
  SARADC_VDET_THR2=150=8'b10010110
  HY_COEFF[3:0]=15=4'b1111

Combining the results for all three threshold voltages yields a single HY_COEFF[3:0]=15=4'b1111

13.2.3 Microphone Detection Application Notes

KEYDET_CTRL.HY_COEFF_REG0X14[3:0] can be used to change the hysteresis range. As shown by the dashed lines in Figure 51:

- The SARADC voltage must be lower than the hysteresis range to go into the lower level Key.
- The SARADC voltage must be higher than the hysteresis range to go into a higher level key.

If the voltage sampled is in the hysteresis range, the level needs to be compared to the previous state. For example, if the previous stat is Key 2 and the new sample is in the Key 1 hysteresis range, the logic will claim the status is still Key 2.

The register **KEYDET_CTRL.ENABLE_LEVEL REG0X14[10:8]** selects the number of keys being used. If the register **KEYDET_CTRL.ENABLE_LEVEL REG0X14[10:8]** is set to 3'b010, then only three keys will be supported: (Key0, Key1, and Key2). The threshold voltages must be set up using **SARADC_ VDET_THR2.**

Any voltage sampled above the Level 2 threshold will be considered as a Key Release.

13.2.4 SAR ADC Sampling and Conversion

Once the SARADC has been enabled using **SAR_CTRL_REG0X13**, the SAR ADC enters a sampling phase. In this phase, the voltage level on the MIC input is sampled at a speed determined by **SAR_CTRL**. This time can be adjusted from 2 µs to 16 µs, doubling each step. During the sampling phase, the sample signal will be held HIGH together with the MSB and held LOW with the LSB.

Note that the maximum input current of the ADC can be reduced by selecting a bigger input resistor in series with the sampling capacitor. The value of the input resistor can track the sampling time.

Table 31 lists the resistor values that can be selected for **SAR_CTRL.RES_SEL REG0X13[6:4].**

Table 31 SAR ADC Current Limit Resistor Selection

SAR_CTRL.**RES_SEL REG0X13[6:4]**	**Resistor Value [Ohm]**
000	35 k
001	70 k
010	170 k
011	360 k
1xx	short

The register **SAR_CTRL.SAMPLE_SPEED REG0X13[1:0]]** is used to set the SARADC sampling rate. Before changing the sampling rate, **SAR_CTRL.SAR_ENA REG0X13[12]** must be set to '0'. After the sample speed is set, then SAR_ENA sets to '1'.

After the sampling phase, the ADC enters a conversion phase that consists of eight compare cycles. Each of these compare cycles can last from 500 ns to 4 µs, doubling each step. To adjust the compare time, use **SAR_CTRL.COMP_SPEED REG0X13[3:2]**.

Note that **SAR_CTRL** can be used to set the voltage of the 5 V PMOS in the Track-and-Hold portion of the ADC. Setting this register makes the back gate voltage equal to MICBIAS ('0') or MICVDD ('1'). It is also important to set the gain in **SAR_CTRL.SAR_TRACKGAIN REG0X13[10:8]**. Because the output of MICBIAS is adjustable, the input voltage range of the ADC must track the output voltage of MICBIAS**. Table 32** shows the settings for these registers.

Table 32 SAR ADC MICBIAS Gain Tracking Settings

MIC_BIAS.MICBIASLVL1REG0X74[2:0]	**MICBIAS Level**	**SAR_ TRACKGAINREG0X13[10:8]**
000	1.0*VDDA	000
001	1.0*VDDA	001
010	1.1*VDDA	010
011	1.2*VDDA	011
100	1.3*VDDA	100
101	1.4*VDDA	101
110	1.53*VDDA	110
111	1.53*VDDA	111

13.3 Jack Interrupt Sequence

The NAU88L25B includes an interrupt sequence feature that can detect various types of interrupts and trigger associated sequences. This system works by continually waiting for an interrupt to occur. Once an interrupt occurs, the x10 register is read to determine the type of interrupt while the x11 register is reset to prepare for further interrupts.

13.3.1 Jack Insertion Detection

This feature detects when a headset is inserted into the external headset jack interrupt and clears the x11 register to reset for further interrupts. Refer to **Figure 52** for the flowchart of Jack Insertion detection. The impedance measurement mode is set up to read the impedance of the headset and the successive approximation register is read to determine whether or not both the headphone and the microphone need to be enabled. It then resumes waiting for further interrupts.

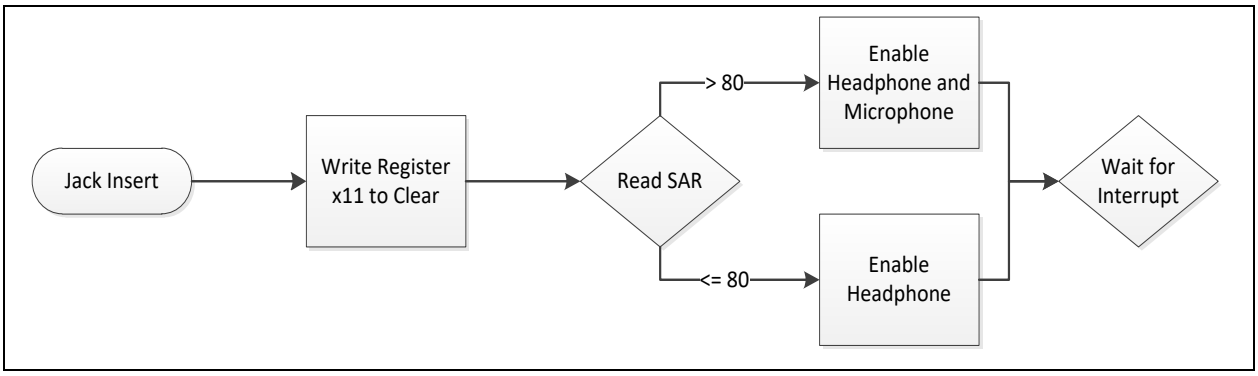


Figure 52 Jack Insertion Flowchart

13.3.2 Jack Ejection Detection

This feature detects when a headset is ejected from the external headset jack and clears the x11 register to reset for further interrupts. The headphone and microphone are disabled accordingly and resume waiting for further interrupts. The flowchart for Jack Ejection detection is shown in **Figure 53**.

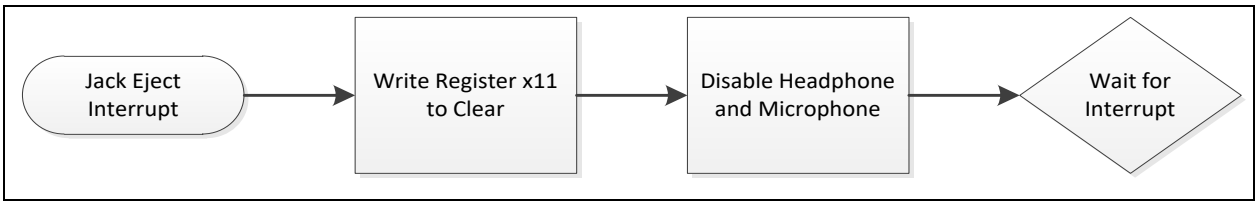


Figure 53 Jack Ejection Flowchart

13.3.3 Short Key Press

This feature detects the software programmable user-defined actions as short-key or long- key press interrupts and clears the x11 register to reset for further interrupts after reading the key. The feature then waits for a second interrupt and clears the x11 register to reset for further interrupts and reads the x10 register to determine the type of key press. The associated sequence is then triggered and resumes waiting for further interrupts. See **Figure 54** for the Short-Key Press flowchart.

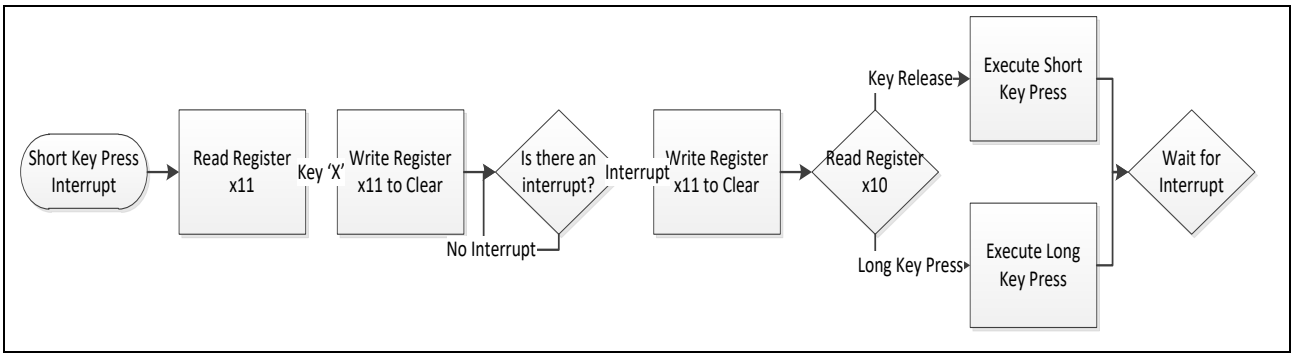


Figure 54 Short Key Press Flowchart

13.3.4 Key Release

This feature detects the edge case where the key press interrupt is not followed by a release interrupt until later on in the sequence and clears the x11 register to prepare for further interrupts.The flowchart for Key Release is shown in **Figure 55**.

Figure 55 Key Release Flowchart

14 Registers

14.1 Basic Register Sequences

The following register sequences are provided as a general guide to setting up the NAU88L25B.

14.1.1 Enable VREF and General Bias

Reset all registers by writing anything to register 0x00 twice.

1. Enable VREF in High Impedance Mode by setting **BIAS_ADJ.VMIDEN REG0X66[6]** = '1' and **BIAS_ADJ.VMIDSEL REG0X66[5:4]** = 10.
2. Wait for 2 ms
3. Set **BOOST.BIASEN REG0X76[12]** = '1'.
4. Set **BOOST.PDVMDFST REG0X76[13]** = '1'.

The chip is now ready to enable analog block functions.

14.1.2 Enable or Disable Input PGA

To Enable PGA:

1. Set **BIAS_ADJ.MUTEL REG0X66[13]** = '1'.
2. Set **POWER_UP_CONTROL.PUPR REG0X7F[14]** = '1'.
3. Select the input using **FEPGA.FEPGA_MODEL REG0X77[3:0]**, **ANALOG_**
4. **CONTROL.MUTEMICP REG0X6A[3], ANALOG_**
5. **CONTROL.MUTEMICN REG0X6A[2].**
6. Set **FEPGA.ACDC_CTRL REG0X77[15:14]** to the inputs used.
7. Set **BOOST.DISCHRG REG0X76[11]** = '1'.
8. Wait 1 ms.
9. Set **BOOST.DISCHRGREG0X76[11**] = '0'.
10. Set **FEPGA.ACDC_CTRL REG0X77[15:14]** = '0'.
11. Set **POWER_UP_CONTROL.FEPGA_GAIN REG0X7F[13:8]** for gain.
12. Wait 10 ms (or more depending on pop).
13. Set **ANALOG_**
14. **CONTROL.MUTEMICP REG0X6A[3], ANALOG_**
15. **CONTROL.MUTEMICN REG0X6A[2]** = '0'.
16. (Optional) **SET_BOOST.STG2_SEL REG0X76[14]** = '1' for better Total Harmonic Distortion (THD) performance.

To Disable Left & Right PGA:

1. Set **BIAS_ADJ.MUTEL REG0X66[13**] = '1'.
2. Set **POWER_UP_CONTROL.PUFEPGA REG0X7F[14]** = '0'.

14.1.3 Enable Analog-to-Digital Converter

1. Set **ANALOG_ADC_2.PDNOTL REG0X72[6]** = '1'.
2. Set **ANALOG_ADC_2.LFSRRESETNREG0X72[5]** = '0'.
3. Set **ANALOG_ADC_2.LFSRRESETNREG0X72[5]** = '1' on the next I2C command.

14.1.4 Enable or Disable Frequency Locked Loop

It is assumed that VREF, **BOOST.BIASEN_REG0X76[12]**, and the System Master Clock are running.

To Enable FLL:

1. Set **FLL6.DCO_EN REG0X09[15]** = '0'.
2. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '0'.
3. Program the remaining FLL registers from **FLL1_REG0X04** through **FLL_VCO_RSV REG0X0A.**
4. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '1'.

To Disable FLL:

1. Set **FLL6.DCO_EN REG0X09[15]** = '0'.
2. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '0'.

To Enable Free Running Mode:

1. Set **FLL6.DCO_EN REG0X09[15]** = '0'.
2. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '0'.
3. Set **FLL6.DCO_EN REG0X09[15]** = '1'.
4. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '1'.

To Enable Free Running Mode with Reference Clock:

1. Set **FLL6.DCO_EN REG0X09[15]** = '0'.
2. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '0'.
3. Program the remaining FLL registers from **FLL1 REG0X04** through **FLL_VCO_RSV REG0X09.**
4. Set **CLK_DIVIDER.SYSCLK_SRC REG0X03[15]** = '1'.
5. Wait for the FLL to lock by monitoring the CSB pin.
6. Disable/Remove reference clock.

14.1.5 Enable or Disable Digital-to-Analog Converter

To Enable DAC:

1. Set up the I2S to DAC paths
2. Set **RDAC.CLK_DAC_EN REG0X73[9:8]** = '11'.
3. Set **RDAC.DACVREFSELLO REG0X73[3:2]** = '10'.
4. Set **RDAC.DAC_EN REG0X73[13:12]** = '11'.
5. Set **CHARGE_PUMP_AND_POWER_DOWN_CONTRL.PDB_DACREG0X80[9:8]** = '00'.

To Disable the DAC:

1. Set **RDAC.CLK_DAC_EN REG0X73[9:8]** = '00'.
2. Set **RDAC.DACVREFSELLO REG0X73[3:2]** = '00'.
3. Set **RDAC.DAC_EN REG0X73[13:12]** = '00'.
4. Set **CHARGE_PUMP_AND_POWER_DOWN_CONTRL.PDB_DAC REG0X80[9:8]** = '11'.
5. Disable the I2S to DAC paths.

14.1.6 Enable or Disable Headphone

It is assumed that VREF, **BOOST.BIASEN REG0X76[12]**, the System Master Clock, and the DAC are running.

To Enable the Headphone:

1. Set **HSD_CTRL.MANU_SPKR_DWN1R REG0XC[1]** and **HSD_CTRL.MANU_SPKR_DWN1L REG0XC[0]** both to '1'.

2. Set **CHARGE_PUMP_AND_POWER_ DOWN_CONTRL.RNIN REG0X80[5]** and **CHARGE_PUMP_AND_POWER_ DOWN_CONTRL.JAMFORCE2 REG0X80[7]** both = '1'.
3. Enable Class-G if desired.
4. Set **BIAS_ADJ.TESTDACREG0X66[9:8]** = '11'.
5. Set **CHARGE_PUMP_AND_POWER_ DOWN_CONTRL.PDB_DAC_REG0X80[13:12]** = '11'.
6. Set **BIAS_ADJ.TESTDACREG0X66[9:8]** = '11'.
7. Set **BOOST.BOOSTGDIS REG0X76[8]** ='1'.
8. Set **TRIM_SETTINGS.DRV_IBCTRHS REG0X68[15]** = '1'
9. Set the registers **POWER_UP_ CONTROL.PUP_INTEG REG0X7F[5:4]** and **POWER_UP_ CONTROL.PUP_DRV_INSTG REG0X7F[3:2]** ='11'.
10. Set **POWER_UP_ CONTROL.PUP_MAIN_DRV REG0X7F[1:0]** = '11' at next I2C command.
11. Set **HSD_CTRL.MANU_SPKR_DWN1R** & **MANU_SPKR_DWN1L** both to '0' **REG0X0C[1:0]** = '00' at the next I2C command.
12. **BIAS_ADJ.TESTDAC REG0X66[9:8]** = '0' at the next I2C command.

To Disable the Headphone:

1. Set **BIAS_ADJ.TESTDAC REG0X66[9:8]** = '11' at the next I2C command.
2. Set **POWER_UP_ CONTROL.PUP_MAIN_DRV REG0X7F[1:0]** = '00' and **HSD_CTRL. MANU_SPKR_DWN1R** & **MANU_SPKR_DWN1L** both to '1' and **REG0X0C[1:0]** = '11' at the next I2C command.
3. Set the registers **POWER_UP_ CONTROL.PUP_INTEGREG0X7F[5:4] AND POWER_UP_ CONTROL.PUP_DRV_INSTG REG0X7F[3:2]** = '00' on the next I2C command.

The disable sequence is necessary only when a headset is connected. If the headset is disconnected, everything can be powered down at once.

14.1.7 Enable DAC to Headphone Low-Power/MP3 Playback Mode

It is assumed that the DAC to headphone path is running and the System Clock is running. VDDC must be set to .2 V for lowest power, FS = 44.1 kHz, 16 bits and all unused functions are powered off or gated off.

1. Set **TRIM_SETTINGS.DRV_IBCTRHS REG0X68[15]** = '0'.
2. Set **TRIM_SETTINGS.DRV_ICUTHS REG0X68[14]** = '1'.
3. Set **BOOST.BOOSTDIS REG0X76[9]** = '1'.
4. Set **RDAC.DACVREFSEL REG0X73[3:2]** from '10' to '00'.
5. Set **BIAS_ADJ.BIASADJREG0X66[1:0]** = '10'.
6. Set **DAC_CTRL1.DAC_RATEREG0X2C[2:0]** = '100' for OSR=32.
7. Set **CLK_DIVIDER.CLK_DAC_SRC REG0X03[5:4]** = '11'.
8. Set **DAC_CTRL1.DISABLE_DEM REG0X2C[15]** = '1'.

14.1.8 Headset or Button Detection

It is assumed the NAU88L25B Audio CODEC is not in Jack Detect Debounce Bypass Mode (having a clock for Jack Detection).

1. Set bias circuit by **BIAS_ADJ.VMID REG0X66[6]** ='1' and **BIAS_ADJ.VMIDSEL[1:0] REG0X66[5:4]** ='1', after 2 ms.
2. Set enable global analog bias by **BOOST.BIASEN REG0X76[12]** ='1' and VMID pre-charge is disabled by **BIAS_ADJ.PVDMDFST REG0X76[13]** ='1'.
3. Enable debounce clock **ENA_CTRL.CLK_SAR_EN REG0X01[1]** ='1'.
4. Set insert debounce time **JACK_DET_CTRL.INSERT_DT REGX0D[7:5]** = '7' (Maximum debounce time.).
5. Set eject debounce time **JACK_DET_CTRL.EJECT_DT REGX0D[4:2]** = '7' (Maximum ejection debounce time.).
6. For SAR ADC, set Reg0X13-18 to the desired values (will depend on which headset is used).
7. **SAR_CTRL.SAR_ENA REG0X13[12]** ='1'.
8. **HSD_CTRL.HSD_AUTO_MODE[6]** ='1' to enable headset automatically detection.
9. **INTERRUPT_MASK.IRQ_OE REG0XF[11]** = '1' to enable IRQ output.
10. **INTERRUPT_DIS_CTRL. REG0X12** = '0x0010' to disable MIC detection interrupt '
11. Set MIC bias output = VDDA by **MIC_BIAS.MICBIASLVL1[2:0] REG0X74[2:0]** = '0', then turn on MIC BIAS **MIC_BIAS.POWERUP REG74[8]** = '1' (Will vary by customer requirement.).

14.1.9 Write or Read Programmable Bi-Quad Filters

To Write Programmable Bi-Quad Filters:

1. Write **BIQ_CTRL.BIQ_WRT_EN REGX20[4]** = '0' //to disable write .
2. Write **BIQ_CTRL.BIQ_PATH_SE REGX20[0]** = '0' for ADC Path or '1' for DAC Path.
3. Write Bi-Quad parameters to REG0X21 ^~ 0X2A:
    a. Each Parameter will be in the form [sign]XX.XXXXXXXXXXXXXXX.
    b. To obtain coefficient A1 to be -1.28461: write **REG0X22=X0005** as -1=b101=x5 and **REG0X21=0X6F2D** as 28461 = b110111100101101 = 6F2D.
4. Write **BIQ_CTRL.BIQ_WRT_EN REGX20[4]** = '1' //to load REG0X21-0X2A to the Bi-Quad Filter.

To Read Programmable Bi-Quad Filters:

1. Write **BIQ_CTRL.BIQ_WRT_EN REGX20[4]** = '0' //to disable write.
2. Write **BIQ_CTRL.BIQ_PATH_SE REGX20[0]** = '0' for ADC Path or '1' for DAC Path.
3. Read REG0X21-0X2A.

14.2 Register Map

Table 33 Register Map

REG	Function
0	SOFTWARE_RST
1	ENA_CTRL
2	I2C_ADDR_SET
3	CLK_DIVIDER
4	FLL1
5	FLL2
6	FLL3
7	FLL4
8	FLL5
9	FLL6
A	FLL_VCO_RSV
C	HSD_CTRL
D	JACK_DET_CTRL
F	INTERRUPT_MASK
10	IRQ_STATUS
11	INT_CLR_KEY_STATUS
12	INTERRUPT_DIS_CTRL
13	SAR_CTRL
14	KEYDET_CTRL
15	VDET_THRESHOLD_1
16	VDET_THRESHOLD_2
17	VDET_THRESHOLD_3
18	VDET_THRESHOLD_4
19	GPIO34_CTRL
1A	GPIO12_CTRL
1B	TDM_CTRL
1C	I2S_PCM_CTRL1
1D	I2S_PCM_CTRL2
1E	LEFT_TIME_SLOT
1F	RIGHT_TIME_SLOT
20	BIQ_CTRL
21	BIQ_COF1
22	BIQ_COF2
23	BIQ_COF3
24	BIQ_COF4
25	BIQ_COF5
26	BIQ_COF6
27	BIQ_COF7
28	BIQ_COF8

REG	Function
29	BIQ_COF9
2A	BIQ_COF10
2B	ADC_RATE
2C	DAC_CTRL1
2D	DAC_CTRL2
2F	DAC_DGAIN_CTRL
30	ADC_DGAIN_CTRL
31	MUTE_CTRL
32	HSVOL_CTRL
33	DACL_CTRL
34	DACR_CTRL
38	ADC_DRC_KNEE_IP12
39	ADC_DRC_KNEE_IP34
3A	ADC_DRC_SLOPES
3B	ADC_DRC_ATKDCY
45	ADC_DRC_KNEE_IP12
46	DAC_DRC_KNEE_IP34
47	DAC_DRC_SLOPES
48	DAC_DRC_ATKDCY
4C	MODE_CTRL
50	CLASSG_CTRL
51	OPT_EFUSE_CTRL
55	MISC_CTRL
58	I2C_DEVICE_ID
59	SARDOUT_RAM_STATUS
66	BIAS_ADJ
68	TRIM_SETTINGS
69	ANALOG_CONTROL_1
6A	ANALOG_CONTROL_2
71	ANALOG_ADC_1
72	ANALOG_ADC_2
73	RDAC
74	MIC_BIAS
76	BOOST
77	FEPGA
7F	POWER_UP_CONTROL
80	CHARGE_PUMP_AND_POWER_DOWN_CONTRL
81	CHARGE_PUMP_INPUT_READ
82	GENERAL_STATUS

14.3 Control and Status Registers

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
0	SOFTWARE_RST	SOFTWARE_RESET																	**Hardware Reset** (Write any value ***once*** to reset all the registers.)
1	ENA_CTRL	CMLCK_ENB																	**PGA Common Mode Lock Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		CLK_DAC_INV																	**DAC Clock Inversion In Analog Domain Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		RDACEN																	**Right Channel DAC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		LDACEN																	**Left Channel DAC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADCEN																	**ADC Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DCLK_ADC_EN																	**ADC Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DCLK_DAC_EN																	**DAC Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		CLK_MODE_EN																	**Mode Ctrl Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		CLK_I2S_EN																	**I2S Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		CLK_BIST_EN																	**BIST Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		RESERVED																	**RESERVED**
		CLK_SAR_EN																	**SAR Clock Enable Control** (For jack or button/key detection) 0 = Disable 1 = Enable (DEFAULT)
		CLK_DRC_EN																	**DRC Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	**0x00FF**
2	I2C_ADDR_SET	I2C_LSB_VALUE																	**Set I2C Address LSB Value** Bit0 = 0 I2C LSB is from GPIO in directly Bit0 = 1 to latch the I2C LSB value
		I2C_ADDDR_SEL																	**When read back from REG0x02** Bit1 is saved as I2C LSB value Bit0 is saved as I2C_ADDR_SEL
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
3	CLK_DIVIDER	SYSCLK_SRC																	**Master Clock Source Select** 0 = MCLK_PIN (DEFAULT) 1 = ½ DCO_CLK
		CLK_CODEC_SRC																	**ADC & DAC Clock Source Select** 0 = From internal MCLK (DEFAULT) 1 = From MCLK_PIN or ½ DCO_CLK
		CLK_DAC_PL																	**DAC Clock Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
		CLK_ADC_PL																	**ADC Clock Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		CLK_GPIO_SRC																	**Scaling Divider For GPIO Clock From MCLK** 00 = 1/8 (DEFAULT) 01 = 1 10 = 1/2 11 = 1/4
		CLK_ADC_SRC																	**Scaling Divider For ADC Clock From CODEC_SRC** 00 = 1 01 = 1/2 (DEFAULT) 10 = 1/4 11 = 1/8
		CLK_DAC_SRC																	**Scaling Divider For DAC Clock From CODEC_SRC** 00 = 1 01 = 1/2 (DEFAULT) 10 = 1/4 11 = 1/8
		MCLK_SRC																	**Scaling Divider For MCLK From SYSCLK_SRC** 0000 = 1 (DEFAULT) 0001 = Inverted 0010 = 1/2 0011 = 1/4 0100 = 1/8 0101 = 1/16 0110 = 1/32 0111 = 1/3 1000 = 1 1001 = Inverted 1010 = 1/6 1011 = 1/12 1100 = 1/24 1101 = 1/48 1110 = 1/96 1111 = 1/5
		DEFAULT	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0x0050
4	FLL1	FLLISELDAC																	**Increase Drive Strength Of FLL DAC** 000 = (DEFAULT)
		ICTRL_LATCH																	**FLL Latch Drive Strength Multiplier** (When FLL running at high frequency with long decimal number, DSP needs to operate at high speed. By adjusting ICTRL_LATCH, FLL DSP can optimize between performance and power consumption (111 has highest power consumption for FLL DSP.) On the other hand, (DCO frequency)/(FLL input reference frequency)=integer, default setting can be used to reduce power. This register is using thermometer coding.) 000 = (DEFAULT) 001 = 1x 010 = 1.5x 011 = 2x 110 = 2.5x 111 = 3x
		ICTRL_V2I																	**Amp Half Bias-Current Select** (Amp bias current must be reduced to 50% of its nominal value.) 00 = No power reduction (DEFAULT) 01 = Half bias current on FLL_BIAS_AMP2X 10 = Half bias current on FLL_BIAS_AMP 11 = Half current on both amps
		FLL_LOCK_BP																	**Manual Force of FLL Lock Enable Control** 0 = Disable (DEFAULT) 1 = Enable

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		FLL_RATIO																	**Input Clock Frequency Select** 0000001 = For input clock frequency ≥ 512KHz 0000010 = For input clock frequency ≥ 256KHz 0000100 = For input clock frequency ≥ 128KHz 0001000 = For input clock frequency ≥ 64KHz 0010000 = For input clock frequency ≥ 32KHz 0100000 = For input clock frequency ≥ 8KHz 1000000 = For input clock frequency ≥ 4KHz
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
5	FLL2	FLL_FRAC																	**FLL 16-bit Fractional Input**
		DEFAULT	0	0	1	1	0	0	0	1	0	0	1	0	0	1	1	0	**0x3126**
6	FLL3	GAIN_ERR																	**FLL Gain Error** (The threshold is comparison between DCO and target frequency. 1111 has the most accurate DCO to target frequency. However, the gain error setting conditionally and inversely depends on FLL input reference clock rate. Higher FLL reference input frequency can only set lower gain error, such as 0000 for input reference from MCLK=12.288MHz. On the other side, if FLL reference input is from Frame sync, 48KHz, higher error gain can apply such as 1111.) 0000 = (DEFAULT) 0001 = x1 0010 = x2 0011 = x3 0100 = x4 0101 = x5 0110 = x6 0111 = x8 1000 = x9 1001 = x10 1010 = x12 1011 = x16 1100 = x17 1101 = x18 1110 = x20 1111 = x24
		FLL_CLK_REF_SRC																	**FLL Reference CLK Source Select** 00 = MCLK pin (DEFAULT) 01 = MCLK pin 10 = BCLK pin
		FLL_INTEGER																	**FLL 10-bit Integer Input**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0x0008**
7	FLL4	RESERVED																	**RESERVED**
		FLL_CLK_REF_DIV_4CHK																	**FLL CLK_REF Divider For Accurate Lock Detection** 000 = 1 (DEFAULT) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		FLL_CLK_REF_DIV																	**FLL Pre-Scale Divider** 00 = 1 (DEFAULT) 01 = 1/2 10 = 1/4 11 = 1/8
		FLL_N2																	**FLL 10-bit Integer DCO Divider For FLL Filter Clock** (The value is in orders of 2. When 0x8[13]=1, it selects DCO clock as FLL filter clock. The filter clock rate needs to be less than 1Mhz. With setting proper value, filter clock can be divided down from DCO clock. For example, DCO runs at 96Mhz, by setting value 0x60=96, filter clock becomes 1MHz.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x0010**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
8	FLL5	RESERVED																	**RESERVED**
		CHB_FILTER_EN																	**FLL Loop Filter To Reduce FLL Output Noise Enable Control** (Especially, (DCO frequency)/(FLL input reference frequency) is not an integer.) 0 = Disable (DEFAULT) 1 = Enable (by REG0x09[13:12])
		CLK_FILTER_SW																	**Select Filter Clock Source Select** 0 = Select REFCLK 1 = Select divided DCO clock based on register FLL_N2 (DEFAULT)
		FILTER_SW																	**FLL Loop Filter Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		FLL_LOCK_LENGTH																	**Set FLL Lock-In Length** (Set the time that FLL must stay within the lock-in range before lock signal goes high.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
9	FLL6	DCO_EN																	**FLL Free-running Mode Enable Control** (Need to enable 0x76[12] BIASEN) 0 = Disable (DEFAULT) 1 = Enable
		SDM_EN																	**FLL Sigma-Delta Modulator Enable Control** (To create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not an integer. If the ratio is integer, it still can be on for lower noise output but higher power consumption.) 0 = Disable 1 = Enable (DEFAULT)
		CUTOFF500																	**FLL 500KHz Cut-off Frequency Enable Control** (If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give the best FLL performance with the highest power consumption.) 0 = Disable 1 = Enable (DEFAULT)
		CUTOFF600																	**FLL 600KHz Cut-off Frequency Enable Control** (If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give a moderate FLL performance with moderate power consumption.) 0 = Disable (DEFAULT) 1 = Enable
		FLL_FLTR_DITHER_SEL																	**Filter Output Random Bit Select** 00 = No dither (DEFAULT) 01 = The LSB is a random bit 10 = Two LSBs are random bits 11 = Three LSBs are random bits
		FLL_SD_DITHER_SEL																	**Input Of SD Modulator Random Bit Select** 00 = No dither (DEFAULT) 01 = The LSB is a random bit 10 = Two LSBs are random bits 11 = Three LSBs are random bits
		DLR																	**FLL Dynamic Lock Range** 0000 = (DEFAULT)
		DEFAULT	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x6000**
A	FLL_VCO_RSV	DOUT2VCO_RSV																	**FLL DCO Frequency Free-running Mode**
		DEFAULT	1	1	1	1	0	0	0	1	0	0	1	1	1	1	0	0	**0xF13C**
C	HSD_CTRL	RESET_HSD																	**Reset Headset Detection**
		HSD_AUTO_MODE																	**Headset Detection Auto Mode**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		MANUAL_START																	**Manual Access START**
		MANU_ENGND1																	**Manual Access JKR2** (For headset detection auto mode) 0 = Open 1 = Shorted to GND (DEFAULT)
		MANU_ENGND2																	**Manual Access JKSLV** (For headset detection auto mode) 0 = Open 1 = Shorted to GND (DEFAULT)
		MANU_SPKR_DWN1R																	**Manual Access SPKR_DWN1R** (For headset detection auto mode) 0 = Open (DEFAULT) 1 = Shorted to GND (16 ohm internal resistor)
		MANU_SPKR_DWN1L																	**Manual Access SPKR_DWN1L** (For headset detection auto mode) 0 = Open (DEFAULT) 1 = Shorted to GND (16 ohm internal resistor)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	**0x000C**
D	JACK_DET_CTRL	JK_3_PL																	**Jack Detection Source 3 Configuration** (For WLCSP package only) 00 = From GPIO3JD2 (DEFAULT) 01 = From Inverted GPIO3JD2 10 = Ignore the input and set to 0 11 = Ignore the input and set to 1
		JK_2_PL																	**Jack Detection Source 2 Configuration** (For WLCSP package only) 00 = From JKDETL (DEFAULT) 01 = From Inverted JKDETL 10 = Ignore the input and set to 0 11 = Ignore the input and set to 1
		JK_1_PL																	**Jack Detection Source 1 Configuration** 00 = From GPIO2JD1 (DEFAULT) 01 = From Inverted GPIO2JD1 10 = Ignore the input and set to 0 11 = Ignore the input and set to 1
		JD_RESTART																	**Manual Restart Jack Detection** (Toggle this bit to 1 and then to 0 to restart the jack detection.)
		DB_BP_MODE																	**Jack Detect De-bounce Bypass** 0 = Enable de-bounce circuit (need to set REG4B[0] = 1 to enable the clock) (DEFAULT) 1 = Bypass the de-bounce circuit
		INSERT_DT																	**Insertion De-Bounce Time** 2^(INSERT_DT +2) ms
		EJECT_DT																	**Ejection De-Bounce Time** 2^(EJECT_DT +2) ms
		JKDET_PL																	**Jack Insertion/ Detection Logic Polarity** 0 = Invert the JACK detection logic before de-bounce circuit (DEFAULT) 1 = Non-inverted
		JKDET_LOGIC																	**Jack Detection Logic Control** 0 = OR gate (DEFAULT) 1 = AND gate
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
F	INTERRUPT_MASK	IRQ_PL																	**IRQ Logic Select** 0 = Active low (DEFAULT) 1 = Active high
		IRQ_PS																	**IRQ Pin Pull Select** 0 = Pull down (DEFAULT) 1 = Pull up
		IRQ_PE																	**IRQ Pin Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_DS																	**IRQ Drive Current Select** 0 = Low drive current (DEFAULT) 1 = High drive current

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		IRQ_OE																	**IRQ Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		HSD_ COMPLETE_ INTP_MASK																	**Headset Detection Complete Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		APR_EMRGE NCY_SHTDW N1_INTP_MA SK																	**APR Emergency Shutdown Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		RMS_INTP_ MASK																	**RMS Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		KEY_ RELEASE_ INTP_MASK																	**Key Release Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		LONG_ KEYINTP_ MASK																	**Key Pressed Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		SHORT_KEY _INTP_MASK																	**Missing MCLK Detection Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		MIC_DET_ INTP_MASK																	**MIC Detection Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		JK_EJECT_ INTP_MASK																	**Jack Ejection Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		JK_DET_ INTP_MASK																	**Jack Insertion Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
10	IRQ_STATUS	HSD_COMPL ETE_ INT																	**Headset Detection Complete IRQ**
		APR_EMRGN CY_SHTDWN																	**APR Emergency Short Circuit Shutdown IRQ**
		RMS_INT																	**Impedance Measurement IRQ Status**
		KEY_RELEA SE_INT																	**Key Release for Key Detection IRQ Status**
		LONG_KEY_ INT																	**Long Key Detection IRQ Status**
		SHORT_KEY _INT																	**Short Key Detection IRQ Status**
		MIC_DET_IN T																	**MIC Detection IRQ Status**
		JACK_EJCT_ IRQ																	**Jack Ejection IRQ Status** 00 = Cleared state 01 = Jack ejection detected 10 = A jack ejection was cleared due to a jack insertion 11 = Undefined
		JACK_DET_ IRQ																	**Jack Insertion IRQ Status** 00 = Cleared state 01 = Jack ejection detected 10 = A jack insertion interrupt was cleared due to jack removal detection 11 = Undefined
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**READ ONLY 0x0000**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
11	INT_CLR_KEY_STATUS	INT_CLR_KEY_STATUS																	**Write Operation:** (Write bits[15:0] clear corresponding REG10 [15:0]. Write 1s to bits that you want to reset to 0, except) Bit0 or Bit1 = clear Jack insertion interrupt Bit2 or Bit3 = clear Jack ejection interrupt **Read Operation:** REG11[15:0]--- RD_SAR level Key Detection statues for each Key Bit 0 = Long Key 0 Bit 1 = Long Key 1 Bit 2 = Long Key 2 Bit 3 = Long Key 3 Bit 4 = Long Key 4 Bit 5 = Long Key 5 Bit 6 = Long Key 6 Bit 7 = Long Key 7 Bit 8 = Short Key 0 Bit 9 = Short Key 1 Bit 10 = Short Key 2 Bit 11 = Short Key 3 Bit 12 = Short Key 4 Bit 13 = Short Key 5 Bit 14 = Short Key 6 Bit 15 = Short Key 7
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Write**
12	INTERRUPT_DIS_CTRL	KEY_RELEASE_CLR_INTR																	**Auto Clear Short & Long Key Interrupt Status** (When key release interrupt)
		KEY0_RELEASE_INT_DIS																	**Key_0 Release Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		LONG_KEY0_INT_DIS																	**Key_0 Long Key Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		HSD_COMPLETE_INT_DIS																	**Headset Detect Complete Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		SHRT_SHTDMN_INT_DIS																	**APR Emergency Short Circuit Shutdown Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		RMS_INT_DIS																	**RMS Impedance Measurement Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		KEY_RELEASE_INT_DIS																	**Key Release Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		LONG_KEY_INT_DIS																	**Long Key Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		SHORT_KEY_INT_DIS																	**Short Key Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		MIC_DET_INT_DIS																	**MIC Detection/Headset Configuration Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		JACK_EJCT_INT_DIS																	**Jack Ejection Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)
		JACK_DET_INT_DIS																	**Jack Insertion/Detection Interrupt Disable Control** 0 = Enable 1 = Disable (DEFAULT)

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF
13	SAR_CTRL	SAR_OUT_INV																	**SAR Output Invert Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SAR_ENA																	**SAR ADC Enable Control** (Need to enable CLK_SAR_EN) 0 = Disable (DEFAULT) 1 = Enable
		INPUT_SEL																	**SAR Input Select** 0 = Connected to JKR2 pin (DEFAULT) 1 = Connected to JKSLV pin
		SAR_TRACKGAIN																	**SAR Track Gain** (Should be same as MIC_BIAS.MICBIASLVL1)
		HV_SEL																	**High Voltage Select** 0 = Disable (DEFAULT - Supplied by MICBIAS) 1 = Enable (Supplied by VDDMIC)
		RES_SEL																	**SAR Series Resistor Select** 00 = 35 KOhms 001 = 70 KOhms (DEFAULT) 010 = 170 KOhms 011 = 360 KOhms 1XX = Shorted
		COMP_SPEED																	**Compare Cycle Time Select** **(The total conversion has 8 compare cycles.)** 00 = 500 ns 01 = 1 µs (DEFAULT) 10 = 2 µs 11 = 4 µs
		SAMPLE_SPEED																	**Sampling Phase Time Select** 00 = 2 µs 01 = 4 µs (DEFAULT) 10 = 8 µs 11 = 16 µs
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0x0015
14	KEYDET_CTRL	LONGKEY_DT																	**Long Key Detection De-bounce Time** 0 = 500 ms (DEFAULT) 1 = 1 s
		SHORTKEY_DT																	**Short Key Detection De-bounce Time** 00 = 30 ms (DEFAULT) 01 = 50 ms 10 = 100 ms 11 = 30 ms
		ENABLE_LEVEL																	**Digital Threshold Level Enable Control** 000 = Enable Until Key 0 Threshold Level 001 = Enable Until Key 1 Threshold Level (DEFAULT) 010 = Enable Until Key 2 Threshold Level 011 = Enable Until Key 3 Threshold Level 100 = Enable Until Key 4 Threshold Level 101 = Enable Until Key 5 Threshold Level 110 = Enable Until Key 6 Threshold Level 111 = Enable Until Key 7 Threshold Level
		SARADC_VDET_COEFF																	**Digital Low Pass Filter Voltage Detection Coefficient** Yn = αXn+(1-α)Yn-1 α = 1/(2)coeff
		HY_COEFF																	**Hysteresis Coefficient** (Δ = HY_COEFF Coefficient ranges from 0-15 matching the binary value. SAR ADC Level is from Low to High Voltage: Level 0 is the lowest voltage. Each Level Threshold Voltage would add hysteresis. Threshold_ON = SARADC_VDET_THRx -Δ Threshold_OFF =SARADC_VDET_THRx+Δ X is the number from 0 to 7.)

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0x0110
15	VDET_ THRESHOLD_1	SARADC_ VDET_THR0																	**Key 0 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		SARADC_ VDET_THR1																	**Key 1 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
16	VDET_ THRESHOLD_2	SARADC_ VDET_THR2																	**Key 2 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		SARADC_ VDET_THR3																	**Key 3 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
17	VDET_ THRESHOLD_3	SARADC_ VDET_THR4																	**Key 4 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		SARADC_ VDET_THR5																	**Key 5 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
18	VDET_ THRESHOLD_4	SARADC_ VDET_THR6																	**Key 6 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		SARADC_ VDET_THR7																	**Key 7 SAR ADC Threshold Level Control** (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
19	GPIO34_CTRL	GPIO4_PE																	**GPIO4SDO Pull Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		GPIO4_PS																	**GPIO4SDO Pull Select (Need to enable GPIO4_PE)** 0 = Pull Down (DEFAULT) 1 = Pull Up
		GPIO4_DS																	**GPIO4SDO Driving Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		GPIO4_OE																	**GPIO4SDO Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		GPIO3O																	**GPIO3 JD2 Output**
		GPIO3_PE																	**GPIO3JD2 Pull Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		GPIO3_PS																	**GPIO3JD2 Pull Select (need to enable GPIO3_PE)** 0 = Pull Down (DEFAULT) 1 = Pull Up
		GPIO3_DS																	**GPIO3JD2 Driving Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		GPIO3_OE																	**GPIO3JD2 Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1A	GPIO12_CTRL	GPIO2_PS																	**GPIO2JD1 Pull Select** (Need to enable GPIO2_PE) 0 = Pull Down (DEFAULT) 1 = Pull Up
		GPIO2_DS																	**GPIO2JD1 Driving Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		GPIO2_PE																	**GPIO2JD1 Pull Enable Control** 0 = Enable (DEFAULT) 1 = Disable

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		GPIO2_OE																	**GPIO2JD1 Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		GPIO1POL																	**GPIO1 Polarity Inversion Control** 0 = Non-inverted (DEFAULT) 1 = Inverted
		GPIO1SEL																	**CSB/GPIO1 Function Select** 000 = Input / Output set to logic 0 (DEFAULT) 001 = Jack status from the AND/OR logic 010 = OTP output bit 011 = DAC auto mute condition (logic 1 = one or both DACs auto muted) 100 = Output divided FLL clock or MCLK 101 = FLL locked condition (logic 1 = PLL locked) 110 = Short frame sync detection output 111 = Output set to logic 1
		GPIO1_PS																	**GPIO1CSB Pull Control** (Need to enable GPIO1_PE) 0 = Pull down (DEFAULT) 1 = Pull up
		GPIO1_DS																	**GPIO1 Driving Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		GPIO1_PE																	**GPIO1CSB Pull Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		GPIO1_OE																	**GPIO1CSB Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	**0x0000**
1B	TDM_CTRL	TDM																	**TDM Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PCM_OFFSET_MODE_CTRL																	**PCM Offset In TDM Enable Control** 0 = Non-inverted (DEFAULT) 1 = Inverted
		DAC_LEFT_SEL																	**DAC Left Channel Source Under TDM Mode (TDM = 1 & PCM_OFFSET_MODE_CTRL = 0)** I2S: 00 = Slot 0 of right (DEFAULT) 01 = Slot 1 of right 10 = RESERVED 11 = RESERVED PCM: 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3
		DAC_RIGHT_SEL																	**DAC Right Channel Source Under TDM Mode (TDM = 1 & PCM_OFFSET_MODE_CTRL = 0)** I2S: 00 = Slot 0 of right (DEFAULT) 01 = Slot 1 of right 10 = RESERVED 11 = RESERVED PCM: 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3
		ADC_TX_SEL																	**ADC Data Source Under TDM/I2S Mode** 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1C	I2S_PCM_CTRL1	DACCM0																	**DAC Companding Mode Select** 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding
		ADCCM0																	**ADC Companding Mode Select** 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding
		ADDAP0																	**ADC Output Data Stream Directly Routed To DAC Input Data Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CMB8_0																	**8-bit Word For Companding Mode Of Operation Enable Control** 0 = Normal operation (DEFAULT - No companding) 1 = 8-bit operation for companding mode
		UA_OFFSET																	**uLaw Offset Select** 0 = 1's complement (DEFAULT) 1 = 2's complement
		BCP0																	**Bit Clock Phase Inversion Option For BCLK** 0 = Non-inverted (DEFAULT) 1 = Inverted
		LRP0																	**PCMA & PCMB Left-right Word Ordering Select** 0 = Right Justified/Left Justified/I2S/PCMA mode (DEFAULT) 1 = PCMB Mode Enable - MSB is valid on 1st rising edge of BCLK after rising edge of FS
		DACPHS0																	**DAC Audio Data Left-Right Ordering** 0 = Left DAC data in left phase of LRP (DEFAULT) 1 = Left DAC data in right phase of LRP (left-right reversed)
		ADCPHS0																	**ADC Audio Data Left-Right Ordering** 0 = Left ADC data in left phase of LRP (DEFAULT) 1 = Left ADC data in right phase of LRP (left-right reversed)
		WLEN0																	**Word Length of Audio Data Stream Select** 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length (DEFAULT) 11 = 32-bit word length
		AIFMT0																	**Audio Interface Data Format Select** 00 = Right justified 01 = Left justified 10 = Standard I2S format 11 = PCMA or PCMB audio data format option (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	**0x000B**
1D	I2S_PCM_CTRL2	I2S_TRI																	**I2S Tri State Enable Control** 0 = Normal mode 1 = Output high Z (DEFAULT)
		I2S_DRV																	**I2S Drive Enable Control** 0 = Normal mode (DEFAULT) 1 = Always out
		LRC_DIV																	**LRC(FS) Divider From BCLK Frequency** 00 = 1/256 (DEFAULT) 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS_EN0																	**PCM Time Slot Function Enable Control** (Only PCM_A_MODE or PCM_B_MODE can be used when PCM Mode is selected.) 0 = Disable time slot function for PCM mode (DEFAULT) 1 = Enable time slot function for PCM mode

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		TRI0																	**Without TDM Mode** 0 = Drive the full clock of LSB (DEFAULT) 1 = Tristate the 2nd half of LSB
		PCM8BIT0																	**8-Bit PCM Select** 0 = Use Error! Reference source not found.**WLEN** to select word length (DEFAULT) 1 = PCM select 8-bit word length
		PCM_TS_SEL																	**RESERVED**
		ADCDAT0_PE																	**ADCDAT IO Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADCDAT0_PS																	**ADCDAT IO Pull Up/Down Enable Control** 0 = Pull down (DEFAULT) 1 = Pull up
		ADCDAT0_OE																	**ADCDAT IO Output Enable Control** 0 = ADCDAT output DATA (when no data out, ADCOUT pin becomes high.) 1 = ADCDAT output buffer, always output DATA (DEFAULT)
		MS0																	**Master/Slave Mode Enable Control** 0 = Slave mode (DEFAULT) 1 = Master mode
		BCLK_DIV																	**BCLK Divider From MCLK Frequency** 000 = 1/2 (DEFAULT) 001 = 1/4 010 = 1/8 011 = 1/16 100 = 1/32 101 = 1/64
		DEFAULT	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x8010**
1E	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	**Triggers Short Frame Sync Signal Select** (If frame sync is less than) 00 = 252 x MCLK (DEFAULT) 01 = 253 x MCLK 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	**Short Gram Sync Detection Logic Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		TSLOT_L0																	**Left channel PCM Time Slot Start Value / PCM TDM Offset Mode Slot Start Value**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
1F	RIGHT_TIME_SLOT	TSLOT_R0																	**Right channel PCM Time Slot Start Value / unused for PCM TDM Offset Mode**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
20	BIQ_CTRL	BIQ_WRT_EN																	**Bi-Quad Parameter Write/Updated Enable Control** (Valid only when change from 0 to 1) 0 = Disable (DEFAULT) 1 = Enable **To program BIQ parameters for ADC or DAC path, follow these steps:** **(**1) Write Reg0x20 with Bit[4] = 0, Bit[0] for BIQ path (2) Write Reg0x21~0x2A as needed (3) Write Reg0x20 with Bit[4] = 1, Bit[1] for Sync Select, Bit[0] for BIQ path **To read back BIQ parameters for ADC or DAC, follow these steps:** (1) Write Reg 0x20 with Bit[4] = 0, and Bit[0] for BIQ path wants to read back (2) Read Reg 0x21~0x2A
		DAC_PATH_EN																	**Bi-Quad DAC Path Enable Control** (Read-only) 0 = Disable (DEFAULT) 1 = Enable

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		ADC_PATH_EN																	**Bi-Quad ADC Path Enable Control** (Read-only) 0 = Disable (DEFAULT) 1 = Enable
		BIQ_COF_SE																	**Bi-Quad Parameter Updated Sync Select** 0 = Sync with FS (DEFAULT) 1 = No sync
		BIQ_PATH_SE																	**Bi-Quad Path Select** 0 = For ADC (DEFAULT) 1 = For DAC
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
21	BIQ_COF1	BIQ_A1_L																	**Program BIQ_A1 Parameter Bit[15:0]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
22	BIQ_COF2	BIQ_A1_H																	**Program BIQ_A1 Parameter Bit[18:16]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
23	BIQ_COF3	BIQ_A2_L																	**Program BIQ_A2 Parameter Bit[15:0]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
24	BIQ_COF4	BIQ_A2_H																	**Program BIQ_A2 Parameter Bit[18:16]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
25	BIQ_COF5	BIQ_B0_L																	**Program BIQ_B0 Parameter Bit[15:0]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
26	BIQ_COF6	BIQ_B0_H																	**Program BIQ_B0 Parameter Bit[18:16]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
27	BIQ_COF7	BIQ_B1_L																	**Program BIQ_B1 Parameter Bit[15:0]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
28	BIQ_COF8	BIQ_B1_H																	**Program BIQ_B1 Parameter Bit[18:16]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
29	BIQ_COF9	BIQ_B2_L																	**Program BIQ_B2 Parameter Bit[15:0]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
2A	BIQ_COF10	PATH_EN																	**BIQ0 ADC Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BIQ_B2_H																	**Program BIQ_B2 Parameter Bit[18:16]**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
2B	ADC_RATE	SMPL_RATE																	**Generating 2.048MKHz based on Sample Rates** 000 = 48K (DEFAULT) 001 = 32K 110 = 96K 111 = 192K
		SINC4																	**4th-Order SINC Filter Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		GAINCMP																	**RESERVED**
		ADC_RATE																	**ADC SINC Down Select** 00 = Down 32 (DEFAULT) 01 = Down 64 10 = Down 128 11 = Down 256
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x0010**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
2C	DAC_CTRL1	DISABLE_DEM																	**Dynamic Element Matching Disable Control** 0 = Disable (DEFAULT) 1 = Enable (to disable DEM control of RateConvert2 module)
		DEM_DLY_N																	**DAC Dynamic Element Matching Delay Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		CICCLP_OFF																	0 = (DEFAULT)
		CIC_GAIN_ADJ																	**Gain Adjustment** (Fine tunes the DAC output)
		DAC_RATE																	**DAC Oversample Rate Select** 000 = 64 001 = 256 (DEFAULT) 010 = 128 100 = 32
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	**0x0001**
2D	DAC_CTRL2	DEM_DITHER																	**First Order Dynamic Element Matching Dithering Select** (Set probability of first order DEM dithering.) (Step size is 1/16.) 0000 = No dithering (DEFAULT) 0001 = 1/16 0010 = 2/16 0011 = 3/16 0100 = 4/16 0101 = 5/16 0110 = 6/16 0111 = 7/16 1000 = 8/16 1001 = 9/16 1010 = 10/16 1011 = 11/16 1100 = 12/16 1101 = 13/16 1110 = 14/16 1111 = 15/16
		SDMOD_DITHER																	**Bit Numbers Of Dithering On SD Modulator** (Step size is 1bit.) 00000 = No dithering (DEFAULT) 00001 = 1 00010 = 2 00011 = 3 00100 = 4 00101 = 5 00110 = 6 00111 = 7 01000 = 8 01001 = 9 01010 = 10 01011 = 11 01100 = 12 01101 = 13 01110 = 14 01111 = 15
		DAC_STEP_SEL																	**DAC OUT Step Select** 0XX = Use Internal step (DEFAULT) 100 = Clock DAC 101 = Delay 1 cycles of MCLK 110 = Delay 2 cycles of MCLK 111 = Delay 3 cycles of MCLK
		DACPL																	**DAC DEM L Channel Output Polarity** 0 = Non-Inverted (DEFAULT) 1 = Inverted
		DACPR																	**DAC DEM R Channel Output Polarity** 0 = Non-Inverted (DEFAULT) 1 = Inverted
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
2F	DAC_ DGAIN_CTRL	I2S_TO_ DAC0_ST																	**I2S Channel to DAC CH0 Gain Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB ▼ 0x0F = -96dB 0x0E = Mute ▼ 0x00 = Mute (DEFAULT)
		I2S_TO_ DAC1_ST																	**I2S Channel to DAC CH1 Gain Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB ▼ 0x0F = -96dB 0x0E = Mute ▼ 0x00 = Mute (DEFAULT)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
30	ADC_ DGAIN_CTRL	ADC_TO_ DAC_ST0																	**ADC to DAC CH0 Sidetone Select** (Step size is 3dB.) 0x00 = Mute (DEFAULT) 0x01 = -42dB ▼ 0x0E = -3dB 0x0F = 0dB
		ADC_TO_ DAC_ST1																	**ADC to DAC CH1 Sidetone Select** (Step size is 3dB.) 0x00 = Mute (DEFAULT) 0x01 = -42dB ▼ 0x0E = -3dB 0x0F = 0dB
		DGAIN_ ADC																	**ADC Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x02 = -102.5dB 0x01 = -103dB 0x00 = Mute
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0x00CF**
31	MUTE_CTRL	PGA_SMUTE _STEP																	**Analog Attn Mute Step Select** 00 = 128 sample 01 = 32 sample (DEFAULT) 10 = 16 sample 11 = 1 sample
		DAC_ZC_UP _EN																	**DAC Zero Crossing Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		AMUTE_EN																	**Auto Mute Enable Control** (Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.) 0 = Disable (DEFAULT) 1 = Enable
		AMUTE_CTR L																	**Auto Mute Control** 0 = Both DAC channels must have 0 values for 1024 samples before AMUTE turns on (DEFAULT) 1 = Either Ch0 or Ch1 must have 1024 consecutive zero samples

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		SMUTE_EN																	**Soft Mute Enable Control** 0 = Gradually increase DAC volume to volume register setting (DEFAULT) 1 = Gradually lower DAC volume to zero
		SMUTE_CTRL																	**DAC Limiter Output Enable Control** 0 = (DEFAULT) 1 = (When soft mute is enabled, DAC limiter output is also muted to remove any DC offset produced by the audio processing block.)
		ADC_ ZC_UP_EN																	**ADC Zero Crossing Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADC_ SMUTE_EN																	**ADC Soft Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
32	HSVOL_CTRL	HSPGA_ MUTE_EN																	**Headphone Diver Manual Attn Enable Control** (With HSPGA_ATTN_EN and AMUTE_EN enabled) 0 = Disable (DEFAULT) 1 = Enable
		HSPGA_ MUTE_AUTO _MODE																	**Headphone Driver Auto Attn Enable Control** (With HSPGA_ATTN_AUTO_MODE and AMUTE_EN enabled) 0 = Disable (DEFAULT) 1 = Enable
		MUTE_ HSPGA0																	**Right Channel Headphone Driver Manual Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_ HSPGA1																	**Left Channel Headphone Driver Manual Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		HSPGA0_VOL																	**Left Channel Headphone Driver Volume Control** (Step size is -1dB.) 000000 = 0dB (DEFAULT) 000001 = -1dB ▼ 000010 = -53dB 110110 = -54dB
		HSPGA1_VOL																	**Right Channel Headphone Driver Volume Control** (Step size is -1dB.) 000000 = 0dB (DEFAULT) 000001 = -1dB ▼ 000010 = -53dB 110110 = -54dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
33	DACL_CTRL	DAC_MIXER																	**DAC Channel Data Mixing Control** Bit 15: 0 = Normal DAC Right Channel Out (DEFAULT) 1 = DAC Right Channel is ½(L+R) Bit 14: 0 = Normal DAC Left Channel Out (DEFAULT) 1 = DAC Left Channel is ½(L+R)
		DAC_CH_ SEL0																	**DAC Channel 0 Source Select** 0 = From I2S Left Channel 1 = From I2S Right Channel (DEFAULT)

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DGAINL_DAC																	**DAC Left Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x02 = -102.5dB 0x01 = -103dB 0x00 = Mute
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0x02CF**
34	**DACR_CTRL**	**DAC_CH_SEL1**																	**DAC Channel 1 Source Select** 0 = From I2S Left Channel (DEFAULT) 1 = From I2S Right Channel
		DGAINR_DAC																	**DAC Right Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x02 = -102.5dB 0x01 = -103dB 0x00 = Mute
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0x00CF**
38	**ADC_DRC_KNEE_IP12**	**DRC_ENA_ADC1**																	**DRC ADC Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_IP_ADC1																	**DRC ADC Knee Point 2 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_ADC1																	**DRC ADC Smooth Filter Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_IP_ADC1																	**DRC ADC Knee Point 1 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x1486**
39	**ADC_DRC_KNEE_IP34**	**DRC_KNEE4_IP_ADC1**																	**DRC ADC Knee Point 4 Select** (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_IP_ADC1																	**DRC ADC Knee Point 3 Select** (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DEFAULT	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12
3A	ADC_DRC_SLOPES	DRC_NG_SLP_ADC1																	**DRC ADC Noise Gate Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_ADC1																	**DRC ADC Expansion Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = RESERVED
		DRC_CMP2_SLP_ADC1																	**DRC ADC Compressor Slope (Lower Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_ADC1																	**DRC ADC Compressor Slope (Higher Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_ADC1																	**DRC ADC Limiter Slope** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (DEFAULT)
		DEFAULT	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0x25FF
3B	ADC_DRC_ATKDCY	DRC_PK_COEF1_ADC1																	**DRC ADC Peak Detection Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1001= 511*Ts
		DRC_PK_COEF2_ADC1																	**DRC ADC Peak Detection Release Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts (DEFAULT) 0110 = 4095*Ts 0111 = 8191*Ts 1001= 16383*Ts
		DRC_ATK_ADC1																	**DRC ADC Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADC1																	**DRC ADC Decay Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 =4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		DEFAULT	0	0	1	1	0	1	0	0	0	1	0	1	1	1	0	1	0x3457
45	DAC_DRC_KNEE_IP12	DRC_ENA_DAC																	**DRC DAC Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DRC_KNEE2_IP_DAC																	**DRC DAC Knee Point 2 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x1E = -62dB 0x1F = -63dB
		DRC_SMTH_ENA_DAC																	**DRC DAC Smooth Filter Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_IP_DAC																	**DRC DAC Knee Point 1 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x1486**
46	**DAC_DRC_KNEE_IP34**	DRC_KNEE4_IP_DAC																	**DRC DAC Knee Point 4 Select** (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_IP_DAC																	**DRC DAC Knee Point 3 Select** (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0x0F12**
47	**DAC_DRC_SLOPES**	DRC_NG_SLP_DAC																	**DRC DAC Noise Gate Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_DAC																	**DRC DAC Expansion Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_CMP2_SLP_DAC																	**DRC DAC Compressor Slope (Lower Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_DAC																	**DRC DAC Compressor Slope (Higher Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_DAC																	**DRC DAC Limiter Slope** 000 = 0 001 = 1:2 (DEFAULT) 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1
		DEFAULT	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0x25F9**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
48	DAC_DRC_ATKDCY	DRC_PK_COEF1_DAC																	**DRC DAC Peak Detection Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1XXX = RESERVED
		DRC_PK_COEF2_DAC																	**DRC DAC Peak Detection Release Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts (DEFAULT) 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1XXX = RESERVED
		DRC_ATK_DAC																	**DRC DAC Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_DAC																	**DRC DAC Decay Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 =32757*Ts 1010 = 65535*Ts
		DEFAULT	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1	**0x3457**
4C	MODE_CTRL	DACIN_SRC																	**DAC Filter Input Source Select** 000 = From DAC bi-quad output (DEFAULT) 001 = From DRC DAC output 010 = From DAC mixer output 011 = From Built-in sin generator 100 = From μ-Law or A-Law decode output
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
50	CLASSG_CTRL	CLASSG_CLK_SRC																	**Class G Function Clock Divider Select** 00 = Clock 2MHz (DEFAULT) 01 = 1/3 MCLK 10 = MCLK 11 = Disable CLK (disable charge pump)
		CLASSG_TIMER																	**Class G Timer Select** (Define time for supplies go to +-0.9 after a Class G signal goes lower than threshold voltage.) 000000 = (DEFAULT) 000001 = 1 ms 000010 = 2 ms 000100 = 8 ms 001000 = 16 ms 010000 = 32 ms 100000 = 64 ms
		CLASSG_THRSLD																	**Class G Threshold Select** (Threshold for DAC signal level comparison for Class G supplies: Below threshold ± .9 or above ± 1.8 Volt. 1 full scale=1 Vrms) 00 = 1/16 full scale (DEFAULT) 01 = 1/8 full scale 10 = 3/16 full scale 11 = 1/4 full scale

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		CLASSG_CMP_EN																	**Class G Compare Path Enable Control** (Each Bit enables according DAC path. If CLASSG_EN=1, and CLASSG_CMP_EN=00, supplies stay at ± .9) 0 = Disable (DEFAULT) 1 = Enable Bit 0 = Left DAC Bit 1 = Right DAC
		CLASSG_EN																	**Class G Function Enable Control** (±0.9 Volt supply option) 0 = Disable (DEFAULT- only provide ±1.8V) 1 = Enable (supplies are either =-1.8 or +-0.9 depend on signal amplitudes, see CLASSG_CMP_EN)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
51	**OPT_EFUSE_CTRL**	**STANDBY_IN**																	**OTP Stand By Status Register Control** 0 = OTP standby (DEFAULT) 1 = OTP in operation mode
		NR_IN																	**OTP Normal Read Mode Status Register Control** 0 = Standby mode (DEFAULT) 1 = Normal read mode
		PGEN_IN																	**OTP Program Mode Status Register Control** Active Low 0 = Enable (DEFAULT) 1 = Disable
		STROBE_IN																	**OTP Strobe Signal Status Register Control** 0 = Disable (DEFAULT) 1 = Enable
		WL_BIN																	**eFuse Determiner Bit** (Determines which bit to read or write to on the eFuse)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
55	**MISC_CTRL**	**SPIEN**																	**I2C/SPI Select** 0 = Enable I2C (DEFAULT) 1 = Enable SPI
		RAM_TEST_START																	**RAM Test Control** 0 = Disable (DEFAULT) 1 = Enable
		D2A_LOOP																	**ADC To DAC Loop** 0 = Disable (DEFAULT) 1 = Enable (use ADC decimation filter output as DAC left filter input)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
58	**I2C_DEVICE_ID**	**I2C_DEVICE_ID1**																	**I2C Device ID Read In**
		I2C_DEVICE_ID2																	**I2C Device ID LSB Read In** (Set by GPIO1/CSB pin)
		GPIO2JD1																	**Jack Detect 1 GPIO2 Status** 0 = Inserted (DEFAULT) 1 = Ejected
		GPIO3JD2																	**Jack Detect 2 GPIO3 Status** (For WLCSP package only)
		JKDETL																	**Jack Tip Insertion Detect Status** (For WLCSP package only)
		SILICON REVISION ID																	**Silicon Revision ID**
		SOFTWARE ID																	**Software ID** 00 = NAU88L25B
		DEFAULT	**X**	**0**	**0**	**1**	**1**	**0**	**1**	**X**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**READ ONLY 0x1A14**
59	**SARDOUT_RAM_STATUS**	**RATM_TEST_FINISH**																	**RAM Test Status Bit** 0 = Test not finished (DEFAULT) 1 = Test finished

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		RAM_TEST_FAIL																	**RAM Test Result Bit** 0 = Test passed (DEFAULT) 1 = Test failed
		ANALOG_MUTE																	**Analog Mute Flag Bit** 0 = Disable (DEFAULT) 1 = Enable
		SARADC_DOUT																	**SAR ADC Read Out**
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**READ ONLY 0x00FF**
66	BIAS_ADJ	RESERVED																	**RESERVED**
		MUTEL																	**PGA Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	**RESERVED**
		TESTDAC																	**DAC Right, Left Test Only**
		RESERVED																	**RESERVED**
		VMIDEN																	**VMID Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		VMIDSEL																	**VMID Tie-off Impedance Select** 00 = Open (DEFAULT) 10 = 125KOhms 01 = 25KOhms 11 = 2.5KOhms
		RESERVED																	**RESERVED**
		RESERVED																	**RESERVED**
		BIASADJ																	**PGA Master Bias Current Power Select** 00 = Normal operation (DEFAULT) 01 = 9% reduced bias current from normal 10 = 17% reduced bias current from normal 11 = 11% increased bias current from normal
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
68	TRIM_SETTINGS	RESERVED																	**RESERVED**
69	ANALOG_CONTROL_1	TESTDACIN																	**DAC Test Signal** 00 & 11 = GND (DEFAULT) 01 & 10 = High & Low
		PULLUP_GPIO3																	**GPIO3JD2 Pull Up Select** 0 = 1MOhm (DEFAULT) 1 = 100KOhm (For WLCSP package only)
		GPIO3THL																	**GPIO3 JKDET2 Threshold Low Select** (For WLCSP package only) 00 = 0.22 x VDDA (DEFAULT) 10 = 0.40 x VDDA 11 = 0.5 x VDDA
		GPIO3THH																	**GPIO3 JKDET2 Threshold High Select** (For WLCSP package only) 00 = 0.85 x VDDA (DEFAULT) 10 = 0.78 x VDDA 11 = 0.6 x VDDA
		PULLUP_GPIO2																	**GPIO2JD1 Pull Up Select** 0 = 1MOhms (DEFAULT) 1 = 100KOhms
		GPIO2THL																	**GPIO2 JKDET1 Threshold Low Select** 00 = 0.22 x VDDA (DEFAULT) 10 = 0.40 x VDDA 11 = 0.5 x VDDA
		GPIO2THH																	**GPIO2 JKDET1 Threshold High Select** 00 = 0.85 x VDDA (DEFAULT) 10 = 0.78 x VDDA 11 = 0.6 x VDDA
		RESERVED																	**RESERVED**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		JD1POL																	**JKDETL JD1 Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted (For WLCSP package only)
		JKDETLPOL																	**JKDETL Output Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted (For WLCSP package only)
		ENJKDETL																	**Enable Jack Tip Insertion Detection Circuit** (For WLCSP package only)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
6A	ANALOG_ CONTROL_2	ANALOG_ CONTROL																	**Headphone Driver Class-AB Bias Current Adjust In Non-Class-G Mode** 0 = Normal (DEFAULT) 1 = 2x
																			Headphone Driver Bias Current Adjust In Class-G Mode 0 = Normal (DEFAULT) 1 = 0.5x
																			Headphone Driver Bias Current Adjust In non-Class-G Mode 0 = Normal (DEFAULT) 1 = 2.5x
																			Headphone Out Boost Driver Bias Current Adjust in Class-G Mode 1 0 = Normal (DEFAULT) 1 = Low
																			Headphone Out Boost Driver Bias Current Adjust in Class-G Mode 2 0 = Normal (DEFAULT) 1 = Low
		AB_ADJ																	**Headphone Driver Bias Adjust In Class-AB** 0 = Normal (DEFAULT) 1 = Increase bias
		RESERVED																	**RESERVED**
		MUTEMICP																	**MUTE MICP Input to PGA** 0 = Unmute (DEFAULT) 1 = Mute
		MUTEMICN																	**MUTE MICN Input to PGA** 0 = Unmute (DEFAULT) 1 = Mute
		CAPMSB																	**DAC Reference Decoupling Capacitor Enable MSB**
		CAPLSB																	**DAC Reference Decoupling Capacitor Enable LSB**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
71	ANALOG_ADC_1	RESERVED																	**RESERVED**
		RESETL																	**Integrators in ADC Reset Control** 0 = No action (DEFAULT) 1 = Reset
		RESERVED																	**RESERVED**
		CHOP ENABLE																	**ADC Chopper First Integrator Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CHOPPHASE																	**ADC Chopper Phase Enable Control** (If chopper is disabled, this can be used to change the phase of the chopper switches. It helps determine the offset of the first integrator of the ADCs) 0 = Normal operation (DEFAULT) 1 = Change phase
		CHOP RESETN																	**ADC Chopper Reset Control** 0 = No action (DEFAULT) 1 = Reset
		CHOPFIXED																	**ADC Chopper Frequency** 0 = Dither chopper frequency (DEFAULT) 1 = Fixed chopper frequency

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		CHOPORDER																	**ADC Chopper Dither Order** (To choose the order of dithering chopper frequency) 0 = First order dither 1 = Second order dither (DEFAULT)
		CHOPF																	**ADC Fixed Chopper Frequency Select** (Only effective in fixed frequency mode) 00 = OSR*Fs/2 01 = OSR*Fs/4 (DEFAULT) 10 = OSR*Fs/8 11 = OSR*Fs/16
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**0x0011**
72	ANALOG_ADC_2	RESERVED																	**RESERVED**
		ADC_UPL																	**PGA Bias Current Increase Enable Control** (For driving the ADC at high sample rates) 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	**RESERVED**
		BIAS																	**ADC Bias Current Select** 00 = Nominal (DEFAULT) 01 = Double 10 = Half 11 = Quarter
		VREFSEL																	**ADC Bias Current Select** 00 = Nominal (DEFAULT) 01 = Double 10 = Half 11 = Quarter
		RESERVED																	**RESERVED**
		PDNOTL																	**ADC Analog Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		LFSRRESETN																	**DEM Algorithm LFSR Reset Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	**0x0020**
73	RDAC	FS_BCLK_ENB																	**FS/BCLK Output Driving Enable Control** (Work with MS0) 1 = Disable 0 = Enable
		DAC_EN																	**DAC Enable Control** 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left DAC Bit1 = Right DAC
		CLK_DAC_EN																	**DAC Clock Enable Control** 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left DAC Bit1 = Right DAC
		FC_CTR																	**DAC Smoothing Filter On HS Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_DELAY																	**DAC Clock Delay Setting** 000 = Delay 0 nsec (DEFAULT) 100 = Delay 4 nsec 001 = Delay 1 nsec 101 = Delay -3 nsec 010 = Delay 2 nsec (Recommended) 110 = Delay -2 nsec 011 = Delay 3 nsec 111 = Delay -1 nsec

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DACVREFSEL																	**DAC Full Scale Reference Voltage Select** (By setting this value, it will change DAC full scale output. For best performance, use default value.) 00 = External VDDA 01 = 1.5V 10 = 1.6V (DEFAULT) 11 = 1.7V
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0x0008**
74	MIC_BIAS	INT2KB																	**MICBIAS1 Internal 2K Ohm Resistor For JKSLV Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		INT2KA																	**MICBIAS1 Internal 2K Ohm Resistor For JKR2 Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		LOWNOISE																	**Low Power / Low Noise Mode Select** 0 = Low power mode (DEFAULT) 1 = Low noise mode
		POWERUP																	**MICBIAS1 Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		NOCAP																	**Low Noise Mode Capacitance Settings** 0 = 2.2µF or 4.7µF on MICBIAS1 output (DEFAULT) 1 = No capacitance on MICBIAS1 output
		MICBIASLVL1																	**MICBIAS1 Output Level Select** 000 = VDDA (DEFAULT) 001 = 1x 010 = 1.1x 011 = 1.2x 100 = 1.3x 101 = 1.4x 110 = 1.53x 111 = 1.53x
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x0006**
76	BOOST	CLR_APR_EMRGNCY_SHTDWN																	**Clear Headset Short Circuit Shutdown IRQ** 0 = (DEFAULT) 1 = Reset (Momentary)
		STG2_SEL																	**PGA In Class-A Mode Of Operation Enable Instead Of Class-AB Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PDVMDFST																	**VMID Pre-charge Disable Control** 0 = Disable (DEFAULT) 1 = Enable
		BIASEN																	**Global Analog Bias Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DISCHRG																	**Charge Input Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BYPS_IBCTR																	**Bypass PGA Current Control Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BOOSTDIS																	**HP Boost Driver Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		BOOSTGDIS																	**HP Boost Driver In Class-G Mode Disable Control** 0 = Enable (DEFAULT) 1 = Disable

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		SHRT_SHTDWN_DIG_EN																	**Short Circuit Shutdown Digital Domain Enable Control** 0 = Disable (DEFAULT – APR_EMRGNCY_SHTDWN interrupt should be manually cleared by 0x76[15] CLR_APR_EMRGNCY_SHTDWN.) 1 = Enable (APR_EMRGNCY_SHTDWN interrupt can be automatically cleared 1 msec after shortage detected.)
		EN_SHRT_SHTDWN																	**Automatic Short-circuit Shutdown Enable Control** 0 = Disable (DEFAULT – APR_EMRGNCY_SHTDWN interrupt is generated within 16.3 µsec debounce when shortage detected.) 1 = Enable (Headset driver power will be down immediately when shortage detected. No interrupt will be generated.)
		HS_SHRT_THRESHLD																	**Headset Short Circuit Protection Limit** 00= 115mA at +FS (DEFAULT) 11= 155mA at +FS
		PAMP_THRSHLD																	**Adjust HS Boost P-driver Bias Current** 00 = Normal (DEFAULT) 11 = Decrease current
		NAMP_THRSHLD																	**Adjust HS Boost N-driver Bias Current** 00 = Normal (DEFAULT) 11 = Decrease current
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
77	FEPGA	ACDC_CTRL																	**Input Pin DC State Enable Control** (Effective when DISCHRG = 1) 0 = Disable (DEFAULT) 1 = Enable Bit0 = Charges MICP to VREF Bit1 = Charges MICN to VREF
		CMLCK_ADJ																	**PGA Common Mode Threshold Lock Adjust** 00 = (DEFAULT)
		IB_LOOP_CTR																	**PGA Current Trim** 0 = (DEFAULT)
		IBCTR_CODE																	**PGA Current Trim** 000 = (DEFAULT)
		RESERVED																	**RESERVED**
		FEPGA_MODEL																	**FEPGA Mode Select** 0 = Disable (DEFAULT) 1 = Enable MODE[0] = Anti-aliasing filter adjust MODE[1] = Disconnects MICP & MICN MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
7F	POWER_UP_CONTROL	PUFEPGA																	**FEPGA Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		FEPGA_GAIN																	**Right PGA Gain Control** (Step size is 1dB.) 0x00 = -1dB (DEFAULT) 0x01 = 0dB ▼ 0x24 = 35dB 0x25 = 36dB

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		PUP_INTEG																	**Output Integrator Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left HP driver Bit1 = Right HP driver
		PUP_DRV_INSTG																	**Output Driver Power Enable Control** (To reduce pop noise, turn on this first, then turn on PUP_MAIN_DRV.) 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left HP driver Bit1 = Right HP driver
		PUP_MAIN_DRV																	**Main Driver Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left HP driver Bit1 = Right HP driver
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
80	CHARGE_PUMP_AND_POWER_DOWN_CONTRL	RESERVED																	**RESERVED**
		BCLK_DS																	**BCLK IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		FS_DS																	**FS IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		ADCDAT_DS																	**ADCDAT IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		SDA_DS																	**SDA IO Drive Strength Control** 0 = Normal 1 = Stronger (DEFAULT)
		JAMNODCW																	**RESERVED**
		PDB_DAC																	**DAC Right / Left Power Down Bar Enable Control** 00 = Disable 11 = Enable (DEFAULT)
		JAMFORCE2																	**Register Output Force 1 Control** (Charge pump clock to not slow) 0 = Disable (DEFAULT) 1 = Enable
		JAMFORCE1																	**Register Output Force 2 Control** (Charge pump clock to not slow) 0 = Disable (DEFAULT) 1 = Enable
		RNIN																	**Charge Pump Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PRECHARGE																	**VPOS Pre-charge Enable Control** **(For faster startup)** 0 = Disable (DEFAULT) 1 = Enable
		DISCHARGE VEE																	**VEE Pad Discharge Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DISCHARGE VPOS																	**VPOS Pad Discharge Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SHCIRSEL2																	**Charge Up Current Limit 2** 0 = Low (DEFAULT) 1 = High
		SHCIRSEL1																	**Charge Up Current Limit 1** 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	**0x0B00**
81	CHARGE_PUMP_INPUT_READ	APR_EMRGNCY_SHTDWN																	**APR Emergency Short Circuit Shutdown IRQ**

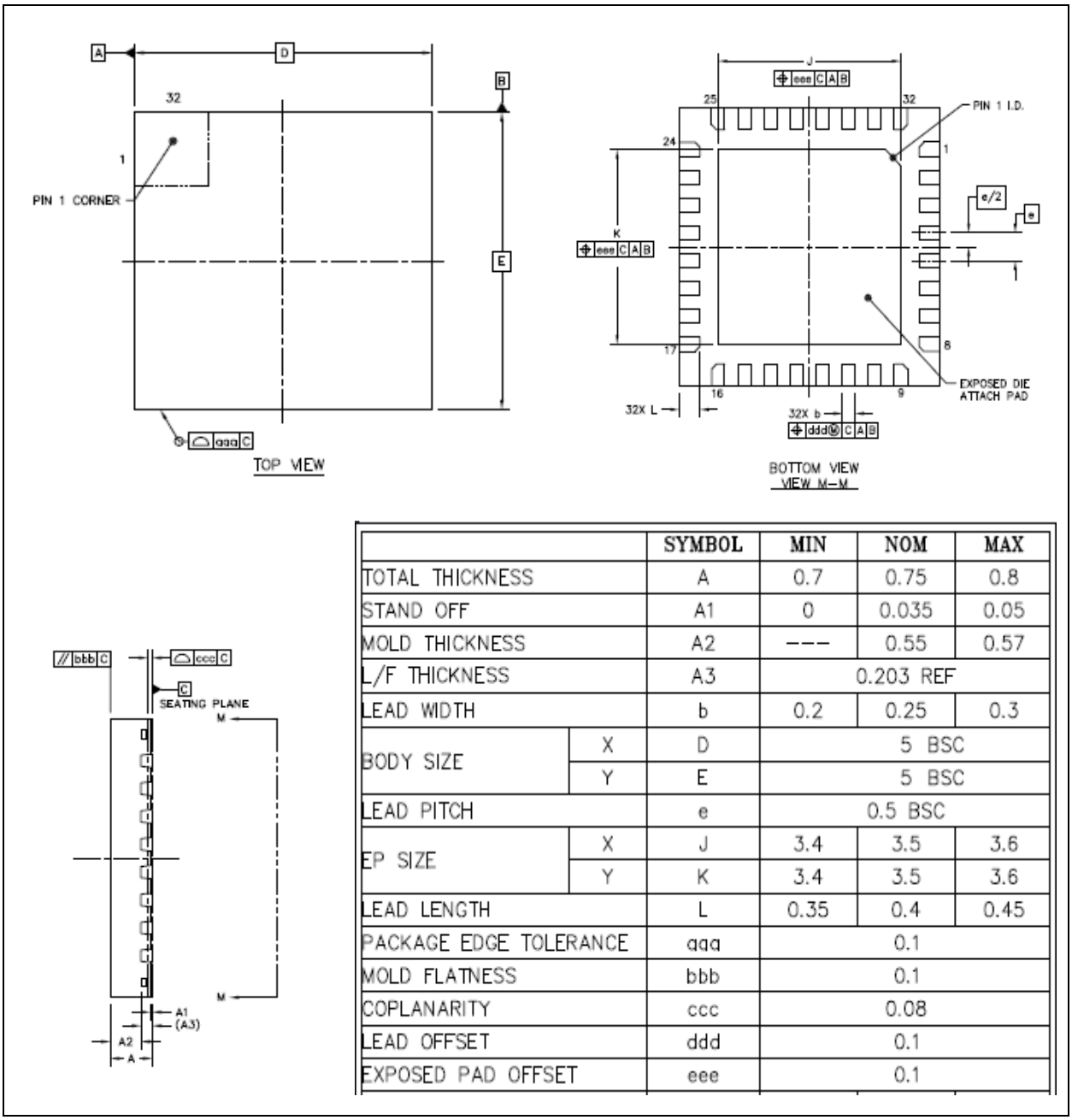
REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		MODE1BUF																	**Monitor MODE1 State Of Charge Pump Block**
		NODCBUF																	**Monitor Charge Pump Drawing DC Current** 0 = Drawing 1 = Not drawing (DEFAULT)
		RN2BUF																	**Monitor Charge Pump Enable Status** 0 = Off (DEFAULT) 1 = On
		VPOSOK																	**Monitor High Voltage Status Of VPOS** 0 = Possible short circuit (DEFAULT) 1 = Max output (Normal operation)
		VCOMPBUF																	**Monitor Low Voltage & Low Current Status Of Charge Pump** 0 = No current 1 = With current (DEFAULT)
		FORCE1BUF																	**Monitor Charge Pump Frequency Status** 0 = Normal 1 = Max frequency (DEFAULT)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**READ ONLY 0x0013**
82	GENERAL_ STATUS	OUT2_OUT																	**OUT2 After Headset Detection (JKSLV)**
		OUT1_OUT																	**OUT1 After Headset Detection (JKR2)**
		OUT2																	**OUT2 From Analog**
		OUT1																	**OUT1 From Analog**
		JK_EJECT_ INTR																	**JACK Ejection Interrupt**
		JK_INSERT_ INTR																	**JACK Insertion Interrupt**
		JKDET_ON																	**Pre-debounce JACK Status**
		JKDETL																	**JKDETL** (For WLCSP package)
		GPIO4_IN																	**GPIO4 Input** (For WLCSP package)
		GPIO3_IN																	**GPIO3 Input** (For WLCSP package)
		GPIO2_IN																	**GPIO2 Input Pin Status** (same as **I2C_DEVICE_ID** REG0X58[7])
		GPIO1_IN																	**GPIO1 Input**
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**READ ONLY 0x0020**

15 Package Dimensions

The NAU88L25B Audio CODEC is available in a 32-Lead QFN package, as shown in **Figure 56** or a 42-Ball WLCSP package, as shown in **Figure 57**.

15.1 QFN 32-Lead Package

QFN32L 5X5 mm^2, Thickness 0.8 mm (Max) , Pitch 0.5 mm (Saw Type) EP SIZE 3.5 X 3.5 mm.

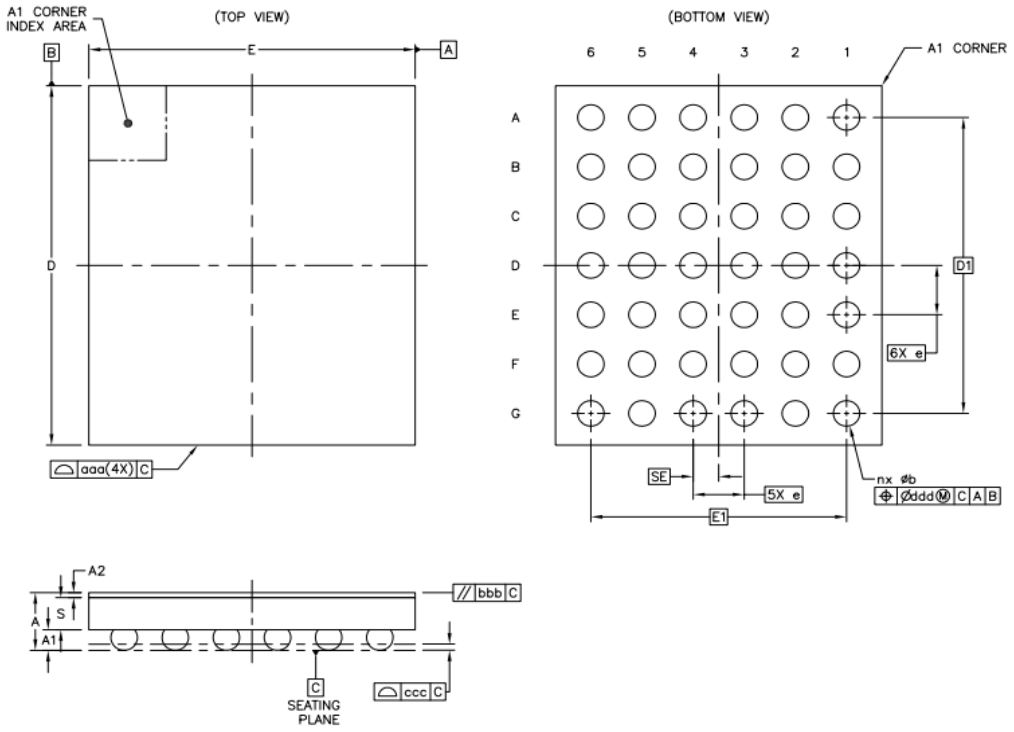


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 56 QFN 32-Lead Package

15.2 WLCSP 42-Ball Package

WLCSP 42-Balls package, 2.552 x 2.915 mm, with 0.4 mm Pitch.

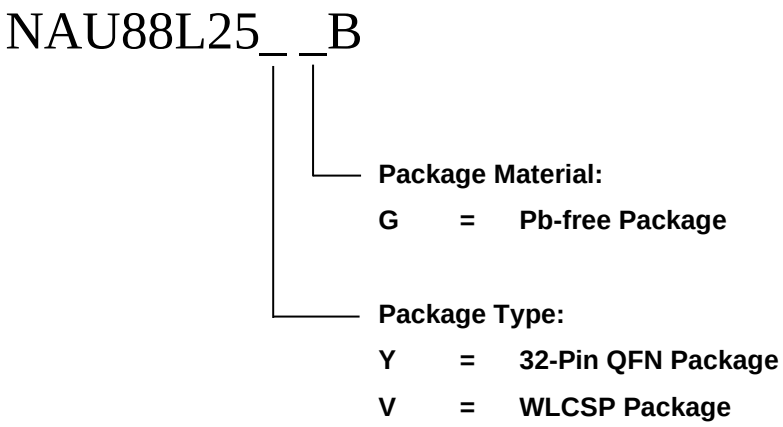


		SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS		A	0.467 ± 0.059
WAFER THICKNESS		S	0.26 ± 0.025
STAND OFF		A1	0.137 ~ 0.197
FILM THICKNESS		A2	0.04 ± 0.004
BODY SIZE	X	E	2.552
	Y	D	2.915
BALL/BUMP PITCH	X	SE	0.2 BSC
	Y	SD	--- BSC
EDGE BALL CENTER TO CENTER	X	E1	2 BSC
	Y	D1	2.4 BSC
PITCH		e	0.4 BSC
BALL DIAMETER (SIZE)			0.2
BALL/BUMP WIDTH		b	0.178 ~ 0.238
BALL/BUMP COUNT		n	42
PACKAGE EDGE TOLERANCE		aaa	0.03
WAFER FLATNESS		bbb	0.06
COPLANARITY		ccc	0.05
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015

Figure 57 WLCSP 42-Ball Package

16 Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L25YGB	5x5 mm	QFN-32	Green
NAU88L25VGB	2.552x2.915mm	42 Balls WLCSP	Green



17 Revision History

Version			Description
#	Date	Page(s)	
0.1	October 13, 2015	57,68,74, 77,79	Changes from orignal chip
		74-79	Added Reg0x2
			Added Reg0x2D[3:2], and Reg0x73[15]
			Changed Reg0x58[2]; changed descriptions for Reg0X80[9:8]. Reserved Reg0x80[11]
0.2	October 16, 2015	85-86	Updated and added Application Diagram.
		88	Added WLCSP package information.
0.3	October 27, 2015	90	Updated QFN package information
0.4	November 13, 2015	8	Added WLCSP package dimensions.
		12	I(VDDA) when VDDC=1.2 added.
		13	Updated Ground switch resistance.
		36	Figure 10 SYSTEM_SRC added.
0.5	December 14, 2015	89	Note added for application diagram.
		48-51	Added 8.7 Audio Timing Diagram section.
0.6	January 18, 2016	69	Reg0X3[13] description added.
		74	Reg0X13 SAR_TRACKGAIN added.
		71	Reg0x8 register default setting changed.
		81	Reg0x32 MUTE_HSPGA0/A1 swapped.
		13	Added Crosstalk and Switch Impedence When Enabled data for WLCSP
0.7	March 8, 2016	43-44	SPI 4-wire description added.
		93,94	Typical application circuit diagram updated.
2.0	August 19, 2016	All	Content sequence and format changes, edits for grammar and clarity. Color removed from graphics.
		12	1.3.1 and Figure 1 USB Headphone application added for use with NUC123 microprocessor. Reference diagram added.
		14	Figure 3 Revised Audio Jack Application with WLCSP package diagram.
		22	Table 4 Operating Conditions: QFN Package: Junction to Ambient and Junction to Case Temperatures added.
		25	Table 7 Channel Crosstalk Left to Right value added for WLCSP package. Ground Switch ON Resistance value for WLCSP package added.
2.0	August 19, 2016	33	Chapter 7.1 Sigma Delta Modulator and Decimator descripton updated.

Version			Description
#	Date	Page(s)	
		40	8.2.1 Soft UnMute description added.
		56	Figure 23 Typical I2C Level Shifter Circuit Diagram replaced.
		75	13.2 Microphone Detection description updated.
		91	Reg6 GAIN ERR bit descriptions updated.
		112	Reg73 RDAC: Bit Descriptions corrected for DAC_EN and CLK_DAC_EN.
2.1	November 10, 2016	88-115	0x4[12:10] 0x6[15:12] 0x7[9:0] 0x8[15:12] 0x9[14:12] 0x1E[15:13] 0x66[9:8] 0x69[15:14] 0x80[10] 0x81[5] Register description enhancement
2.2	July 30, 2018	99	0x1D[2:0] value correct
		38	ADDAP0 need to turn on for DAC sidetone applicaiotn
		13	Add low pass filter at SCLK and SDIO
2.3	January 17, 2020	54	Enhance FLL app. note
2.4	August 30, 2021	69	Table 27, Table 28, secton 11.2.8
2.5	Sep 20, 2021	90	Table 28, secton 11.2.8, updated 0x3[9:8]
2.6	Feb 10, 2022	88-114	Updated Register Table Format
2.7	May 16, 2022	68	Updated Table 27, 28, I2S timing ; Note for testing probe; Updated 0x1D[2:0] BCLK_DIV descritpion
2.8	July 28, 2022	68 73 99	Updated Table 27, 28, I2S timing ; Note for Tdod testing conditoin; Humming noice preventive circuit description Updated 0x1D[4] ADCDAT0_OE and 0x1D[2:0] BCLK_DIV descritpion

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