ISD ARM® Cortex®-M4F SoC
ISD941A00 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The ISD941A00 series 32-bit microcontrollers are an embedded ARM® Cortex®-M4F core with DSP extensions and a Floating Point Unit which run up to 200 MHz. It provides up to 512 KB of flash memory and up to 192 KB of SRAM. It is ideal for consumer product applications which need communication interfaces and high computing power.

The ISD941A00 is also equipped with a variety of peripheral devices, such as Multi-Function Timers, Watchdog Timers, RTC, PDMA, UART, SPI, I^2C, PWM, GPIO, 12-bit ADC, USB1.1 Device, Low voltage reset and Brown-out Detector. In addition, it supports plenty of audio peripherals such as I^2S, DMIC, audio DPWM modulator and stereo audio codec.

The stereo audio codec supports both analog and digital audio functions. It includes one digital audio interface (I2S/PCM), one digital microphone interface, one digital mixer, two high quality DACs and ADCs, and one stereo capless headphone amplifier. The advanced on-chip signal processing engine that includes dynamic range compressor (DRC), programmable biquad filter, as well as an integrated frequency locked loop (FLL) to support various input clocks.

The ISD941A00 series is suitable for a wide range of applications such as:

- Audio Processing Platform
- Consumer Products
- Industrial Automation
- Home Automation
- Security Alarm System
- System Supervisors
- Gaming Controller
- Smart Remote Controller

2 FEATURES

2.1 Features

- Core
  - ARM® Cortex®-M4F core running up to 200 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Low Power Sleepmode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Supports Embedded Trace Macrocell
- Built-in LDO for wide operating voltage range
- Flash Memory
  - Up to 512 KB on-chip Application ROM (APROM)
  - Configurable program code/data allocation
  - 4 KB on-chip Flash for user-defined loader (LDROM)
  - Supports 2-wire ICP update through SWD/ICE interface
  - Supports In-system program (ISP), In application program (IAP) update
  - Supports 4 KB page erase for all embedded flash
  - Supports 4 KB two-way cache to reduce power consumption and improve performance.
  - Enhanced performance up to 3.4 Core Mark/MHz when running code in Flash with cache
  - Supports 2-wire ICP flash updating through SWD interface
  - Supports 32-bit/64-bit and multi-word flash programming function.
  - Supports fast flash programming verification by CRC function.
- SRAM
  - Up to 192 KB embedded SRAM
  - 32 KB SRAM in bank 0 that supports hardware parity check and retention mode
  - Supports byte-, half-word- and word-access
  - Supports exception (NMI) generated once a parity check error occurs
  - Supports PDMA mode
- Clock Control
  - Built-in 48.0 MHz or 49.152 MHz selectable internal high speed RC oscillator (HIRC) for system operation.
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation.
  - 4~24.576 MHz external high speed crystal oscillator (HXT) for precise timing operation.
  - 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation.
  - Supports one PLL up to 500 MHz for high performance system operation, sourced from HIRC or HXT.
  - Supports clock failure detection for high/low speed external crystal oscillator.
  - Supports exception (NMI) generation once a clock failure detected.
  - Supports clock output.
- GPIO
  - Supports four I/O modes:
    - Quasi bi-direction

- Push-Pull output
- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high slew driver and high sink current I/O (up to 20mA at 3.3V)
- Supports software selectable slew rate control
- Supports 5V tolerance function on subset of GPIO except analog I/O

- PDMA (Peripheral DMA)
  - Supports 16 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports stride function.
  - Channel 0, 1 supports time-out function for each channel.
  - Supports Basic and Scatter-Gather Transfer modes
  - Each channel supports circular buffer management using Scatter-Gather Transfer mode
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports single and burst transfer type
  - Supports source and destination address can be increment or fixed.
  - DMA transfer count up to 65536.
- Multi-Function Timer (MFT, Timer + PWM)
  - TIMER mode
    - Supports 4 sets of 32-bit timers with 24-bit up-timer and 8-bit prescale counter, 24-bit up counter value is readable.
    - Independent clock source for each timer
    - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
    - Supports event counting function to count the event from external pin
    - Supports input capture function to capture or reset counter value
    - Supports external capture pin event for interval measurement.
    - Supports external capture pin event to reset 24-bit up counter.
    - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
    - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and DMA.
    - Supports Inter-Timer trigger mode
  - PWM mode
    - Supports four 16-bit PWM counters with 10-bit dead time generator
    - Supports 12-bit pre-scale for PWM.
    - Supports independent mode for PWM output channel
    - Supports 8 channel PWM outputs in complementary mode
    - Supports mask function and tri-state enable for each PWM pin
    - Supports interrupt on the following events:
      - PWM counter match zero, period value or compared value
    - Supports trigger EADC on the following events:
      - PWM counter match zero, period value or compared value
- PWM
  - Supports independent PWM outputs with 16-bit resolution
  - Supports maximum clock frequency up to 200MHz
  - Supports 12-bit clock prescale
  - Supports dead time with maximum divided 12-bit prescale
  - Supports one-shot or auto-reload counter operation mode
  - Supports up, down or up-down PWM counter type
  - Supports synchronous function for phase control

- Supports counter synchronous start function
- Supports complementary mode for 3 complementary paired PWM output channel
- Supports brake function with auto recovery after brake condition removed
- Supports mask function and tri-state output for each PWM channel
- Supports trigger EADC to start conversion
- Supports up to 6 independent input capture channels with 16-bit resolution counter

- Watchdog Timer
  - 18-bit free running up counter for WDT time-out interval
  - Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
  - Configurable to force WDT enable after chip power-on or reset.
  - Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  - Window set by 6-bit counter with 11-bit prescale
  - WWDT counter suspends in Idle/Power-down mode
- RTC
  - Supports software compensation by setting frequency compensate register (FCR), compensated clock accuracy reaches ±5ppm within 5 seconds
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports Day of the Week counter
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports 1 Hz, clock output
  - Supports wake-up from idle mode, Power-down mode and Standby Power-down mode
  - Supports 32 kHz Oscillator gain control
  - Supports RTC Time Tick and Alarm Match interrupt
  - Support Time stamp
- UART
  - Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped
  - Support baud rate up to 12.5 MHz
  - Supports 16-byte FIFOs with programmable level trigger
  - Supports auto flow control (CTS and RTS)
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Programmable receiver FIFO trigger level
  - Supports wake-up function
  - Supports 8-bit receiver FIFO time-out detection function
  - Supports Auto-Baud Rate measurement and baud rate compensation function
  - Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function
  - Supports nCTS, incoming data, RX FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode.
  - Supports hardware or software enables to program nRTS pin to control RS-485

transmission direction
- Supports PDMA mode

- I²C
  - Supports up to two sets of I²C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Supports 10 bits mode
  - Support High speed mode 3.4Mbps
  - Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports SMBus and PMBus
  - Supports multi-address Power-down wake-up function
- I²S
  - Supports one I²S interface
  - Interface with external audio CODEC
  - Supports Master and Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Mono and stereo audio data
  - I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
  - PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
  - PCM protocol supports TDM multi-channel transmission in one audio sample, the number of data channels can be set as 2, 4, 6, or 8
  - Two 16-level FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- SPI / I²S
  - Supports two sets of SPI/ I2S controllers – SPI1/ SPI2
  - Supports Master or Slave mode operation
  - Supports two PDMA requests, one for transmitting and the other for receiving
  - SPI supports configurable bit length of a transfer word from 8 to 32-bit
  - SPI Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
  - SPI supports MSB first or LSB first transfer sequence
  - SPI supports the byte reorder function
  - SPI supports Byte or Word Suspend mode
  - SPI supports one data channel half-duplex transfer
  - SPI supports receive-only mode
  - I2S interface with external audio CODEC
  - I2S supports Master and Slave mode
  - I2S supports 8-, 16-, 24- and 32-bit audio data sizes
  - I2S supports mono and stereo audio data
  - I2S supports PCM mode A, PCM mode B, I2S and MSB justified data format
  - I2S Interface with external audio CODEC
  - I2S provides two 4-level FIFO data buffers, one for transmitting and the other for receiving

- Generates interrupt requests when buffer levels cross a programmable boundary

- EADC
  - Analog input voltage range: 0~ V_{DD}
  - Supports single 12-bit SAR EADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 2 MSPS conversion rate
  - Supports three power saving modes:
    - Deep Power-down mode
    - Power-down mode.
    - Standby mode.
  - Supports single EADC interrupt
  - Supports calibration and load calibration words capability.
  - An A/D conversion can be triggered by Software enable, External pin, Timer 0~3 overflow pulse trigger and PWM trigger.
  - 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
  - Maximum EADC clock frequency is 60 MHz.
  - Configurable EADC internal sampling time.
  - Up to 13 sample modules
    - Each of sample module 0~12 which is configurable for EADC converter channel and trigger source.
    - Double buffer for sample module 0~3
    - Configurable sampling time for each sample module.
    - Conversion results are held in 13 data registers with valid and overrun indicators.
  - Supports PDMA transfer
- USB 1.1 Device Controller
  - Compliant with USB 2.0 Full-Speed specification
  - Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
  - Supports Control/Bulk/Interrupt/Isochronous transfer type
  - Supports suspend function when no bus activity existing for 3 ms
  - Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1k bytes buffer size
  - Provides remote wake-up capability
- Digital Microphone Inputs
  - Provides one 32-level FIFO data buffers for receiving.
  - Generates interrupt requests when buffer levels cross a programmable boundary.
  - Supports PDMA transfer.
  - Supports up to four channel digital microphones.
  - Both digital PDM microphone inputs can be used simultaneously.
- Voice Active Detection
  - Configuration detect levels.
  - Supports idle mode wake-up function.
  - Supports auto switch DMIC path when CPU wake-up by VAD.
  - Generates interrupt requests when voice detected.
- Audio DPWM Modulator
  - Differential Audio PWM Output (DPWM).
  - Supports right channel and sub-woofer channels.
  - Supports sample rates from 16~96 kHz.
  - Programmable biquad 10 band filter.
  - PDMA data channel for streaming of PCM audio data.
  - Supports either single precision floating point or fixed-point format input data and BIQ

coefficients.
- Provides 32-sample FIFO data buffer for PCM data.

- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8-/16-/32-bit of data width
  - Programmable seed value
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
  - Supports using DMA to write data to perform CRC operation
- Stereo Audio Codec
  - DAC SNR 105dB (A-weighted), THD+N -88dB.
  - ADC SNR 102dB (A-weighted), THD+N -91dB.
  - Supports digital audio interface (I2S/PCM).
  - Supports stereo differential analog microphone inputs, two single-ended microphone inputs or one stereo digital microphone input.
  - Supports cap-free low noise microphone bias with internal pull high resistor for microphone.
  - Capless headphone amplifier.
  - Supports dynamic range compressor (DRC) and programmable biquad filter.
- Brown-out Detector
  - With 8 levels: 3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 1.5V
- Operating Temperature: -40℃~85℃
- Packages
  - All Green package (RoHS)
  - LQFP 64-pin (7x7 mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
DMIC	Digital Microphone Inputs
DPWM	Audio DPWM Modulator
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	High Speed RC Oscillator
HXT	External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
VAD	Voice Active Detection
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Parts Information

PART NUMBER		I941A00	
Max. CPU frequency (MHz)		200	200
Flash (KB)		512	512
SRAM (KB)		192	192
ISP Loader ROM (KB)		4	4
I/O		29	16
32-bit Timer		4	4
RTC		√	√
PWM		4	2
USB 1.1 FS Device		√	-
12-bit ADC		5	5
Connectivity	UART	1	1
	SPI	-	-
	SPI/I²S	2	2
	I²S	1	-
	I²C	2	2
Audio Function	Audio DPWM	1.1	-
	DMIC	4	2
	VAD	√	√
Stereo Audio Codec		√	√
Package		LQFP 64 (7x7 mm)	QFN 48 (5x5 mm)

Table 4.1-1 Devices Features and Peripheral Counts

4.2 Ordering Information

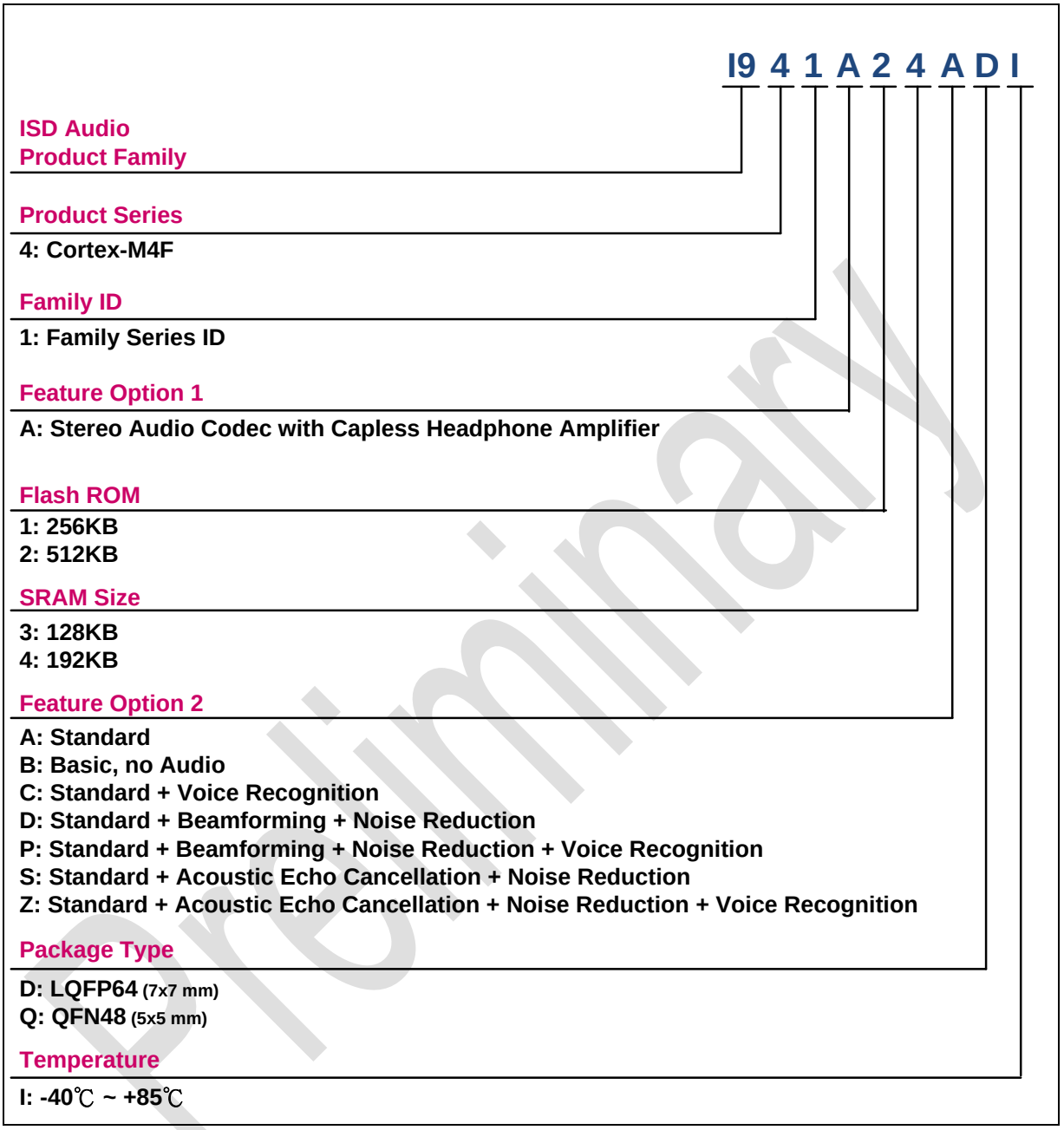


Figure 4.2-1 Ordering Information Scheme

4.3 Pin Configuration

4.3.1 QFN48 (5x5 mm) Pin Diagram

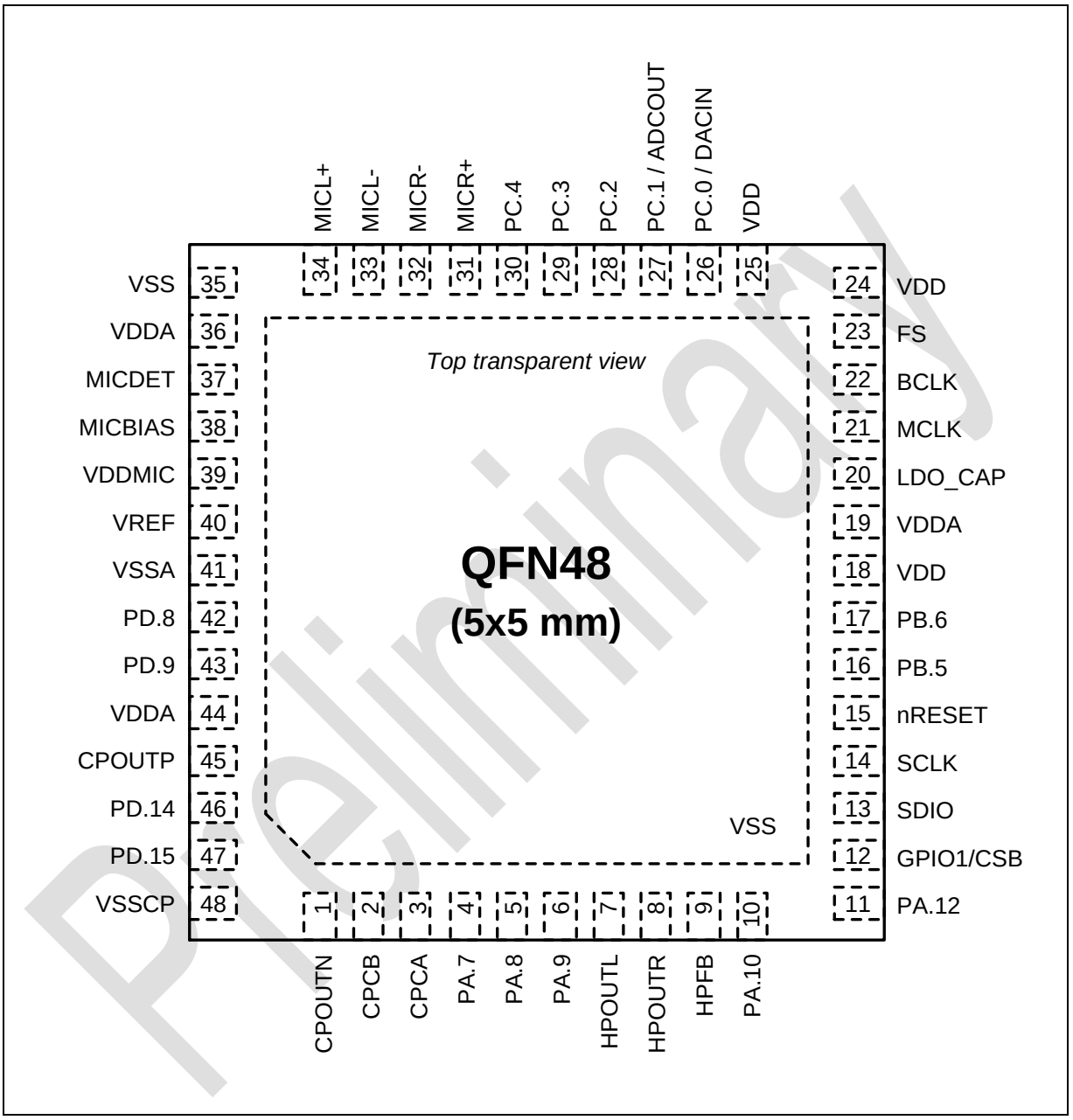


Figure 4.3-1 QFN48 (5x5 mm) Pin Diagram

4.3.2 LQFP64 (7x7 mm) Pin Diagram

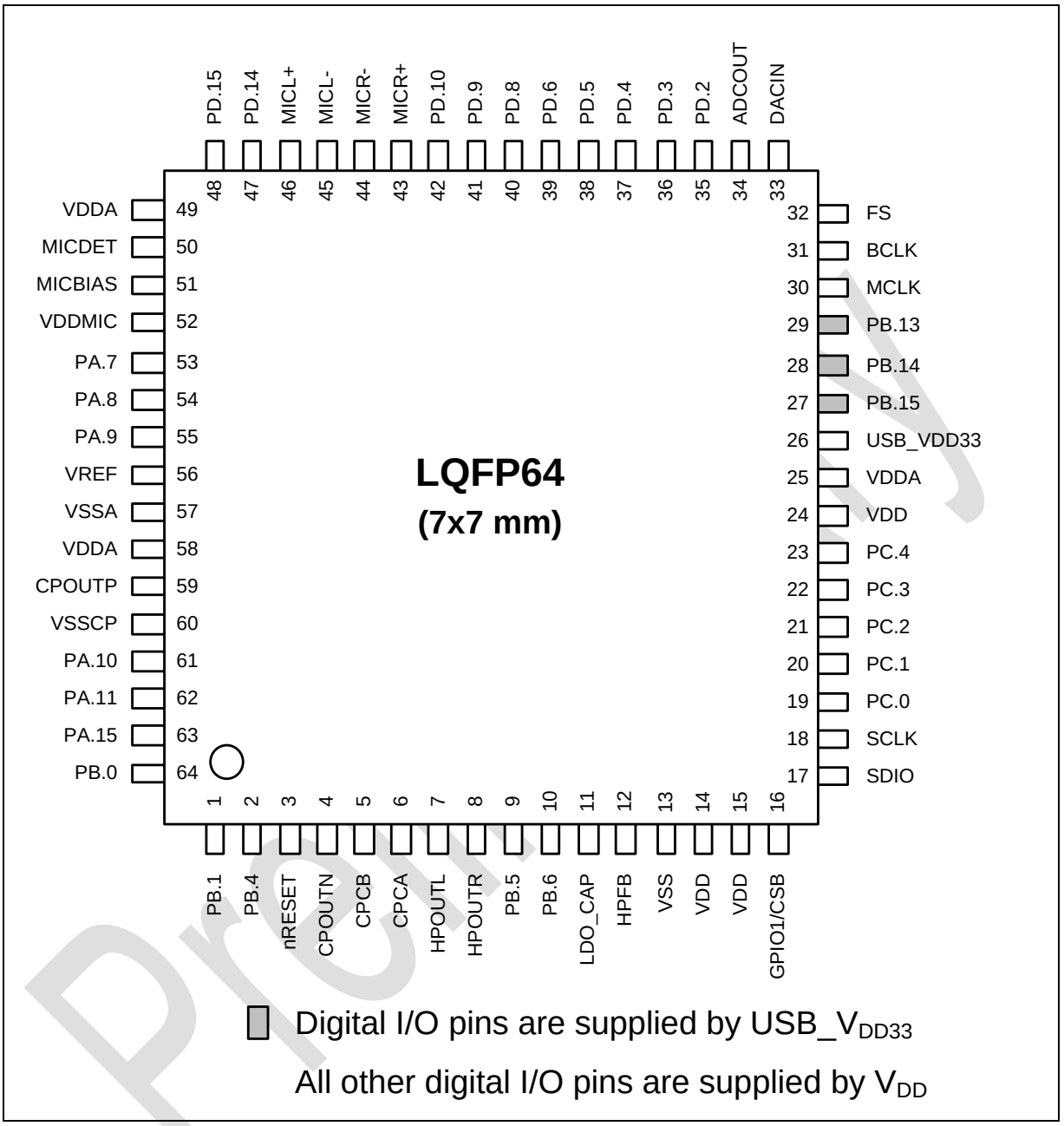


Figure 4.3-2 LQFP64 (7x7 mm) Pin Diagram

4.4 Pin Description

MFP = Multi-function pin.

Note: Pin Type I=Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
	1	PB.1	I/O	MFP0	General purpose digital I/O pin.
		PWM0_SYNC_OUT	I/O	MFP1	PWM0 counter synchronous trigger output pin.
		I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
		PWM0_CH1	I/O	MFP3	PWM0 channel1 output/capture input.
	2	PB.4	I/O	MFP0	General purpose digital I/O pin.
		UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
		PWM0_CH0	I/O	MFP2	PWM0 channel0 output/capture input.
		DMIC_CLK1	O	MFP3	Digital microphone channel 1 clock output pin.
		UART0_TXD	O	MFP4	UART0 data transmitter output pin.
		PWM0_CH4	I/O	MFP5	PWM0 channel4 output/capture input.
15	3	nRESET	I		External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
1	4	CPOUTN	A		Audio codec charge pump negative voltage
2	5	CPCB	A		Audio codec charge pump switching capacitor node B
3	6	CPCA	A		Audio codec charge pump switching capacitor node A
7	7	HPOUTL	A		Audio codec headphone left channel output
8	8	HPOUTR	A		Audio codec headphone right channel output
16	9	PB.5	I/O	MFP0	General purpose digital I/O pin.
		XT1_OUT	I	MFP1	External 4~24.576 MHz (high speed) crystal output pin.
		PWM0_CH1	I/O	MFP2	PWM0 channel1 output/capture input.
		I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
		I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
		DMIC_DAT0	I	MFP5	Digital microphone channel 0 data input pin.
17	10	PB.6	I/O	MFP0	General purpose digital I/O pin.
		XT1_IN	I	MFP1	External 4~24.576 MHz (high speed) crystal input pin.
		PWM0_CH2	I/O	MFP2	PWM0 channel2 output/capture input.
		I2C0_SCL	I/O	MFP4	I2C0 serial clock pin.
		I2C1_SCL	I/O	MFP5	I2C1 serial clock pin.
		DMIC_CLK0	O	MFP6	Digital microphone channel 0 clock output pin.
20	11	LDO_CAP	P		LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
9	12	HPFB	P		Ground pin for headphone driver.
35	13	VSS	P		Ground pin for digital circuit.

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
24	14	VDD	P		Power supply for I/O ports, LDO source for internal PLL, internal analog circuit and digital circuit.
	15	VDD	P		Power supply for I/O ports, LDO source for internal PLL, internal analog circuit and digital circuit.
12	16	GPIO1/CSB	I/O		Audio codec general purpose IO/CSB
13	17	SDIO	I/O		Audio codec serial data for I2C
14	18	SCLK	I		Audio codec serial data clock for I2C
26	19	PC.0	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SCL	I/O	MPF1	I2C1 clock pin.
		X32_OUT	O	MFP2	External 32.768 kHz (low-speed) crystal output pin.
		SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin; or I2S1 data output pin.
27	20	PC.1	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SDA	I/O	MFP1	I2C1 data input/output pin.
		X32_IN	I	MFP2	External 32.768 kHz (low-speed) crystal input pin.
		SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin; or I2S1 data input pin.
28	21	PC.2	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SMBSUS	O	MFP1	I2C1 SMBus SMBSUS# pin (PMBus CONTROL pin)
		TM3	I/O	MFP2	Timer3 event counter input / toggle output.
		SPI1_CLK	I/O	MFP3	SPI1 Serial Clock pin; or I2S1 bit clock pin.
29	22	PC.3	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SMBAL	O	MFP1	I2C1 SMBus SMBALERT# pin
		TM3_EXT	I/O	MFP2	Timer3 external capture input.
		SPI1_SS	I/O	MFP3	SPI1 slave select pin; or I2S1 left right channel clock pin.
30	23	PC.4	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH2	I/O	MFP1	PWM0 channel2 output/capture input.
		CLKO	O	MFP2	Clock Output pin.
		SPI1_I2SMCLK	O	MFP3	SPI1 I2S master clock output pin.
18	24	VDD	P		Power supply for I/O ports, LDO source for internal PLL, internal analog circuit and digital circuit.
19	25	VDDA	P		Power supply for audio codec analog circuit.
	26	USB_VDD33	P		Power supply for USB, DC 3.3V.
	27	PB.15	I/O	MFP0	General purpose digital I/O pin.
		USB_VBUS	P	MFP1	Power supply from USB or HUB.
		I2S0_MCLK	O	MFP2	I2S0 master clock output pin.
	28	PB.14	I/O	MFP0	General purpose digital I/O pin.
		USB_D-	A	MFP1	USB differential signal D-.
		I2S0_DO	O	MFP2	I2S0 data output pin.

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
	29	PB.13	I/O	MFP0	General purpose digital I/O pin.
		USB_D+	A	MFP1	USB differential signal D+.
		I2S0_DI	I	MFP2	I2S0 data input pin.
21	30	MCLK	I		Audio codec master clock input
22	31	BCLK	I/O		Audio codec serial data bit clock input or output for I2S or PCM data
23	32	FS	I/O		Audio codec frame sync input or output for I2S or PCM data
26	33	DACIN	I		Audio codec serial audio data input for I2S or PCM data
27	34	ADCOUT	O		Audio codec serial audio data output for I2S or PCM data
	35	PD.2	I/O	MFP0	General purpose digital I/O pin.
		TRACE_CLK	O	MFP1	TPIU for ETM Tx trace clock output pin.
		SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
		I2S0_MCLK	O	MFP3	I2S0 master clock output pin.
		I2C1_SCL	I/O	MFP4	I2C1 clock pin.
		TM0	I/O	MFP5	Timer0 event counter input / toggle output.
	36	PD.3	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA0	O	MFP1	TPIU for ETM Tx trace data output bit0.
		SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
		I2S0_LRCK	I/O	MFP3	I2S0 left right channel clock pin.
		DMIC_CLK1	O	MFP4	Digital microphone channel 1 clock output pin.
		TM2	I/O	MFP5	Timer2 event counter input / toggle output.
	37	PD.4	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA1	O	MFP1	TPIU for ETM Tx trace data output bit1.
		SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
		I2S0_DI	I	MFP3	I2S0 data input pin.
		DMIC_DAT1	I	MFP4	Digital microphone channel 1 data input pin.
		TM1	I/O	MFP5	Timer1 event counter input / toggle output.
	38	PD.5	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA2	O	MFP1	TPIU for ETM Tx trace data output bit2.
		SPI1_SS	I/O	MFP2	SPI1 Slave Select pin.
		I2S0_DO	O	MFP3	I2S0 data output pin.
		DMIC_CLK0	O	MFP4	Digital microphone channel 0 clock output pin.
		DPWM_RN	O	MFP5	Audio DPWM right channel negative output pin.

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
	39	PD.6	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA3	O	MFP1	TPIU for ETM Tx trace data output bit3.
		SPI1_I2SMCLK	O	MFP2	SPI1 I2S master clock output pin
		I2S0_BCLK	I/O	MFP3	I2S0 Bit Clock pin.
		DMIC_DAT0	I	MFP4	Digital microphone channel 0 data input pin.
		DPWM_RP	O	MFP5	Audio DPWM right channel positive output pin.
42	40	PD.8	I/O	MFP0	General purpose digital I/O pin.
		ICE_CLK	I	MFP1	Serial wired debugger clock pin
		TM0	I/O	MFP2	Timer0 event counter input / toggle output.
		I2C1_SCL	I/O	MFP3	I2C1 clock pin.
		I2C0_SCL	I/O	MFP4	I2C0 clock pin.
		DPWM_SN	O	MFP5	Audio DPWM sub-woofer channel negative output pin.
43	41	PD.9	I/O	MFP0	General purpose digital I/O pin.
		ICE_DAT	I/O	MFP1	Serial wired debugger data pin
		TM0_EXT	I/O	MFP2	Timer0 external capture input.
		I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
		I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
		DPWM_SP	O	MFP5	Audio DPWM sub-woofer channel positive output pin.
	42	PD.10	I/O	MFP0	General purpose digital I/O pin.
		INT5	I	MFP1	External interrupt5 input pin.
		EADC0_ST	I	MFP2	EADC0 external trigger input.
31	43	MICR+	A		PGA MICR+ analog input
32	44	MICR-	A		PGA MICR- analog input / Digital microphone clock output
33	45	MICL-	A		PGA MICL- analog input / Digital microphone data input
34	46	MICL+	A		PGA MICL+ analog input
46	47	PD.14	I/O	MFP0	General purpose digital I/O pin.
		UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
		EADC0_CH11	A	MFP2	EADC0 channel11 analog input.
		I2C0_SCL	I/O	MFP3	I2C0 clock pin.
		UART0_TXD	O	MFP4	UART0 data transmitter output pin.
		I2C1_SCL	I/O	MFP5	I2C1 clock pin.

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
47	48	PD.15	I/O	MFP0	General purpose digital I/O pin.
		UART0_nRTS	O	MFP1	Request to Send output pin for UART0.
		EADC0_CH12	A	MFP2	EADC0 channel12 analog input.
		I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
		UART0_RXD	I	MFP4	UART0 data receiver input pin.
		I2C1_SDA	I/O	MFP5	I2C1 data input/output pin.
36	49	VDDA	P		Power supply for audio codec analog circuit.
37	50	MICDET	A		Microphone/button detect, 2kOhm between Mic and MICBIAS.
38	51	MICBIAS	A		Microphone bias output
39	52	VDDMIC	P		Power supply for audio codec microphone bias.
4	53	PA.7	I/O	MFP0	General purpose digital I/O pin.
		UART0_TXD	O	MFP1	UART0 data transmitter output pin.
		EADC0_CH7	A	MFP2	EADC0 channel7 analog input.
		SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin; or I2S2 data input pin.
5	54	PA.8	I/O	MFP0	General purpose digital I/O pin.
		UART0_RXD	I	MFP1	UART0 data receiver input pin..
		EADC0_CH8	A	MFP2	EADC0 channel8 analog input.
		SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin; or I2S2 data output pin.
6	55	PA.9	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SCL	I/O	MFP1	I2C0 Serial Clock pin
		EADC0_CH9	A	MFP2	EADC0 channel9 analog input.
		SPI2_SS	I/O	MFP4	SPI2 slave select pin; or I2S2 left right channel clock pin.
40	56	VREF	A		Internal DAC & ADC voltage reference decoupling I/O
41	57	VSSA	P		Ground pin for audio codec analog circuit.
44	58	VDDA	P		Power supply for audio codec analog circuit.
45	59	CPOUTP	A		Audio codec charge pump positive voltage.
48	60	VSSCP	P		Audio codec charge pump supply ground.
10	61	PA.10	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SDA	I/O	MFP1	I2C0 data input/output pin.
		EADC0_ST	I	MFP2	EADC0 external trigger input.
		DPWM_RN	O	MFP3	Audio DPWM right channel negative output pin.
		SPI2_CLK	I/O	MFP4	SPI2 clock pin; or I2S2 bit clock pin.
	62	PA.11	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SMBSUS	O	MFP1	I2C0 SMBus SMBSUS# pin (PMBus CONTROL pin)
		TM0	I/O	MFP2	Timer0 event counter input / toggle output.
		DPWM_RP	O	MFP3	Audio DPWM right channel positive output pin.

Package		Pin Name	Type	MFP	Description
QFN 48 (5x5)	LQFP 64 (7x7)				
11		PA.12	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SMBAL	O	MFP1	I2C0 SMBus SMBALERT# pin.
		TM0_EXT	I/O	MFP2	Timer0 external capture input.
		SPI2_I2SMCLK	O	MFP4	SPI2 I2S master clock output pin.
	63	PA.15	I/O	MFP0	General purpose digital I/O pin.
		INT0	I	MFP1	External interrupt0 input pin.
		TM1_EXT	I/O	MFP2	Timer1 external capture input.
	64	PB.0	I/O	MFP0	General purpose digital I/O pin.
		PWM0_SYNC_IN	I/O	MFP1	PWM0 counter synchronous trigger input pin.
		I2C0_SCL	I/O	MFP2	I2C0 clock pin.
		PWM0_CH0	I/O	MFP3	PWM0 channel0 output/capture input.

Table 4.4-1 Pin Description

4.5 GPIO Alternate Function Summary

MFP* = Multi-function pin. (Reference section)

Pin function is defined in SYS_GPx_MFPx registers. For example PA0~7 pin functions are defined in SYS_GPA_MFPL register, and PA8~15 pin functions are defined in SYS_GPA_MFPH register.

MFP0	MFP1	MFP2	MFP3	MFP4	MFP5
PA.7	UART0_TXD	EADC0_CH7		SPI2_MISO	
PA.8	UART0_RXD	EADC0_CH8		SPI2_MOSI	
PA.9	I2C0_SCL	EADC0_CH9		SPI2_SS	
PA.10	I2C0_SDA	EADC0_ST	DPWM_RN	SPI2_CLK	
PA.11	I2C0_SMBSUS	TM0	DPWM_RP		
PA.12	I2C0_SMBAL	TM0_EXT		SPI2_I2SMCLK	
PA.15	INT0	TM1_EXT			
PB.0	PWM0_SYNC_IN	I2C0_SCL	PWM0_CH0		
PB.1	PWM0_SYNC_OUT	I2C0_SDA	PWM0_CH1		
PB.4	UART0_nCTS	PWM0_CH0	DMIC_CLK1	UART0_TXD	PWM0_CH4
PB.5	XT1_OUT	PWM0_CH1	I2C0_SDA	I2C1_SDA	DMIC_DAT0
PB.6	XT1_IN	PWM0_CH2	I2C0_SCL	I2C1_SCL	DMIC_CLK0
PB.13	USB_D+	I2S0_DI			
PB.14	USB_D-	I2S0_DO			
PB.15	USB_VBUS	I2S0_MCLK			
PC.0	I2C1_SCL	X32_OUT	SPI1_MOSI		
PC.1	I2C1_SDA	X32_IN	SPI1_MISO		
PC.2	I2C1_SMBSUS	TM3	SPI1_CLK		
PC.3	I2C1_SMBAL	TM3_EXT	SPI1_SS		
PC.4	PWM0_CH2	CLKO	SPI1_I2SMCLK		
PD.2	TRACE_CLK	SPI1_MOSI	I2S0_MCLK	I2C1_SCL	TM0
PD.3	TRACE_DATA0	SPI1_MISO	I2S0_LRCK	DMIC_CLK1	TM2
PD.4	TRACE_DATA1	SPI1_CLK	I2S0_DI	DMIC_DAT1	TM1
PD.5	TRACE_DATA2	SPI1_SS	I2S0_DO	DMIC_CLK0	DPWM_RN
PD.6	TRACE_DATA3	SPI1_I2SMCLK	I2S0_BCLK	DMIC_DAT0	DPWM_RP
PD.8	ICE_CLK	TM0	I2C1_SCL	I2C0_SCL	DPWM_SN
PD.9	ICE_DAT	TM0_EXT	I2C1_SDA	I2C0_SDA	DPWM_SP
PD.10	INT5	EADC0_ST			
PD.14	UART0_nCTS	EADC0_CH11	I2C0_SCL	UART0_TXD	I2C1_SCL
PD.15	UART0_nRTS	EADC0_CH12	I2C0_SDA	UART0_RXD	I2C1_SDA

Table 4.5-1 GPIO Alternate Function Summary

4.6 Digital I/Os Power Domain

The digital I/Os are powered from VDD and USB_VDD33 as shown in Table 4.6-1.

Digital I/O Power Domain	Digital I/Os
VDD	GPIO1/CSB, SDIO, SCLK, MCLK, BCLK, FS, DACIN, ADCOUT, PA, PB, PC, PD except PB[13:15]
USB_VDD33	PB[13:15]

Table 4.6-1 Digital I/Os Power Domain

5 BLOCK DIAGRAM

5.1 ISD941A00 Series Block Diagram

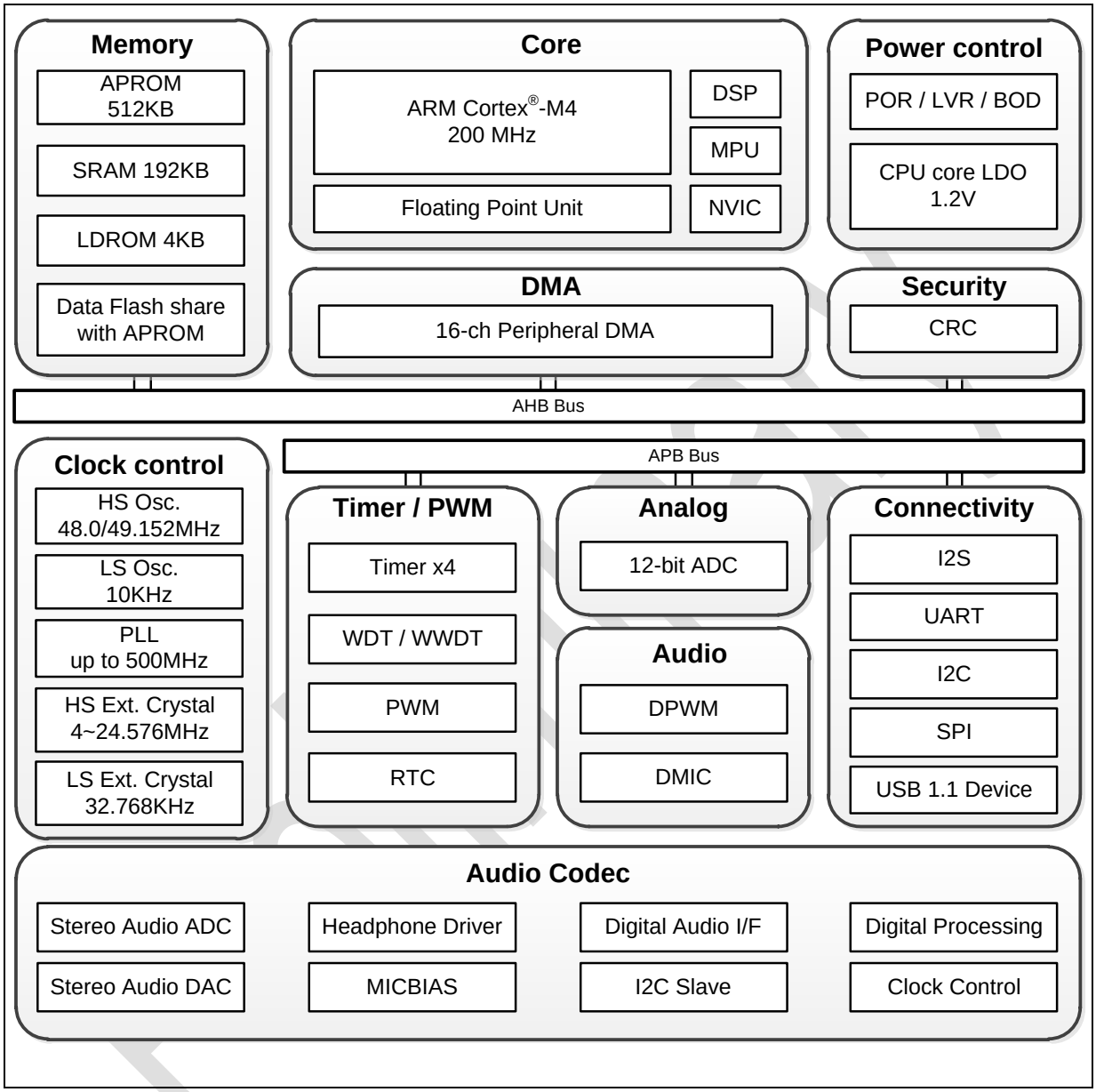


Figure 5.1-1 ISD941A00 Series Block Diagram

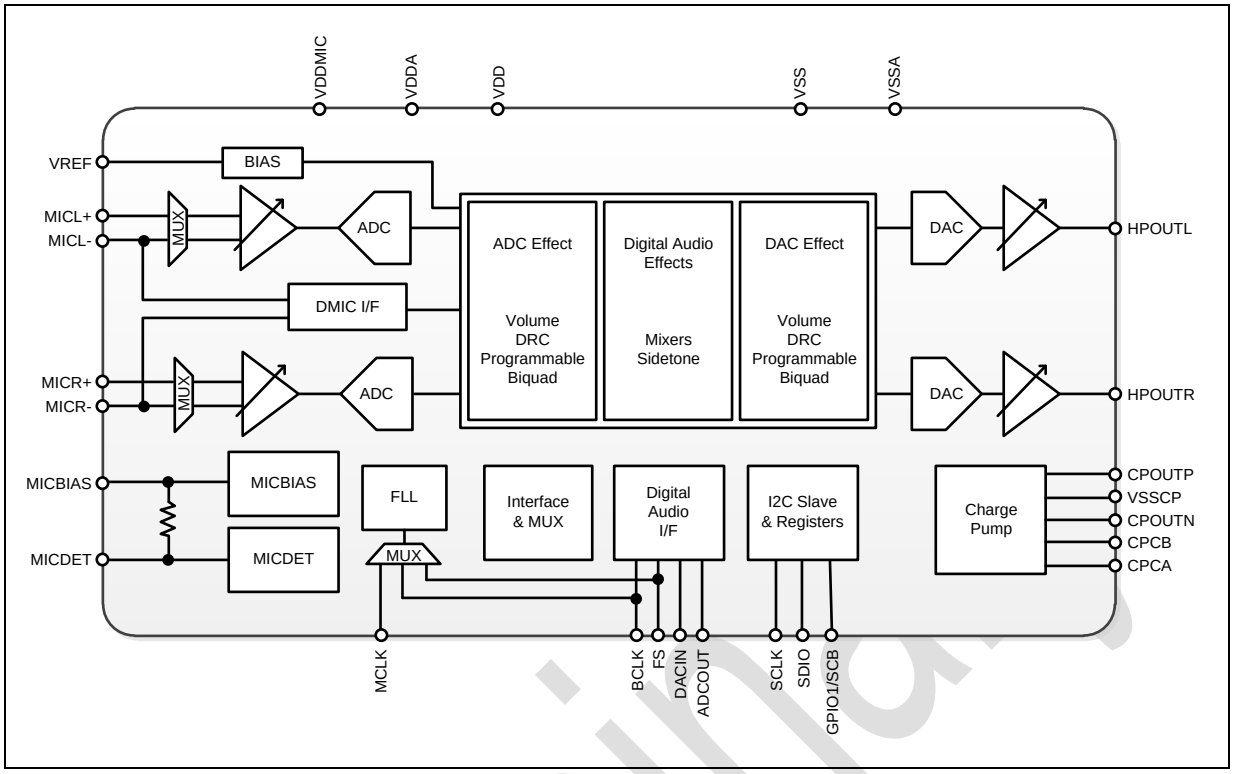


Figure 5.1-2 ISD941A00 Series Audio Codec Block Diagram

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

6.1.1 Voltage Characteristics

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	V_{DD} and USB_V_{DD33} supply voltage	-0.3	+3.6	V
$V_{DDA} - V_{SSA}$	V_{DDA} supply voltage	-0.3	+2.2	V
$V_{DDMIC} - V_{SSA}$	V_{DDMIC} supply voltage	-0.3	+4.0	V
$\|\Delta V_{SS}\|$	Voltage difference V_{SS} to V_{SSA}, V_{SSCP}		50	mV
V_{IN}	Input voltage on V_{DD} power domain digital I/O 5V-tolerance digital I/O	-0.3	5.5	V
	Input voltage on V_{DD} power domain digital I/O Non 5V-tolerance digital I/O[2]	-0.3	V_{DD}	
	Input voltage on analog inputs	-0.3	V_{DDA} + 0.3	

Table 6.1.1-1 Voltage characteristics

Note:

1. All main power and ground pins must always be connected to the external power supply, in the permitted range.
2. Non 5V-tolerance digital I/O: nRESET, PA[7:9], PB[5:6], PB[13:15], PC[0:1], PD[14:15] GPIO1/CSB, SDIO, SCLK, MCLK, BCLK, FS, DACIN and ADCOUT.

6.1.2 Current Characteristics

Symbol	Parameter	Min	Max	Unit
I_{DD}	Maximum Current into V_{DD}		200	mA
I_{SS}	Maximum Current out of V_{SS}		100	
I_{IO}	Maximum Current sunk by a I/O pin		20	
	Maximum Current sourced by a I/O pin		20	
	Maximum Current sunk by total I/O pins		100	
	Maximum Current sourced by total I/O pins		100	

Table 6.1.2-1 Current characteristics

6.1.3 Thermal Characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	

Table 6.1.3-1 Thermal characteristics

6.2 General Operating Conditions

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency			200	MHz
f_{PCLK}	Internal APB clock frequency			90	MHz
V_{DD}	V_{DD} supply voltage range[1]	1.8		3.3	V
USB_V_{DD33}	USB_V_{DD33} supply voltage range	3.0		3.6	V
V_{DDA}	V_{DDA} supply voltage range	1.62		1.98	V
V_{DDMIC}	V_{DDMIC} supply voltage range	3.0		3.6	V
V_{LDO}	LDO output voltage		1.2		V
C_{LDO}	LDO output capacitor on LDO_CAP pin[2]		1		µF
C_{VREF}	VREF output capacitor on VREF pin[3]		4.7		µF

Table 6.2-1 General Operating Conditions

Note:

1. The limitation of V_{DD} operation voltage is 1.62V ~ 3.6V.
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest V_{SS} pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest VSS pin of the device helps decrease output noise and improves the load transient response.
3. To ensure stability, an external 4.7 µF output capacitor, C_{VREF} must be connected between the VREF pin and the closest V_{SSA} pin of the device.

6.3 DC Electrical Characteristics

6.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin switching rate, program location in memory and so on. The supply current measurents were performed under the following conditions:

- All GPIO pins are in quasi-bidirectional mode and high level, and do not drive external components.
- The typical values are measured with V_{DD} = USB_V_{DD33} = V_{DDMIC} = 1.8 to 3.3V, V_{DDA} = 1.8V and T_A = 25℃.
- The maximum values are measured with V_{DD} = USB_V_{DD33} = V_{DDMIC} = 3.3V, V_{DDA} = 1.8V and T_A = 25℃.
- All digital peripherals and audio codec are disabled, unless otherwise specified.
- OVEN (CLK_LDOCTL[8]) is enabled when the frequency of HCLK high than 160 MHz.
- Program run while(1){} from flash.

Symbol	Parameter	Conditions					Typ	Unit
		Digital Peripherals	f_{HXT}	f_{HIRC}	f_{PLL}	f_{HCLK}		
I_{DD_RUN}	Supply current in normal run mode (RUN)	ALL ON	12 MHz	OFF	OFF	f_{HXT}	5	mA
					160 MHz	f_{PLL}	31	
					200 MHz		39	
			OFF	48 MHz	OFF	f_{HIRC}	10	
		ALL OFF	12 MHz	OFF	OFF	f_{HXT}	3.2	
					160 MHz	f_{PLL}	21	
					200 MHz		26.6	
			OFF	48 MHz	OFF	f_{HIRC}	8	

Table 6.3.1-1 Current Consumption in Normal Run Mode

Symbol	Parameter	Conditions					Typ	Unit
		Digital Peripherals	f_{HXT}	f_{HIRC}	f_{PLL}	f_{HCLK}		
I_{DD_IDLE}	Supply current in idle mode (IDLE)	ALL ON	12 MHz	OFF	OFF	f_{HXT}	3.5	mA
					160 MHz	f_{PLL}	19.6	
					200 MHz		24.9	
			OFF	48 MHz	OFF	f_{HIRC}	6.1	
		ALL OFF	12 MHz	OFF	OFF	f_{HXT}	2.3	
					160 MHz	f_{PLL}	8.5	
					200 MHz		10.6	
			OFF	48 MHz	OFF	f_{HIRC}	2.8	

Table 6.3.1-2 Current Consumption in Idle Mode

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD_PD}	Supply current in power-down mode (PD)	Current flows into V_{DDA}	4	16	μA
		Current flows into V_{DD}, USB_V_{DD33}, V_{DDMIC}	700	3500	
I_{DD_LLPD}	Supply current in low leakage power-down mode (LLPD)	Current flows into V_{DDA}	4	16	
		Current flows into V_{DD}, USB_V_{DD33}, V_{DDMIC}	350	1500	
I_{DD_SDP0}	Supply current in standby power-down mode 0 (SPD0)	Current flows into V_{DDA}	4	16	
		Current flows into V_{DD}, USB_V_{DD33}, V_{DDMIC}	25.4	70	
I_{DD_SPD1}	Supply current in standby power-down mode 1 (SPD1)	Current flows into V_{DDA}	4	16	
		Current flows into V_{DD}, USB_V_{DD33}, V_{DDMIC}	15.4	46	
I_{DD_DPD}	Supply current in deep power-down mode (DPD)	Current flows into V_{DDA}	4	16	
		Current flows into V_{DD}, USB_V_{DD33}, V_{DDMIC}	3.9	9.5	

Table 6.3.1-3 Current Consumption in Power-down Mode

Note:

1. The MCU is configured for pin wakeup.

6.3.2 I/O DC Characteristics

6.3.2.1 I/O Input Characteristics

(T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
PA, PB, PC and PD pins						
V_{IL}	Input Low Voltage (Schmitt trigger)			0.3 V_{DD}	V	I/O in V_{DD} domain
				0.3 USB_V_{DD33}		I/O in USB_V_{DD33} domain
	Input low voltage (TTL trigger)			0.8		V_{DD} = USB_V_{DD33} = 3.3 V
				0.6		V_{DD} = USB_V_{DD33} = 1.8 V
V_{IH}	Input High Voltage (Schmitt trigger)	0.75 V_{DD}			V	I/O in V_{DD} power domain
		0.75 USB_V_{DD33}				I/O in USB_V_{DD33} domain
	Input high voltage (TTL trigger)	2.0				V_{DD} = USB_V_{DD33} = 3.3 V
		1.5				V_{DD} = USB_V_{DD33} = 1.8 V
V_{HY}	Hysteresis voltage of schmitt input		0.2 V_{DD}		V	I/O in V_{DD} domain
			0.2 USB_V_{DD33}			I/O in USB_V_{DD33} domain
I_{LK}	Input leakage current	-1		+1	μA	V_{SS} < V_{IN} < V_{DD} V_{SS} < V_{IN} < USB_V_{DD33} Open-drain or input only mode
		-1		+1		V_{DD} < V_{IN} < 5V USB_V_{DD33} < V_{IN} < 5V Open-drain or input only mode on any other 5V tolerance pins
R_{PU}	Internal pull up resistor		52		kΩ	
R_{PD}	Internal pull down resistor		52		kΩ	
nRESET pin						
V_{ILR}	Input Low Voltage (Schmitt trigger)			0.3 V_{DD}	V	
V_{IHR}	Input High Voltage (Schmitt trigger)	0.7 V_{DD}			V	
R_{RST}	Internal nRESET pull up resistor		50		kΩ	
GPIO1/CSB, SDIO, SCLK, MCLK, BCLK, FS, DACIN, ADCOUT pin						
V_{IL}	Input low voltage			0.37 V_{DD}	V	V_{DD} = 3.3V
				0.33 V_{DD}		V_{DD} = 1.8V
V_{IH}	Input high voltage	0.63 V_{DD}			V	V_{DD} = 3.3V
		0.67 V_{DD}				V_{DD} = 1.8V

Table 6.3.2-1 I/O Input Characteristics

Note:

1. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

6.3.2.2 I/O Output Characteristics

(T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
PA, PB, PC and PD pins						
I_{SR}	Source current for push-pull mode and high level		-20		mA	V_{DD} = USB_V_{DD33} = 3.3 V V_{IN} = 2.8 V
		-14	-15			V_{DD} = USB_V_{DD33} = 2.7 V V_{IN} = 2.3 V
		-11	-7.9			V_{DD} = USB_V_{DD33} = 1.8 V V_{IN} = 1.5 V
I_{SK}	Sink current for push-pull mode and low level	14	20		mA	V_{DD} = USB_V_{DD33} = 3.3 V V_{IN} = 0.5 V
		11	15			V_{DD} = USB_V_{DD33} = 2.7 V V_{IN} = 0.4 V
			8.2			V_{DD} = USB_V_{DD33} = 1.8 V V_{IN} = 0.3 V
GPIO1/CSB, SDIO, SCLK, MCLK, BCLK, FS, DACIN, ADCOUT pin						
V_{OL}	Output low level	0.95 V_{DD}			V	V_{DD} = 3.3V, I_{Load} = 1mA
		0.9 V_{DD}				V_{DD} = 1.8V, I_{Load} = 1mA
V_{OH}	Output high level			0.05 V_{DD}	V	V_{DD} = 3.3V, I_{Load} = 1mA
				0.1 V_{DD}		V_{DD} = 1.8V, I_{Load} = 1mA

Table 6.3.2-2 I/O Output Characteristics

6.4 AC Electrical Characteristics

6.4.1 External High Speed Crystal (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24.576 MHz crystal. All the information given in this section are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_OUT pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time.

(V_{DD} - V_{SS} = 3.3 V and T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
f_{HXT}	Oscillator Frequency	4	12	24.576	MHz	
I_{HXT_GM}	Operating Current (GM-type Crystal)		0.37		mA	4 MHz, Gain = L0
			0.5			12 MHz, Gain = L1
			0.66			16 MHz, Gain = L2
			0.84			24 MHz, Gain = L3
I_{HXT_INV}	Operating Current (INV-type Crystal)		0.57		mA	4 MHz, Gain = L0
			1.4			12 MHz, Gain = L1
			2.1			16 MHz, Gain = L2
			2.8			24 MHz, Gain = L3

Table 6.4.1-1 External High Speed Crystal (HXT) Characteristics

6.4.1.1 HXT Typical Crystal Application Circuit

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2.

Crystal	C_1	C_2
4 MHz ~ 24.576 MHz	Optional (depending on the crystal specification)	

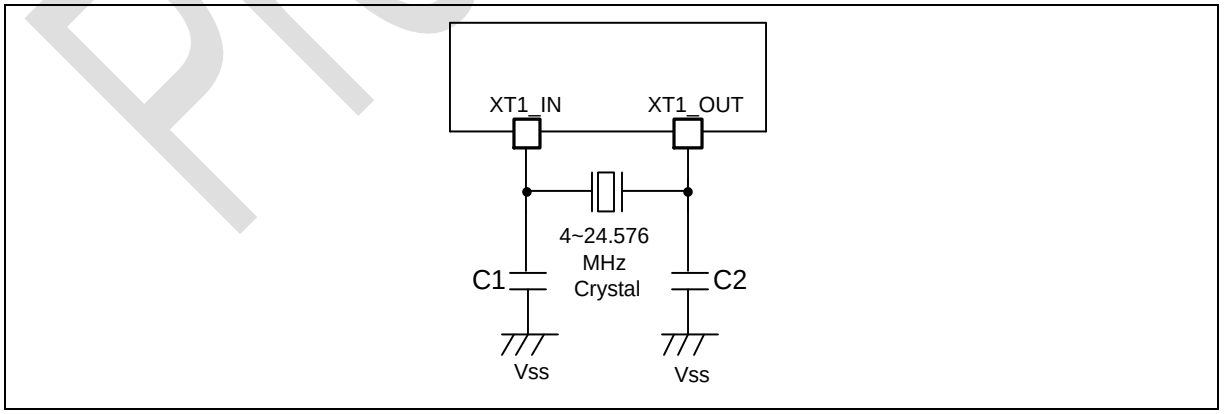


Figure 6.4-1 HXT Typical Crystal Application Circuit

6.4.2 Internal High Speed RC Oscillator (HIRC) Characteristics

The HIRC oscillator is calibrated in production.

(V_{DD} - V_{SS} = 3.3 V and T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{HIRC}	Oscillator frequency		49.152		MHz	HIRCFSEL (CLK_CLKSEL0[24]) = 0
			48			HIRCFSEL (CLK_CLKSEL0[24]) = 1
	Calibrated Internal Oscillator Frequency		±0.25		%	V_{DD} = 3.3 V
		-3		+3	%	T_A = -40℃ ~ 85 ℃
I_{HIRC}	Operating Current		200		μA	

Table 6.4.2-1 Internal High Speed RC Oscillator (HIRC) Characteristics

6.4.3 External Low Speed Crystal (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time.

(V_{DD} - V_{SS} = 3.3 V and T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Operating current		0.8		μA	
T_S	Oscillator stable time		300	500	ms	

Table 6.4.3-1 External Low Speed Crystal (LXT) Characteristics

6.4.3.1 LXT Typical Crystal Application Circuit

Crystal	C_1	C_2
32.768 kHz	Optional (depending on the crystal specification)	

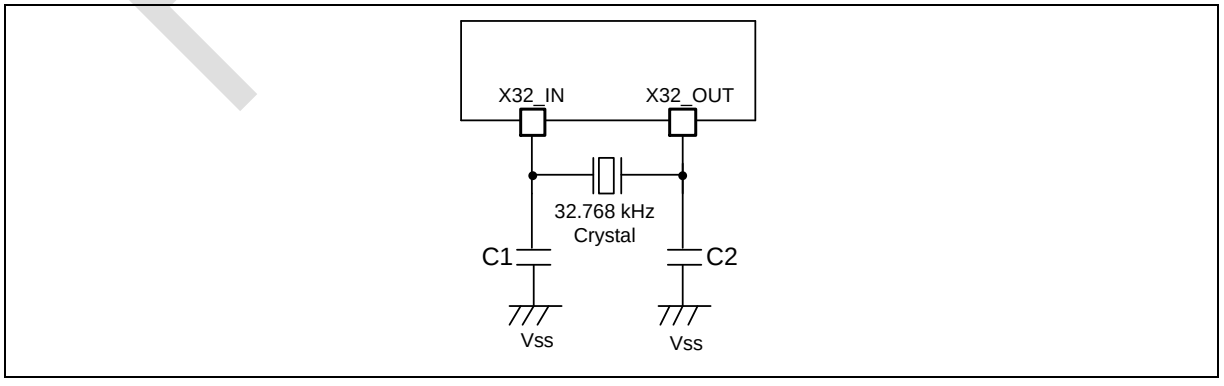


Figure 6.4-2 LXT Typical Crystal Application Circuit

6.4.4 Internal Low Speed RC Oscillator (LIRC) Characteristics

(V_{DD} - V_{SS} = 3.3 V and T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{LRC}	Oscillator frequency	5	10	15	kHz	
I_{LIRC}	Operating current		500		nA	
T_S	Oscillator stable time		100		µS	

Table 6.4.4-1 Internal Low Speed RC Oscillator (LIRC) Characteristics

6.5 Analog Characteristics

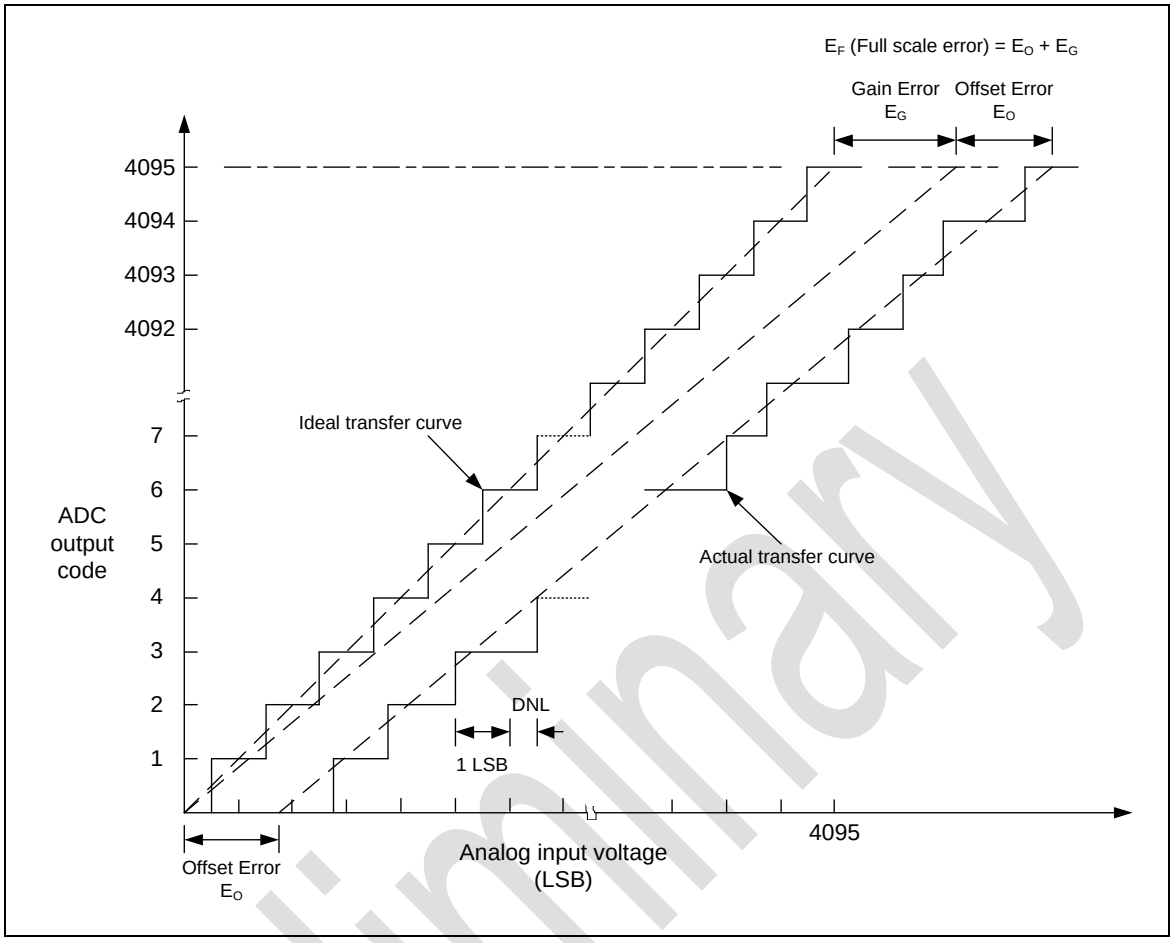
6.5.1 12-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution		12		Bit	-
DNL	Differential Nonlinearity Error			±2	LSB	2MSPS
INL	Integral Nonlinearity Error			±4	LSB	2MSPS
E_O	Offset Error		2		LSB	2MSPS
E_G	Gain Error (Transfer Gain)		-3		LSB	2MSPS
E_A	Absolute Error		6		LSB	2MSPS
-	Monotonic		Guaranteed		-	-
F_{ADC}	ADC Clock Frequency	0.14		60	MHz	V_{DD} = 1.8~3.6 V
F_S	Sample Rate (F_{ADC}/T_{CONV})			2000	kSPS	V_{DD} = 1.8~3.6 V
T_{ACQ}	Acquisition Time (Sample Stage)		2~9		$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time		16~23		$1/F_{ADC}$	-
V_{IN}	Analog Input Voltage	0		V_{DD}	V	-
C_{IN}	Input Capacitance		6		pF	-

Table 6.5.1-1 12-bit SARADC Characteristics

Note:

1. This table is guaranteed by characteristics result, not tested in production.
2. The condition is that the error in a conversion started after ADC enable is less than ±0.5 LSB. The reference and input signal are already settled.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

6.5.2 LDO

(V_{DD} - V_{SS} = 1.62 ~ 3.6 V and T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LDO}	Output Voltage	1.176	1.2	1.224	V	Normal mode
			1.26		V	OVEN (CLK_LDOCTL[8]) is enabled
			0.9		V	In low leakage power-down mode (LLPD)

Table 6.5.2-1 LDO Characteristics

Note:

1. It is critical that a 0.1 µF capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. To ensure power stability, a 1µF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

6.5.3 Low Voltage Reset and Brown-out Detector

(T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{BOD}	Operating Current		60		µA	V_{DD} = 3.6V
V_{BOD_F}	Brown-out Detect Level (Falling edge)	1.50	1.60	1.70	V	BODVL[2:0]=000
		1.70	1.80	1.90	V	BODVL[2:0]=001
		1.90	2.00	2.10	V	BODVL[2:0]=010
		2.10	2.20	2.30	V	BODVL[2:0]=011
		2.30	2.40	2.50	V	BODVL[2:0]=100
		2.50	2.60	2.70	V	BODVL[2:0]=101
		2.70	2.80	2.90	V	BODVL[2:0]=110
		2.90	3.00	3.10	V	BODVL[2:0]=111
V_{BOD_R}	Brown-out Detect Level (Rising edge)		V_{BOD_F} + V_{HYS_BOD}			
V_{HYS_BOD}	Hysteresis		80		mV	
V_{LVR}	Low Voltage Reset Voltage	1.45	1.5	1.55	V	

Table 6.5.3-1 Low Voltage Reset and Brown-out Detector Characteristics

6.5.4 Power-on Reset

(T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{POR}	Power-on Reset Voltage		1.45		V	
V_{PORHYS}	Power-on Reset Hysteresis		110		mV	
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	0.01			ms/V	
FR_{VDD}	VDD Falling Rate to Ensure Power-on Reset	0.5			ms/V	

Table 6.5.4-1 Power-on Reset Characteristics

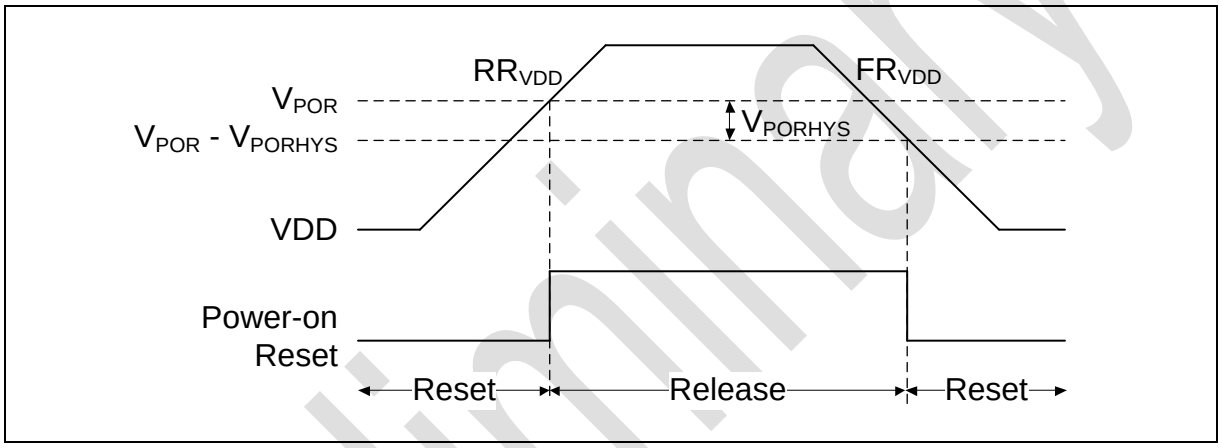


Figure 6.5-1 Power-on Reset Condition

6.6 Audio Codec Characteristics

(V_{DDA} = 1.8V; V_{DDMIC} = 3.6V, R_L(Headphone) = 32 Ω, f = 1kHz, MCLK=12.88MHz, unless otherwise specified. Limits apply for T_A = 25°C)

6.6.1 Audio Codec Supply Current Characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
ISD	Shutdown Current	V_{DDA}	4	16	μA
		V_{DDMIC}	0.2	1	
I_{DD}	Active Current Normal Playback Mode	f_S = 48kHz, Stereo HP DAC On, HP On, P_{OUT} = 0mW. R_L(HP) = 32Ω		5	mA

Table 6.6.1-1 Audio Codec Supply Current Characteristics

6.6.2 Audio Codec Headphone Amplifier Characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
P_O	Output Power	Stereo RL = 32Ω, DAC Input, f=1020Hz, 22kHz BW, THD+N = 1%	28		mW
		Stereo RL = 16Ω, DAC Input, f=1020Hz, 22kHz BW, THD+N = 1%	33		mW
THD+N	Total Harmonic Distortion + Noise	RL = 32Ω, f=1020Hz, PO = 20mW	-88		dB
SNR	Signal to Noise Ratio	VOUT = $1V_{RMS}$, Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted)	105		dB
		VOUT = $1V_{RMS}$, Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted, auto attenuate enabled	108		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{PP} input Referred, Gain = 0dB DAC Input, Ripple Applied to V_{DDA}	90		dB
		Mono_Gain = 0dB Ripple Applied to V_{DDA}	90		dB
		Stereo Single Ended Input Terminated, Stereo_Gain = 0dB Ripple Applied to V_{DDA}	90		dB
XTALK	Channel Crosstalk	Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1020Hz	70		dB
	Interchannel Level Mismatch		±0.1		dB
	Frequency Response	f = 20Hz ~ 20kHz	+0.1/-0.2		dB
	Pop up Noise			1	mV_{RMS}
e_{OS}	Output Noise	Gain = 0dB, f_S=48kHz, OSR = 128, A-Weighted	4.4		uV_{RMS}
	Out of Band Noise Level		-60		dB
V_{OS}	Output Offset Voltage	Gain= 0dB, DAC Input		±1	mV
	Power Consunption MP3 Mode	No Load, No Signal, Amp on fs = 48kHz, Stereo DAC On, Amp On, P_{OUT} = 0mW. R_L = 32Ω	6		mW
	Fs Accuracy (44.1 / 48 kHz)		±0.02		%
	Pop and Click Noise	Plug into or out of DAC to Headphone	1		mV_{RMS}

Table 6.6.2-1 Audio Codec Headphone Amplifier Characteristics

6.6.3 Audio Codec ADC Characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1020Hz, fs = 48KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5mVrms, f=1020Hz, Digital Gain = 0dB, Mono Differential Input	-80		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 48kHz, Mono Differential Input	102		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 48kHz, Mono Differential Input	101		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVPP applied to V_{DDA}, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	90		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100mVrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	65		dB
FS_{ADC}	ADC Full Scale Input Level	V_{DDA}= 1.8V	1		V_{RMS}
	Minimum Input Impedance		10		kOhm
	Frequency Response	f = 20Hz ~ 20kHz	+0.1/-0.2		dB
	Pop up Noise		1		mV_{RMS}
	Power Consumption	No Signal, ADC on fs = 44.1kHz	5		mW

Table 6.6.3-1 Audio Codec ADC Characteristics

6.6.4 Audio Codec MICBIAS Characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{BIAS}	Output Voltage	Programmable 1.8V to 3.0V in 6 steps	2.5		V
I_{OUT}	Output Current			4	mA
e_{os}	Output Noise	Low noise mode, at 1kHz		47	nV/√ Hz

Table 6.6.4-1 Audio Codec MICBIAS Characteristics

6.7 Flash DC Electrical Characteristic

(T_A = 25 ℃ unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{FLA}[1]	Supply Voltage	1.08		1.32	V	
N_{ENDUR}	Endurance	10000			cycles[2]	
T_{RET}	Data Retention	10			year	
T_{ERASE}	Page Erase Time	92		160	ms	
T_{MER}	Mass Erase Time	300		350	ms	
T_{PROG}	Program Time	42		50	us	
I_{DD1}	Read Current			4.12	mA	
I_{DD2}	Program Current			5	mA	
I_{DD3}	Erase Current			5	uA	

Table 6.7-1 Flash DC Electrical Characteristics

Note:

1. VFLA is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table is guaranteed by design, not test in production.

6.8 VAD Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{VADIDLE}$	Operation Current Idle mode with VAD		1.25		mA	VDDA = VDD = 3.3 V HCLK = 3.072MHz (HIRC/16) DMIC_MCLK = 1.536 MHz (HIRC/32) DMIC_CLK = 384 kHz (DMIC_MCLK/4) Sample Rate = 8 kHz (Down sample 48) No load

Table 6.8-1 VAD Characteristics

Note: This table is guaranteed by characteristics result, not tested in production.

6.9 Communications Characteristics

6.9.1 USB Characteristics

6.9.1.1 USB Full-Speed Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input High (driven)	2.0			V	
V_{IL}	Input Low			0.8	V	
V_{DI}	Differential Input Sensitivity	0.2			V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8		2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8		2.0	V	
	Receiver Hysteresis		200		mV	
V_{OL}	Output Low (driven)	0		0.3	V	
V_{OH}	Output High (driven)	2.8		3.6	V	
V_{CRS}	Output Signal Cross Voltage	1.3		2.0	V	
R_{PU}	Pull-up Resistor		1.2		kΩ	
Z_{DRV}	Driver Output Resistance		10		Ω	Steady state drive*
C_{IN}	Transceiver Capacitance			20	pF	Pin to GND

Table 6.9.1-1 USB Full-Speed Characteristics

Note:

1. Driver output resistance doesn't include series resistor resistance.

6.9.1.2 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	Rise Time	4		20	ns	C_L=50p
T_{FF}	Fall Time	4		20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90		111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

Table 6.9.1-2 USB Full-Speed PHY Characteristics

6.9.1.3 USB VBUS Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BUS}	VBUS Pin Input Voltage		5.0		V	

Table 6.9.1-3 USB VBUS Characteristics

6.9.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7		1.2		uS
t_{HIGH}	SCL high period	4		0.6		uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7		1.2		uS
$t_{HD;\ STA}$	START condition hold time	4		0.6		uS
$t_{SU;\ STO}$	STOP condition setup time	4		0.6		uS
t_{BUF}	Bus free time	4.7[3]		1.2[3]		uS
$t_{SU;DAT}$	Data setup time	250		100		nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time		1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time		300		300	nS
C_b	Capacitive load for each bus line		400		400	pF

Table 6.9-1 I²C Dynamic Characteristics

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

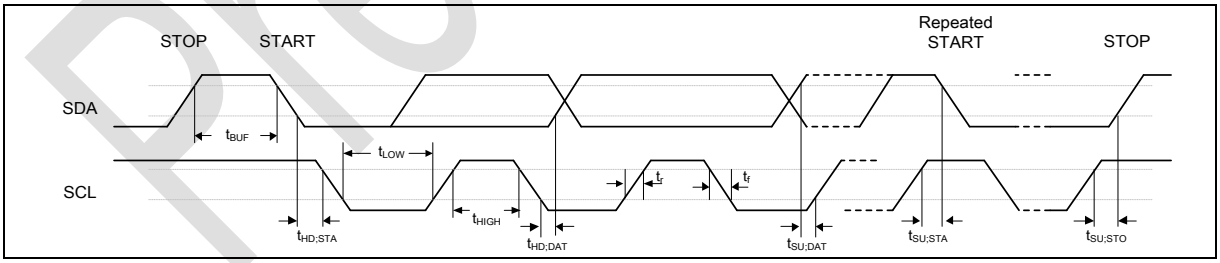


Figure 6.9-1 I²C Timing Diagram

6.9.3 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI MASTER MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5		27.5	ns
t_{DS}	Data input setup time	2			ns
$t_{H(MI)}$	Data input hold time	4			ns
t_V	Data output valid time			1	ns
$t_{H(MO)}$	Data output hold time	0			ns
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5		27.5	ns
t_{DS}	Data input setup time	2			ns
$t_{H(MI)}$	Data input hold time	4			ns
t_V	Data output valid time			1	ns
$t_{H(MO)}$	Data output hold time	0			ns

Table 6.9.3-1 Dynamic Characteristics of Data Input and Output Pin in Master Mode

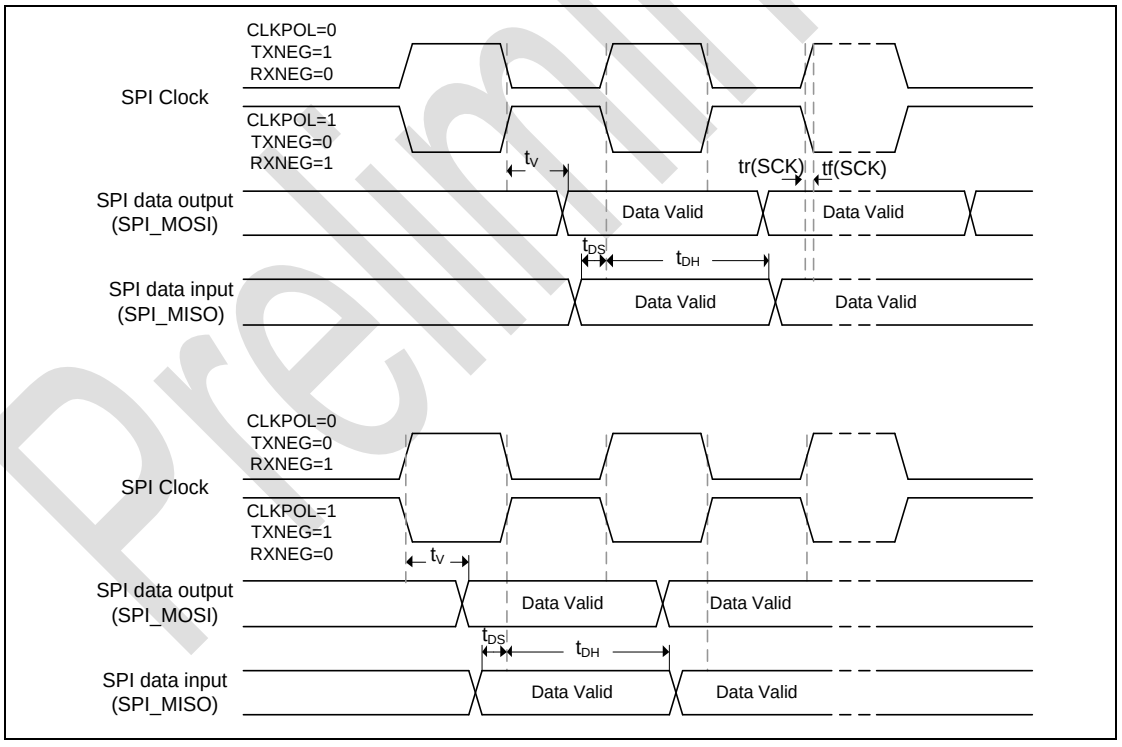


Figure 6.9-2 SPI Master Mode Timing Diagram

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI SLAVE MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3			Peripheral clock
t_{SH}	Slave select hold time	2			Peripheral clock
t_{DS}	Data input setup time	2			ns
$t_{H(SI)}$	Data input hold time	5.5			ns
$t_{a(SO)}$	Data output access time			18	ns
t_V	Data output valid time		18.5-	24.5	ns
$t_{H(SO)}$	Data output hold time	6			ns
SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3			Peripheral clock
t_{SH}	Slave select hold time	2			Peripheral clock
t_{DS}	Data input setup time	2			ns
$t_{H(SI)}$	Data input hold time	6			ns
$t_{a(SO)}$	Data output access time			24	ns
t_V	Data output valid time		23	30	ns
$t_{H(SO)}$	Data output hold time	7			ns

Table 6.9.3-2 Dynamic Characteristics of Data Input and Output Pin in Slave Mode

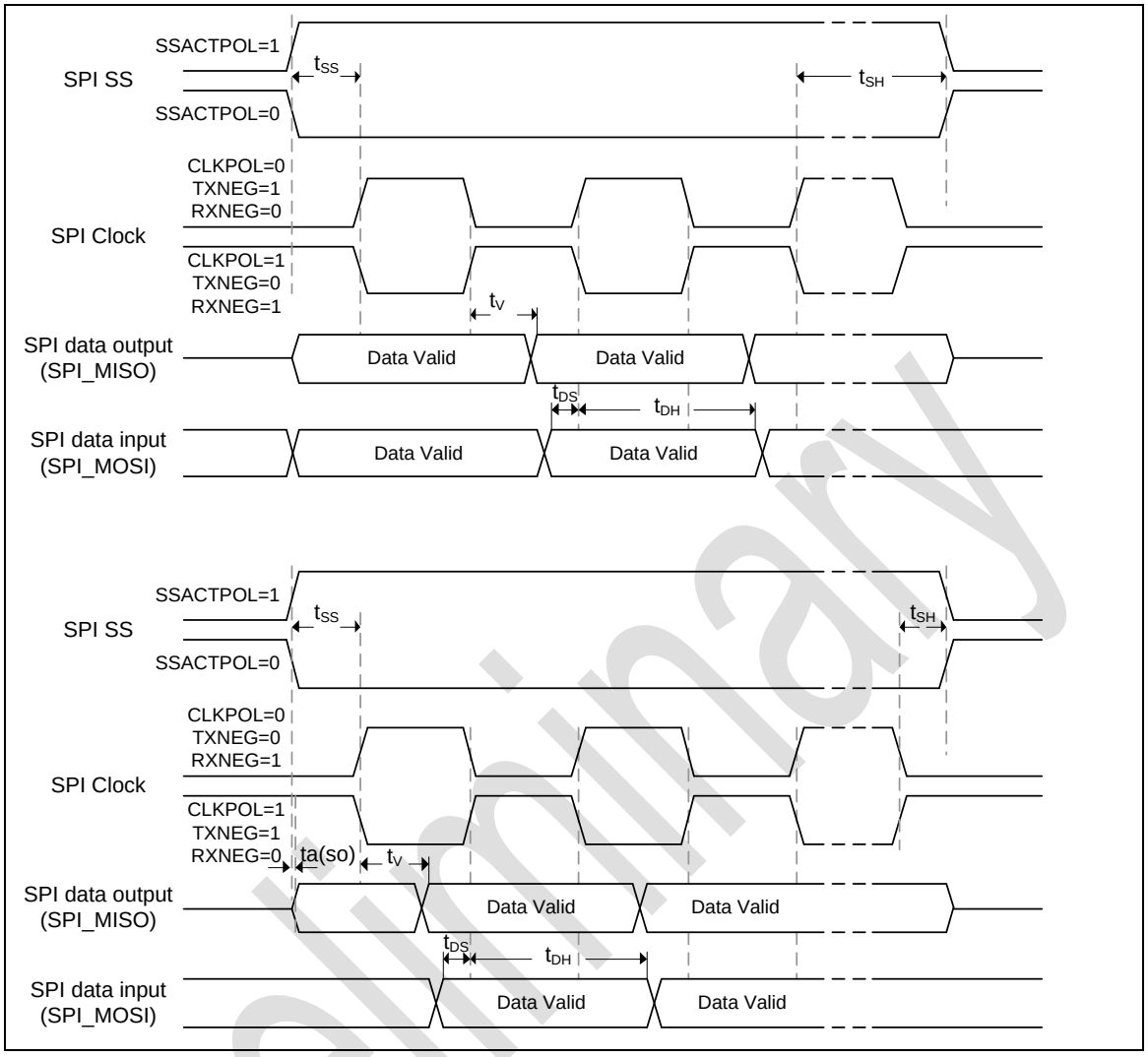


Figure 6.9-3 SPI Slave Mode Timing Diagram

6.9.4 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40		ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40			
$t_{v(WS)}$	WS valid time	4			Master mode
$t_{h(WS)}$	WS hold time	1			Master mode
$t_{su(WS)}$	WS setup time	24			Slave mode
$t_{h(WS)}$	WS hold time	0			Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10		ns	Master receiver
$t_{su(SD\_SR)}$		7			Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7			Master receiver
$t_{h(SD\_SR)}$		4			Slave receiver
$t_{v(SD\_ST)}$	Data output valid time		10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4			Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time		4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0			Master transmitter (after enable edge)

Table 6.9-1 I²S Dynamic Characteristics

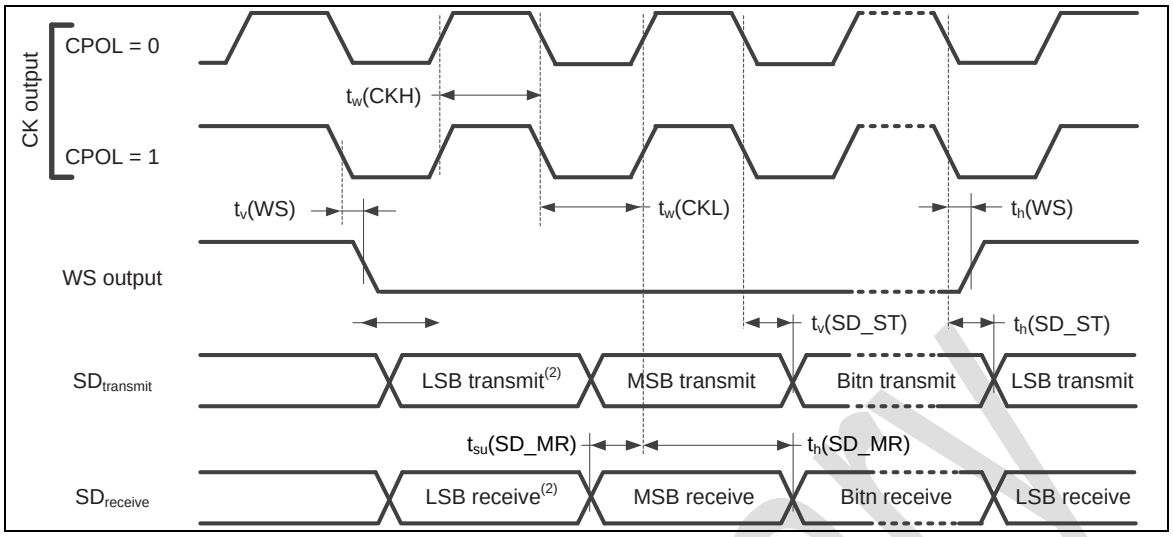


Figure 6.9-4 I²S Master Mode Timing Diagram

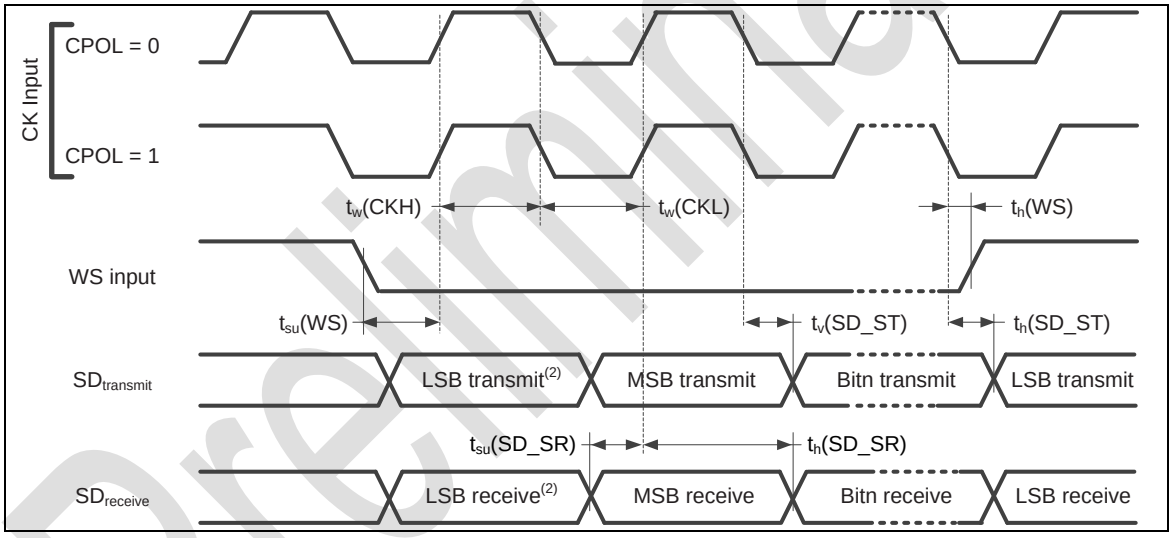


Figure 6.9-5 I²S Slave Mode Timing Diagram

7 APPLICATION CIRCUIT

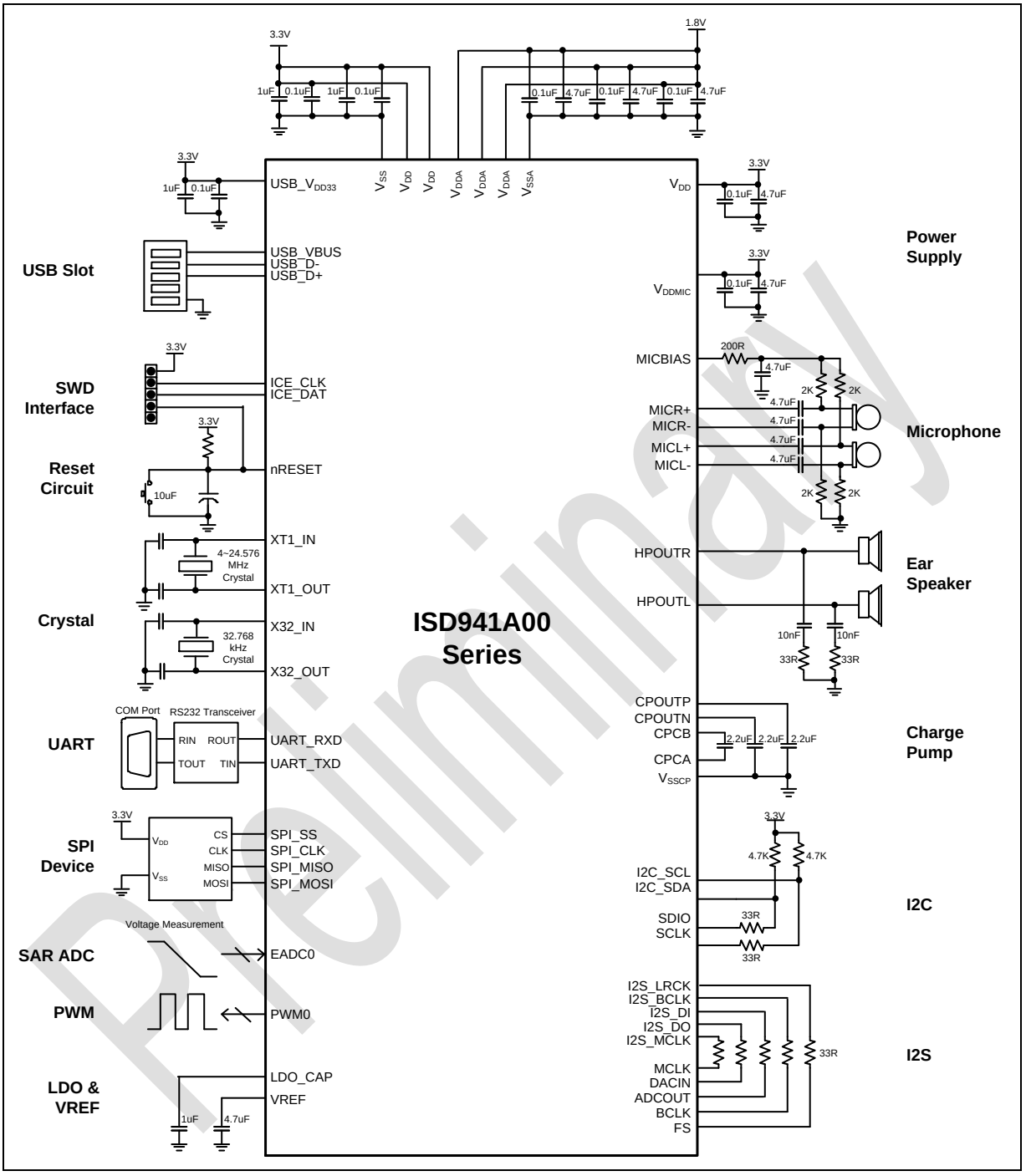
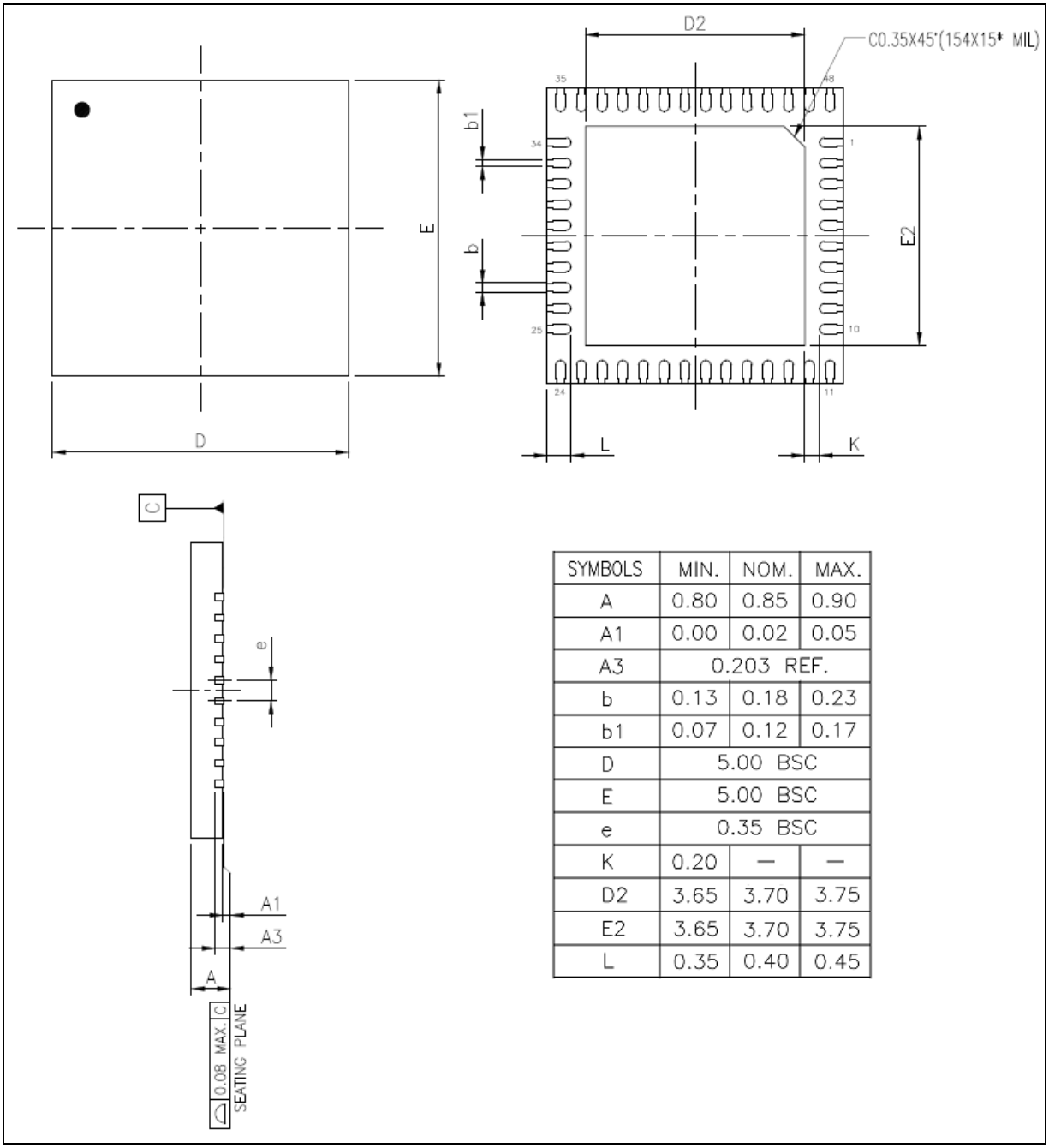


Figure 7-1 Application Circuit

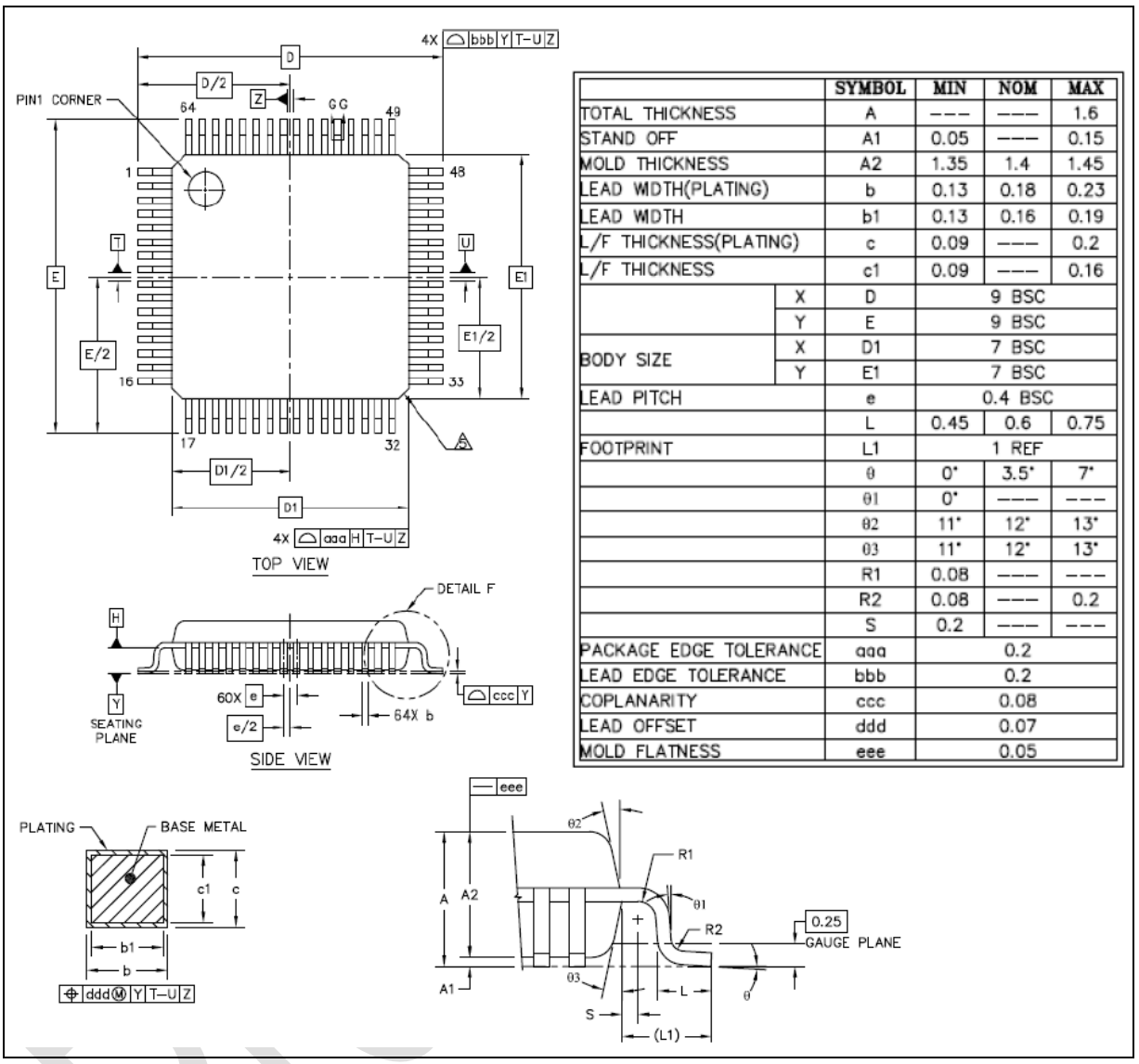
8 PACKAGE DIMENSIONS

8.1 QFN 48 (5x5x0.85 mm^3 Pitch 0.35 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—
D2	3.65	3.70	3.75
E2	3.65	3.70	3.75
L	0.35	0.40	0.45

8.2 LQFP 64L (7x7x1.4 mm³ footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

9 REVISION HISTORY

Date	Revision	Description
2020.08.27	1.00	1. Preliminary version release
2021.01.28	1.01	1. Added QFN48 package

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.